

TLV62585 3-A High Efficiency Synchronous Buck Converter in QFN or SOT563 Package

1 Features

- Up to 95% Efficiency
- Low $R_{DS(ON)}$ Power Switches 56 mΩ / 32 mΩ
- 2.5-V to 5.5-V Input Voltage Range
- Adjustable Output Voltage from 0.6-V to V_{IN}
- Power Save Mode for Light Load Efficiency
- 100% Duty Cycle for Lowest Dropout
- 35-μA Operating Quiescent Current
- 1.5-MHz Typical Switching Frequency
- Short Circuit Protection (HICCUP)
- Output Discharge
- Power Good Output
- Thermal Shutdown Protection
- Available in 2-mm × 2-mm QFN or 1.6-mm × 1.6-mm SOT563 Package
- Create a Custom Design Using the TLV62585 With the [WEBENCH® Power Designer](#)

2 Applications

- General Purpose Point-of-Load Supply
- Battery-Powered Application
- Wireless Router, Solid State Drive
- Set-top Box, Multi Functional Printer
- Motor Control

3 Description

The TLV62585 device is a high-frequency synchronous step-down converter optimized for compact solution size and high efficiency. The device integrates switches capable of delivering an output current up to 3 A. At medium to heavy loads, the converter operates in pulse width modulation (PWM) mode with typical 1.5-MHz switching frequency. At light load, the device automatically enters Power Save Mode (PSM) to maintain high efficiency over the entire load current range. In shutdown, the current consumption is reduced to less than 2 μA.

The internal compensation circuit allows a compact solution and small external components. An internal soft start circuit limits the inrush current during startup. Other features like short circuit protection, thermal shutdown protection, output discharge and power good are built-in.

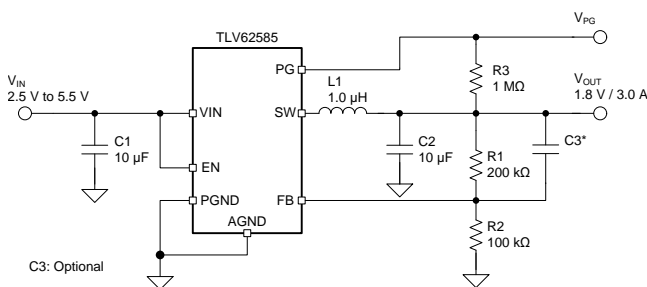
The device is available in a 2-mm × 2-mm QFN or 1.6-mm × 1.6-mm SOT563 package.

Device Information⁽¹⁾

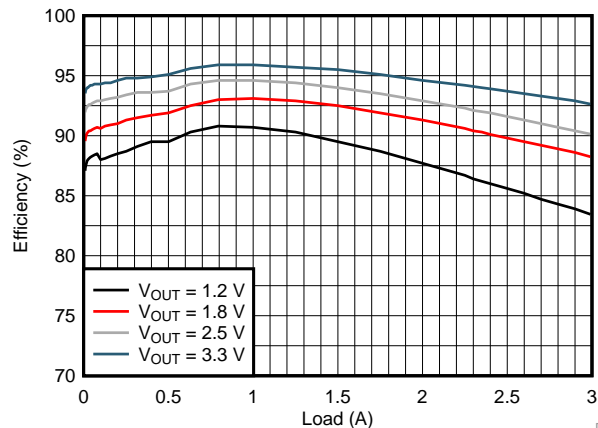
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV62585RWT	QFN (12)	2.00 mm × 2.00 mm
TLV62585DRL	SOT563 (6)	1.60 mm × 1.60 mm
TLV62585PDRL		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



5-V Input Voltage Efficiency



D008



Table of Contents

1 Features	1	8 Application and Implementation	8
2 Applications	1	8.1 Application Information.....	8
3 Description	1	8.2 Typical Application	8
4 Revision History	2	9 Power Supply Recommendations	14
5 Pin Configuration and Functions	3	10 Layout	14
6 Specifications	4	10.1 Layout Guidelines	14
6.1 Absolute Maximum Ratings	4	10.2 Layout Example	14
6.2 ESD Ratings.....	4	10.3 Thermal Considerations	15
6.3 Recommended Operating Conditions.....	4	11 Device and Documentation Support	16
6.4 Thermal Information	4	11.1 Device Support.....	16
6.5 Electrical Characteristics.....	5	11.2 Documentation Support	16
6.6 Typical Characteristics	5	11.3 Receiving Notification of Documentation Updates	16
7 Detailed Description	6	11.4 Community Resources.....	16
7.1 Overview	6	11.5 Trademarks	16
7.2 Functional Block Diagram	6	11.6 Electrostatic Discharge Caution.....	17
7.3 Feature Description.....	6	11.7 Glossary	17
7.4 Device Functional Modes.....	7	12 Mechanical, Packaging, and Orderable Information	17

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2018) to Revision E	Page
• Changed TLV62585DRL and TLV62585PDRL From: <i>Product Preview</i> To: <i>Production</i> data.....	1
• Added PCB layout recommendation for TLV62585PDRL.....	14

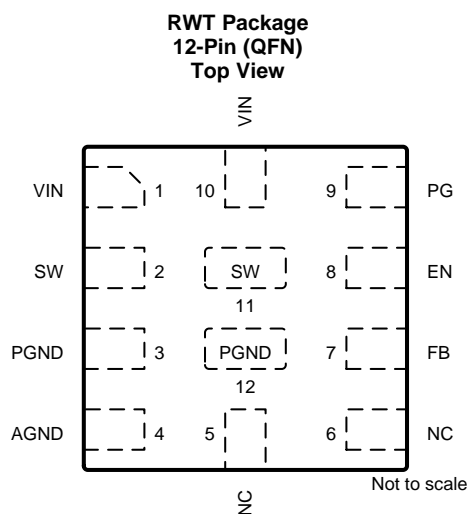
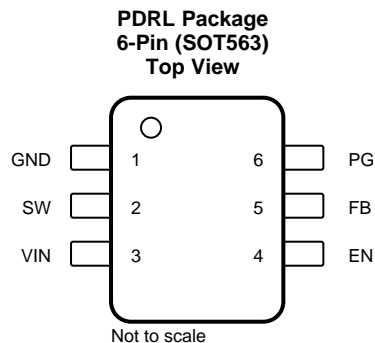
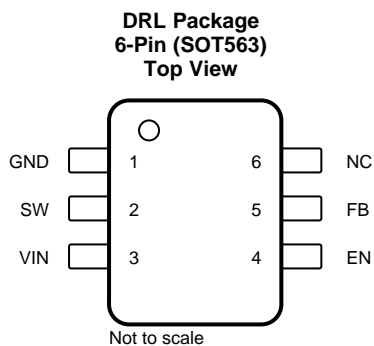
Changes from Revision C (November 2017) to Revision D	Page
• Added TLV62585DRL and TLV62585PDRL to the <i>Device Information</i> table	1
• Added DRL and PDRL devices to the <i>Pin Configurations and Functions</i>	3
• Added the DRL Thermal Information	4
• Added Figure 22	13

Changes from Revision B (September 2017) to Revision C	Page
• Changed HBM From: ± 1000 To: ± 2000 in the <i>ESD Ratings</i> table.....	4

Changes from Revision A (August 2017) to Revision B	Page
• Changed the device status From: <i>Advanced Information</i> To: <i>Production Data</i>	1
• Changed HBM From: TBD To: ± 1000 in the <i>ESD Ratings</i> table	4

Changes from Original (July 2017) to Revision A	Page
• Changed the device status From: <i>Production</i> To: <i>Advanced Information</i>	1
• Changed HBM From: ± 2000 To: TBD in the <i>ESD Ratings</i> table	4

5 Pin Configuration and Functions



Pin Functions

NAME	PIN			I/O	DESCRIPTION
	RWT (QFN)	DRL (SOT563)	PDRL (SOT563)		
VIN	1, 10	3	3	PWR	Power supply voltage pin.
SW	2, 11	2	2	PWR	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
GND	-	1	1	PWR	Ground pin.
PGND	3, 12	-	-	PWR	Power ground pin.
AGND	4	-	-	-	Ground pin.
NC	5, 6	6	-	-	No connection pin. Leave these pins open, or connect those pins to the output or to AGND.
FB	7	5	5	I	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
EN	8	4	4	I	Device enable logic input. Logic high enables the device, logic low disables the device and turns it into shutdown. Do not leave floating.
PG	9	-	6	O	Power good open drain output pin. The pull-up resistor can not be connected to any voltage higher than 5.5 V. If unused, leave it floating or connect to AGND.

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

		MIN	MAX	UNIT
Voltage at Pins ⁽²⁾	VIN, EN, PG	-0.3	6	V
	FB	-0.3	3	
	SW (DC)	-0.3	V _{IN} + 0.3	
	SW (AC, less than 10ns) ⁽³⁾	-3.0	9	
Temperature	Operating Junction, T _J	-40	150	°C
	Storage, T _{stg}	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) While switching

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage range	2.5		5.5	V
V _{OUT}	Output voltage range	0.6		V _{IN}	V
I _{SINK_PG}	Sink current at PG pin			1	mA
I _{OUT}	Output current	0		3	A
T _J	Operating junction temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TLV62585		UNIT
		RWT [QFN]	DRL [SOT]	
R _{θJA}	Junction-to-ambient thermal resistance	95.7	132.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	74.1	43.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	29.4	27.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	5.8	1.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	29.7	26.6	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

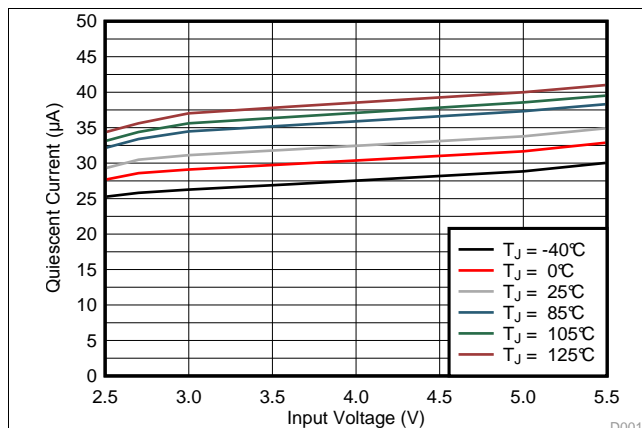
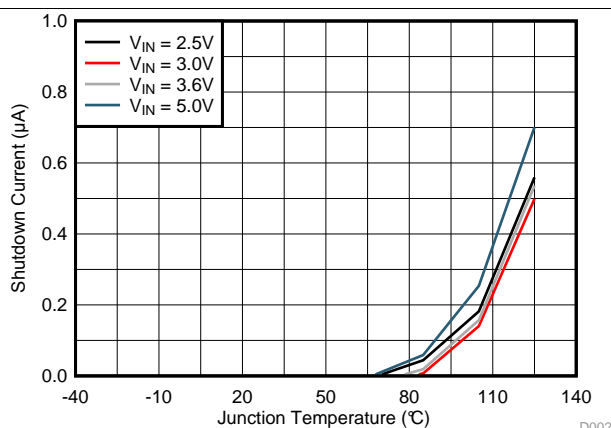
- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

 $T_J = 25\text{ }^\circ\text{C}$, and $V_{IN} = 5\text{ V}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current into VIN	No load, device not switching		35		μA
I_{SD}	Shutdown current into VIN	EN = Low		0.7	2	μA
V_{UVLO}	Under voltage lock out threshold	V_{IN} falling		2.3	2.45	V
	Under voltage lock out hysteresis			150		mV
T_{JSD}	Thermal shutdown threshold	T_J rising		150		$^\circ\text{C}$
	Thermal shutdown hysteresis			20		$^\circ\text{C}$
LOGIC INTERFACE EN						
V_{IH}	High-level input voltage	$V_{IN} = 2.5\text{ V to }5.5\text{ V}$	1.2			V
V_{IL}	Low-level input voltage	$V_{IN} = 2.5\text{ V to }5.5\text{ V}$			0.4	V
SOFT START, POWER GOOD						
t_{SS}	Soft start time	Time from EN high to 95% of V_{OUT} nominal		900		μs
V_{PG}	Power good threshold	V_{OUT} rising, referenced to V_{OUT} nominal		95%		
		V_{OUT} falling, referenced to V_{OUT} nominal		90%		
$V_{PG,OL}$	Low-level output voltage	$I_{sink} = 1\text{ mA}$			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	$V_{PG} = 5.0\text{ V}$		0.01		μA
$t_{PG,DLY}$	Power good delay	V_{FB} falling		40		μs
OUTPUT						
V_{FB}	Feedback regulation voltage	PWM mode, $2.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	594	600	606	mV
		PWM mode, $2.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $-40^\circ\text{C to }125^\circ\text{C}$	588	600	612	
$I_{FB,LKG}$	Feedback input leakage current	$V_{FB} = 0.6\text{ V}$		0.01		μA
R_{DIS}	Output discharge FET on-resistance	EN = Low, $V_{OUT} = 1.8\text{ V}$		10		Ω
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance			56		m Ω
	Low-side FET on-resistance			32		m Ω
I_{LIM}	High-side FET switch current limit		4	4.6		A
f_{SW}	PWM switching frequency	$V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 1\text{ A}$		1.5		MHz

6.6 Typical Characteristics


Figure 1. Quiescent Current vs Input Voltage

Figure 2. Shutdown Current vs Junction Temperature

7 Detailed Description

7.1 Overview

The TLV62585 is a high-efficiency synchronous step-down converter. The device operates with an adaptive off-time with peak current control scheme. The device operates at typically 1.5-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the V_{IN}/V_{OUT} ratio, a simple circuit sets the required off time for the low-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current.

7.2 Functional Block Diagram

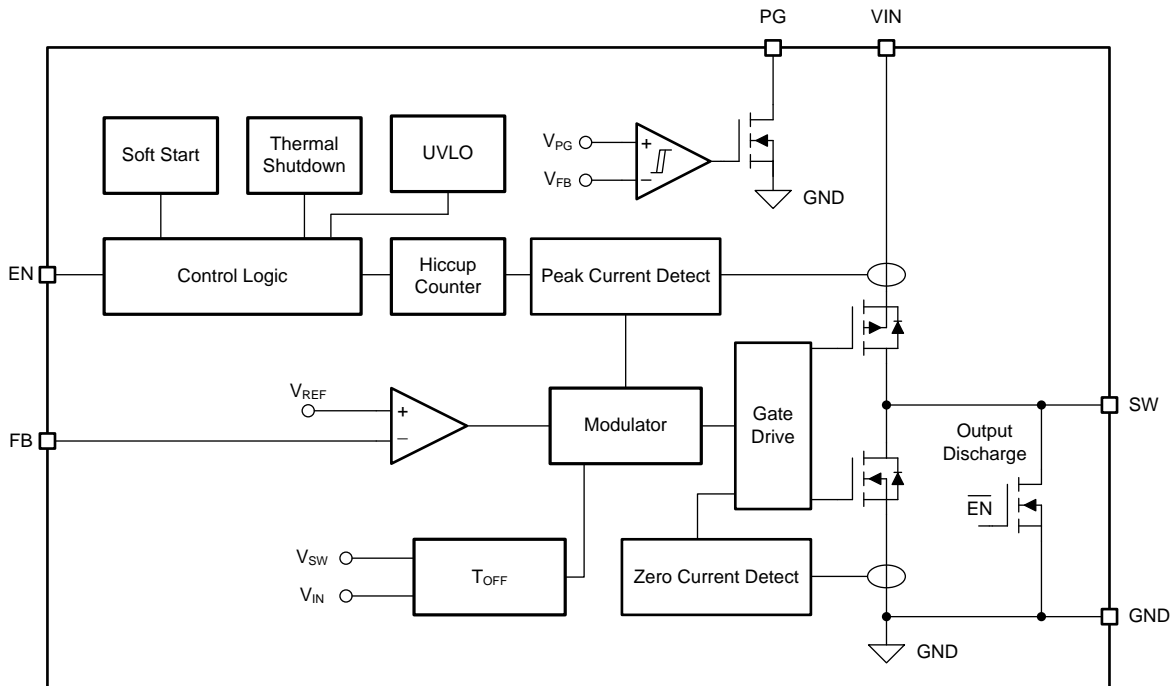


Figure 3. Functional Block Diagram

7.3 Feature Description

7.3.1 Power Save Mode

The device automatically enters Power Save Mode to improve efficiency at light load when the inductor current becomes discontinuous. In Power Save Mode, the converter reduces switching frequency and minimizes current consumption. In Power Save Mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor, or adding a feed forward capacitor, as shown in [Figure 14](#).

7.3.2 100% Duty Cycle Low Dropout Operation

The device offers low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times R_{DS(ON)} + R_L$$

Where

- $R_{DS(ON)}$ = High side FET on-resistance
- R_L = Inductor ohmic resistance (DCR)

(1)

Feature Description (continued)

7.3.3 Soft Start

After enabling the device, internal soft startup circuitry ramps up the output voltage which reaches nominal output voltage during a startup time. This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The TLV62585 is able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

7.3.4 Switch Current Limit and Short Circuit Protection (HICCUP)

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current might occur with a shorted or saturated inductor or a over load or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM} , the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current with an adaptive off-time.

When this switch current limits is triggered 32 times, the device reduces the current limit for further 32 cycles and then stops switching to protect the output. The device then automatically start a new startup after a typical delay time of 500 μ s has passed. This is named HICCUP short circuit protection. The devices repeat this mode until the high load condition disappears. HICCUP protection is also enabled during the startup.

7.3.5 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) is implemented, which shuts down the device at voltages lower than V_{UVLO} with a hysteresis of 150 mV.

7.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops switching when the junction temperature exceeds T_{JSD} . When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

7.4 Device Functional Modes

7.4.1 Enable and Disable

The device is enabled by setting the EN pin to a logic HIGH. Accordingly, shutdown mode is forced if the EN pin is pulled LOW with a shutdown current of typically 0.7 μ A.

In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal output discharge FET discharges the output through the SW pin smoothly.

7.4.2 Power Good

The TLV62585 has a power good output. The power good goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

Table 1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, $V_{FB} \geq V_{PG}$	√	
	EN = High, $V_{FB} \leq V_{PG}$		√
Shutdown	EN = Low		√
Thermal Shutdown			√
UVLO	$1.4 \text{ V} < V_{IN} < 2.3 \text{ V}$		√
Power Supply Removal	$V_{IN} \leq 1.4 \text{ V}$	√	

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV62585 is a synchronous step-down converter in which output voltage is adjusted by component selection. The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

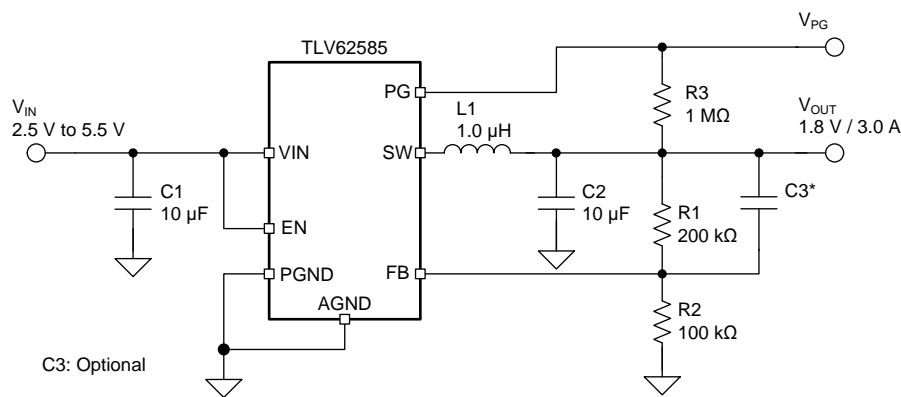


Figure 4. 1.8-V Output Voltage Application

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.5 V to 5.5 V
Output voltage	1.8 V
Maximum output current	3 A

Table 3 lists the components used for the example.

Table 3. List of Components⁽¹⁾

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10 µF, Ceramic capacitor, 10 V, X7R, size 0805, GRM21BR71A106ME51	Murata
C2	22 µF, Ceramic capacitor, 6.3 V, X7T, size 0805, GRM21BD70J226ME44	Murata
C3	Optional	Std
L1	1 µH, Power Inductor, size 4 mm × 4 mm × 1.5 mm, XFL4020-102ME	Coilcraft
R1	Depending on the output voltage, 1%, size 0603;	Std
R2	100 kΩ, Chip resistor, 1/16 W, 1%, size 0603;	Std
R3	1 MΩ, Chip resistor, 1/16 W, 1%, size 0603	Std

(1) See [Third-Party Products](#) disclaimer.

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TLV62585 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Setting The Output Voltage

The output voltage is set by an external resistor divider according to [Equation 2](#):

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.6V \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

R2 must not be higher than 100 k Ω to achieve high efficiency at light load while providing acceptable noise sensitivity.

8.2.2.3 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify the selection process, [Table 4](#) outlines possible inductor and capacitor value combinations for most applications.

Table 4. Matrix of Output Capacitor and Inductor Combinations

NOMINAL L [μ H] ⁽¹⁾	NOMINAL C _{OUT} [μ F] ⁽²⁾⁽³⁾			
	10	22	47	100
0.47				
1	+	+ ⁽⁴⁾	+	
2.2				

- (1) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
- (2) For low output voltage applications (< 1.8 V), more output capacitance is recommended (usually \geq 22 μ F) for smaller ripple. For output capacitance higher than 47 μ F, a feed forward capacitor is needed.
- (3) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.
- (4) Typical application configuration. Other '+' mark indicates recommended filter combinations.

8.2.2.4 Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, [Equation 3](#) is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

where

- $I_{OUT,MAX}$ = Maximum output current
- ΔI_L = Inductor current ripple
- f_{SW} = Switching frequency
- L = Inductor value

(3)

TI recommends choosing the saturation current for the inductor 20% to 30% higher than the $I_{L,MAX}$, out of [Equation 3](#). A higher inductor value is also useful to lower ripple current but increases the transient response time as well.

8.2.2.5 Input and Output Capacitor Selection

The architecture of the TLV62585 allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep its resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric.

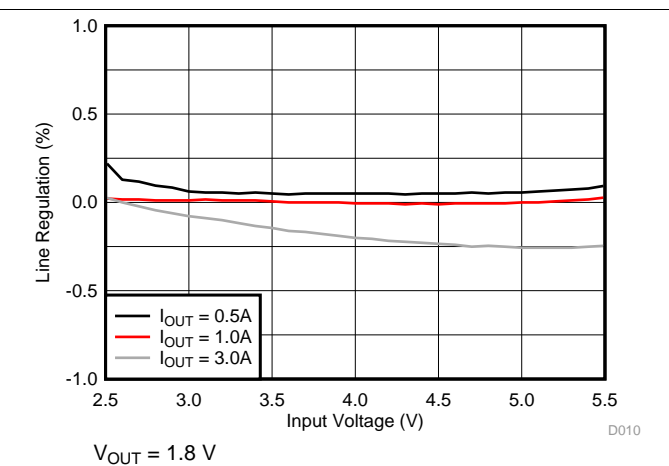
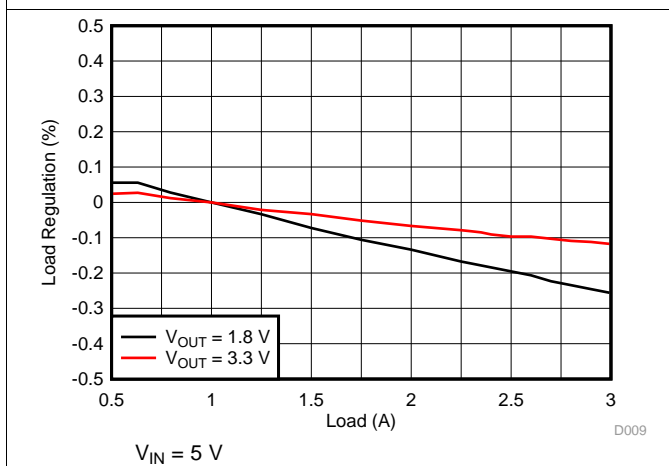
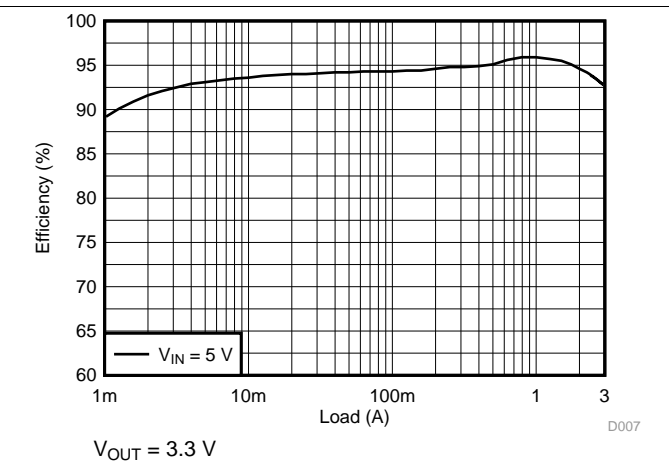
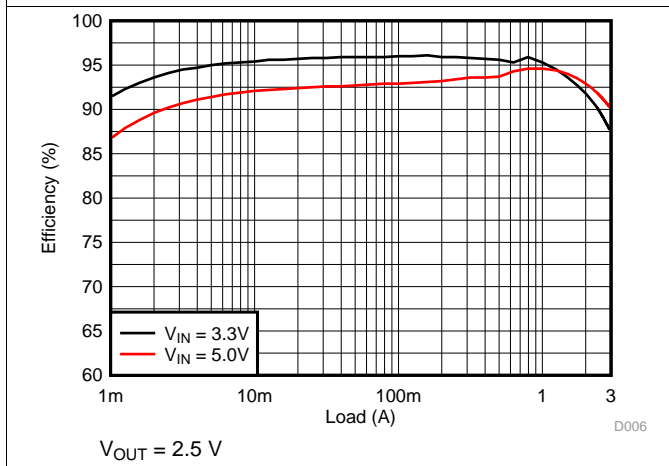
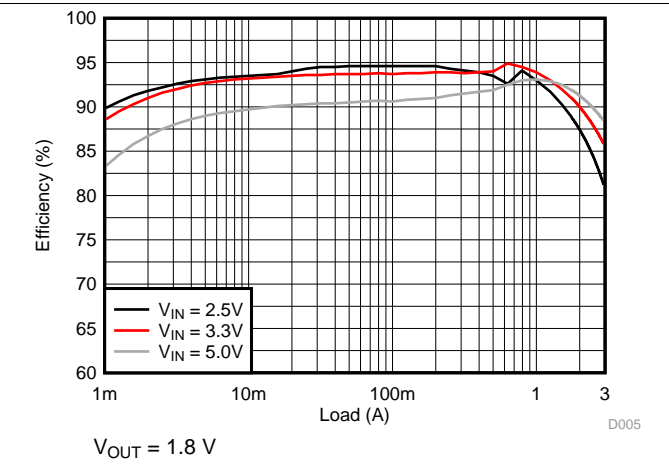
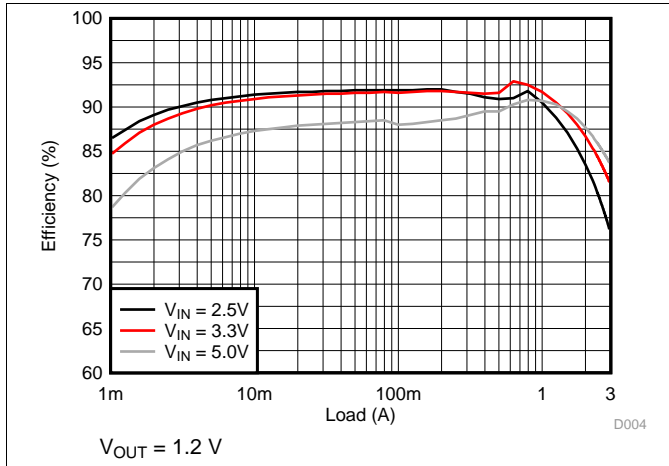
The input capacitor is the low impedance energy source for the converter that helps provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering. For most applications, 10- μ F input capacitor is sufficient; a larger value reduces input voltage ripple.

The TLV62585 is designed to operate with an output capacitor of 10 μ F to 47 μ F, as outlined in [Table 4](#).

A feed forward capacitor reduces the output ripple in PSM and improves the load transient response. A 22-pF capacitor is good for the 1.8-V output typical application.

8.2.3 Application Curves

$V_{IN} = 5\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted.



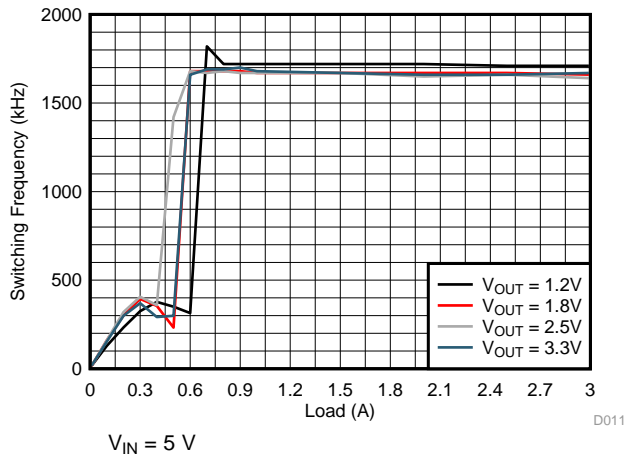


Figure 11. Switching Frequency

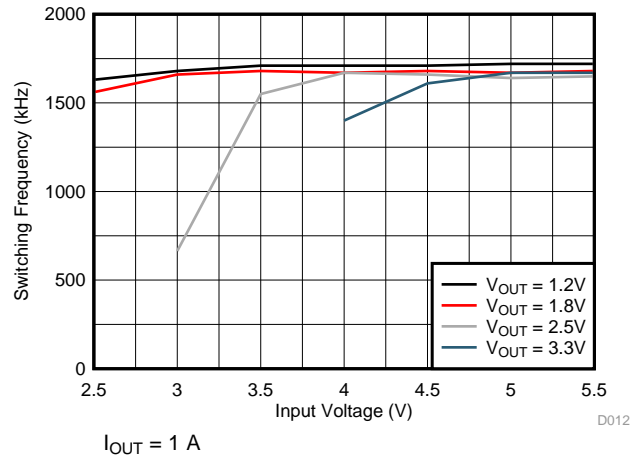


Figure 12. Switching Frequency

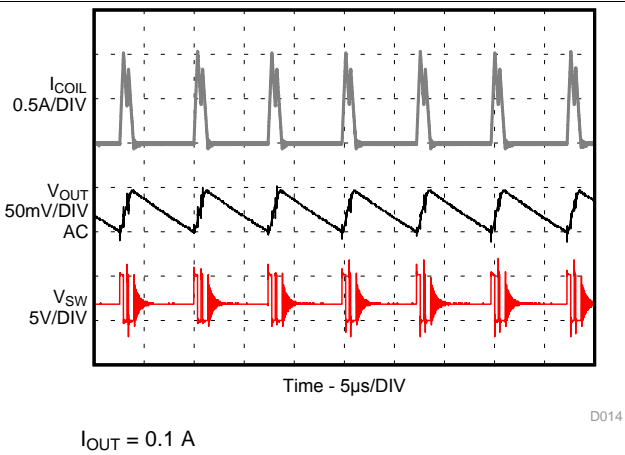


Figure 13. PSM Operation

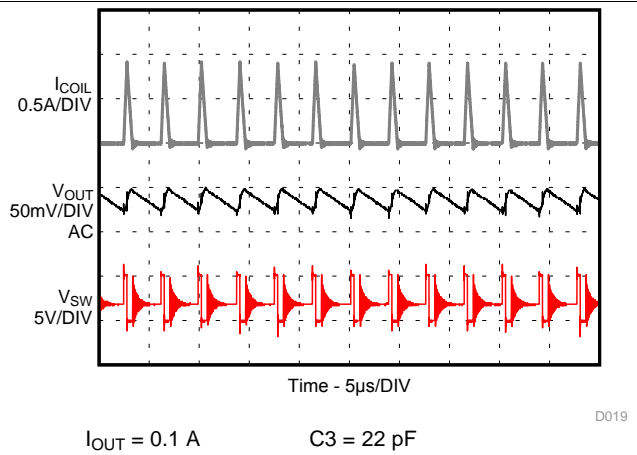


Figure 14. PSM Operation with a Feed Forward Capacitor

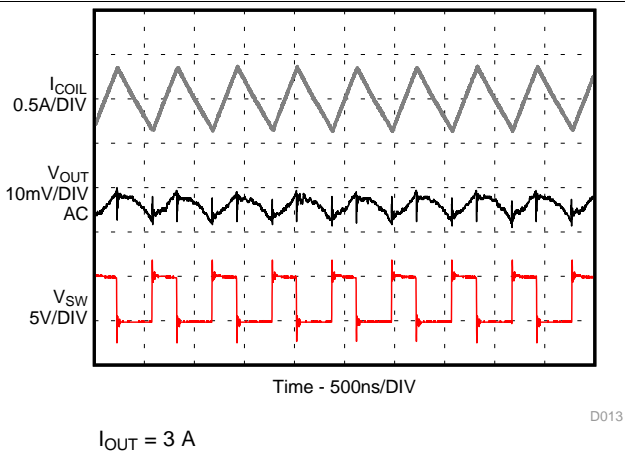


Figure 15. PWM Operation

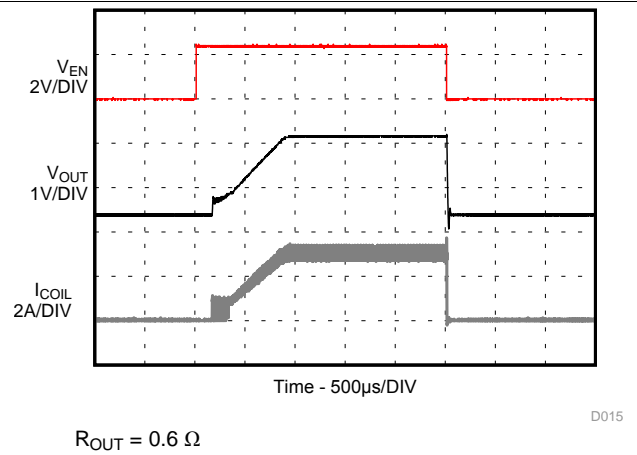
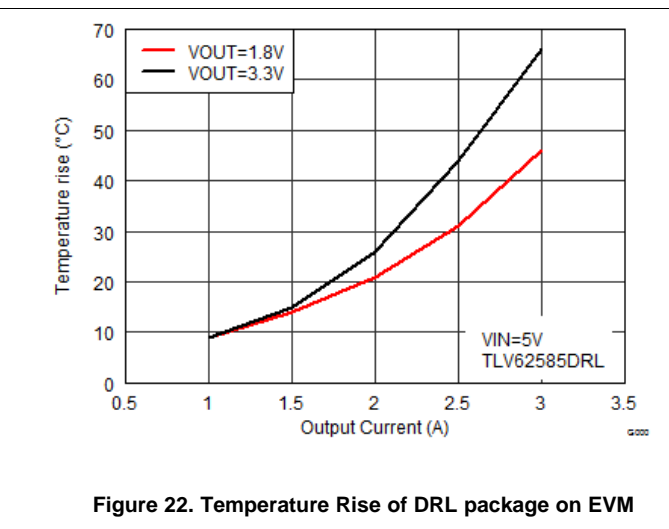
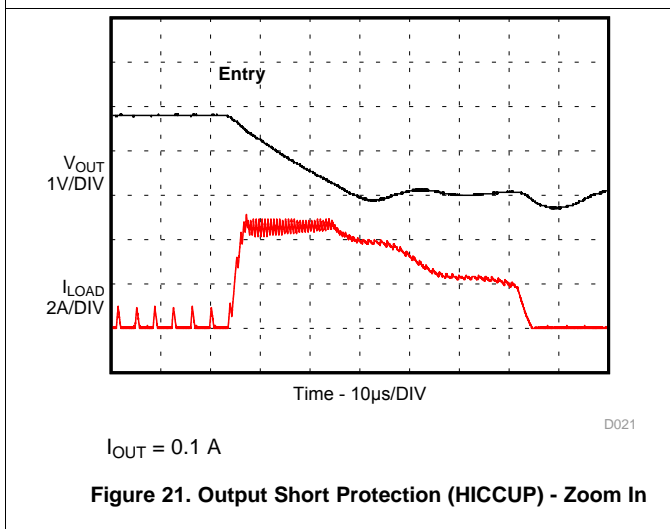
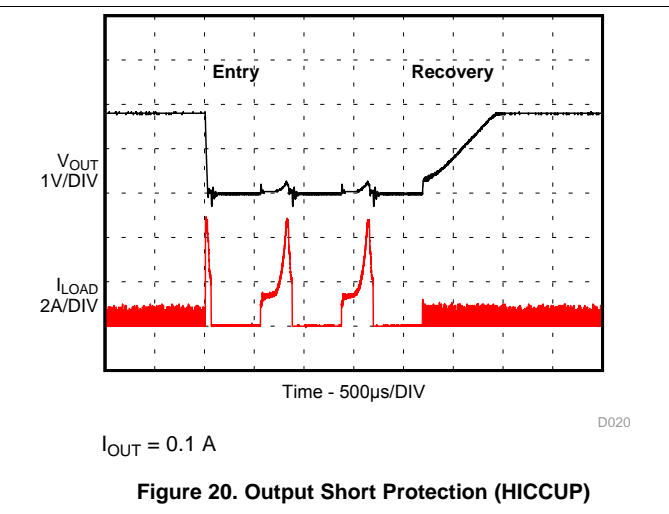
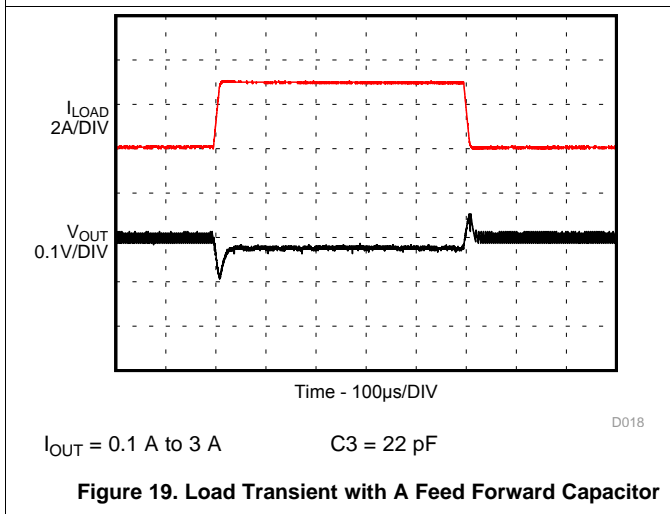
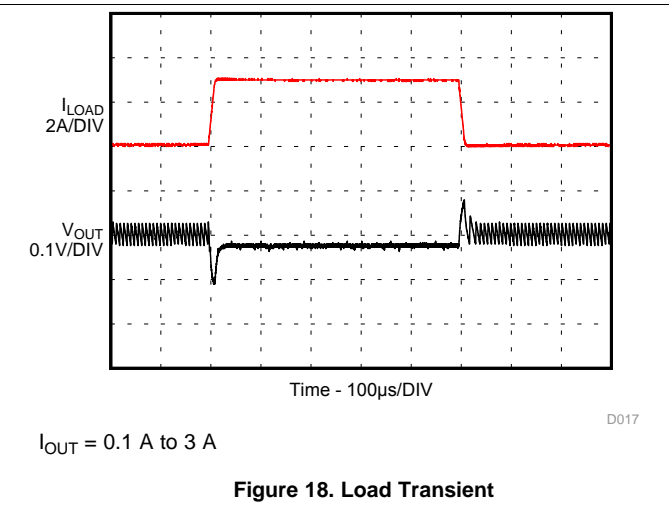
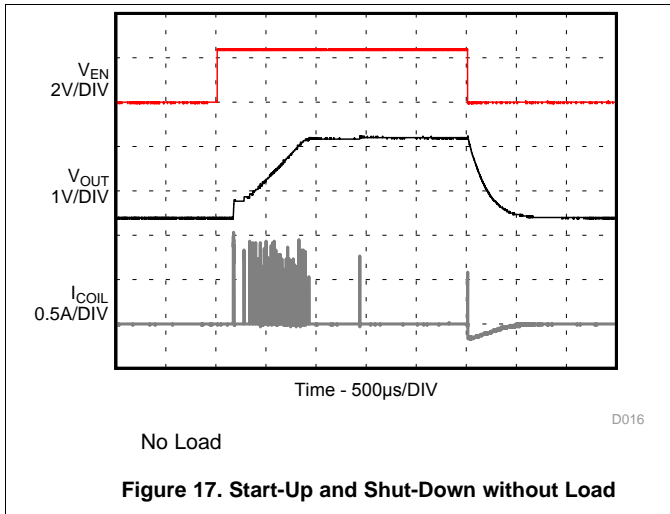


Figure 16. Start-Up and Shut-Down with Load



9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.5 V to 5.5 V. Ensure that the input power supply has a sufficient current rating for the application.

10 Layout

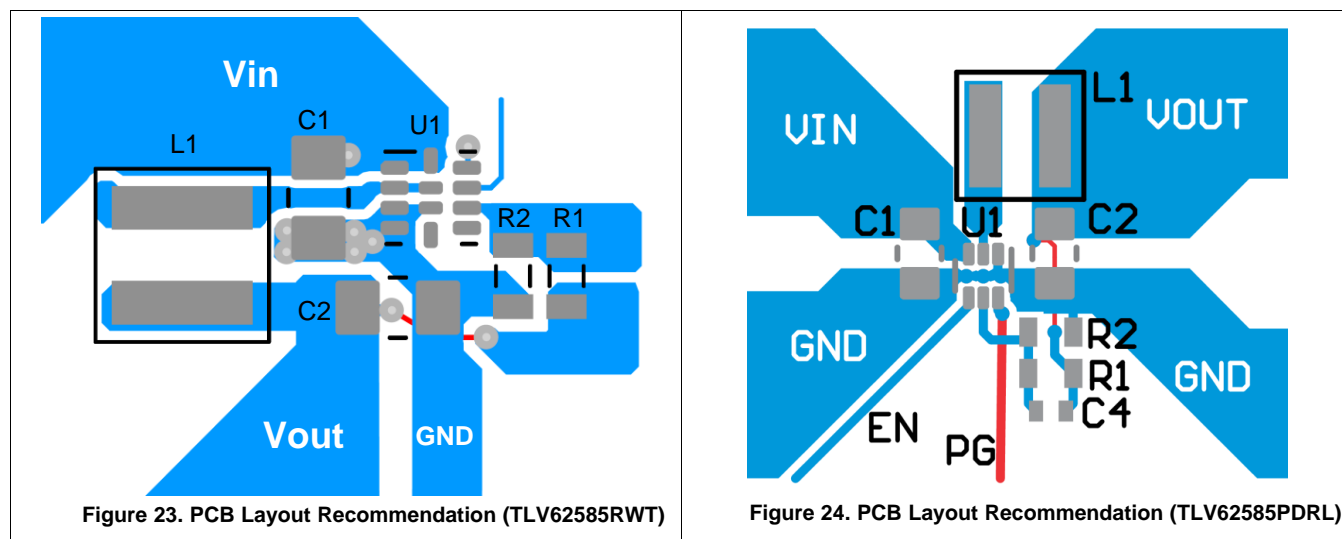
10.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the TLV62585 device.

- The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the GND pin to avoid a ground potential shift.
- The sense traces connected to FB is a signal trace. Special care should be taken to avoid noise being induced. Keep these traces away from SW nodes.
- A common ground should be used. GND layers might be used for shielding.

See [Figure 23](#) and [Figure 24](#) for the recommended PCB layout.

10.2 Layout Example



10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

The big copper planes connecting to the pads of the IC on the PCB improve the thermal performance of the device. For more details on how to use the thermal parameters, see:

- *Thermal Characteristics Application Notes*, [SZZA017](#) and [SPRA953](#)

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TLV62585 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- [Thermal Characteristics Application Note, SZZA017](#)
- [Thermal Characteristics Application Note, SPRA953](#)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV62585DRLR	ACTIVE	SOT-5X3	DRL	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	1BQ	Samples
TLV62585DRLT	ACTIVE	SOT-5X3	DRL	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	1BQ	Samples
TLV62585PDRLR	ACTIVE	SOT-5X3	DRL	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	1BP	Samples
TLV62585PDRLT	ACTIVE	SOT-5X3	DRL	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	1BP	Samples
TLV62585RWTR	ACTIVE	VQFN-HR	RWT	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	17BI	Samples
TLV62585RWTT	ACTIVE	VQFN-HR	RWT	12	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	17BI	Samples
XLV62585DRLT	ACTIVE	SOT-5X3	DRL	6	250	TBD	Call TI	Call TI	-40 to 125		Samples
XLV62585PDRLT	ACTIVE	SOT-5X3	DRL	6	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62585DRLR	SOT-5X3	DRL	6	3000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62585DRLR	SOT-5X3	DRL	6	3000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TLV62585DRLT	SOT-5X3	DRL	6	250	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TLV62585DRLT	SOT-5X3	DRL	6	250	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62585PDRLR	SOT-5X3	DRL	6	3000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TLV62585PDRLR	SOT-5X3	DRL	6	3000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62585PDRLT	SOT-5X3	DRL	6	250	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62585PDRLT	SOT-5X3	DRL	6	250	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TLV62585RWTR	VQFN-HR	RWT	12	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q1
TLV62585RWTT	VQFN-HR	RWT	12	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q1

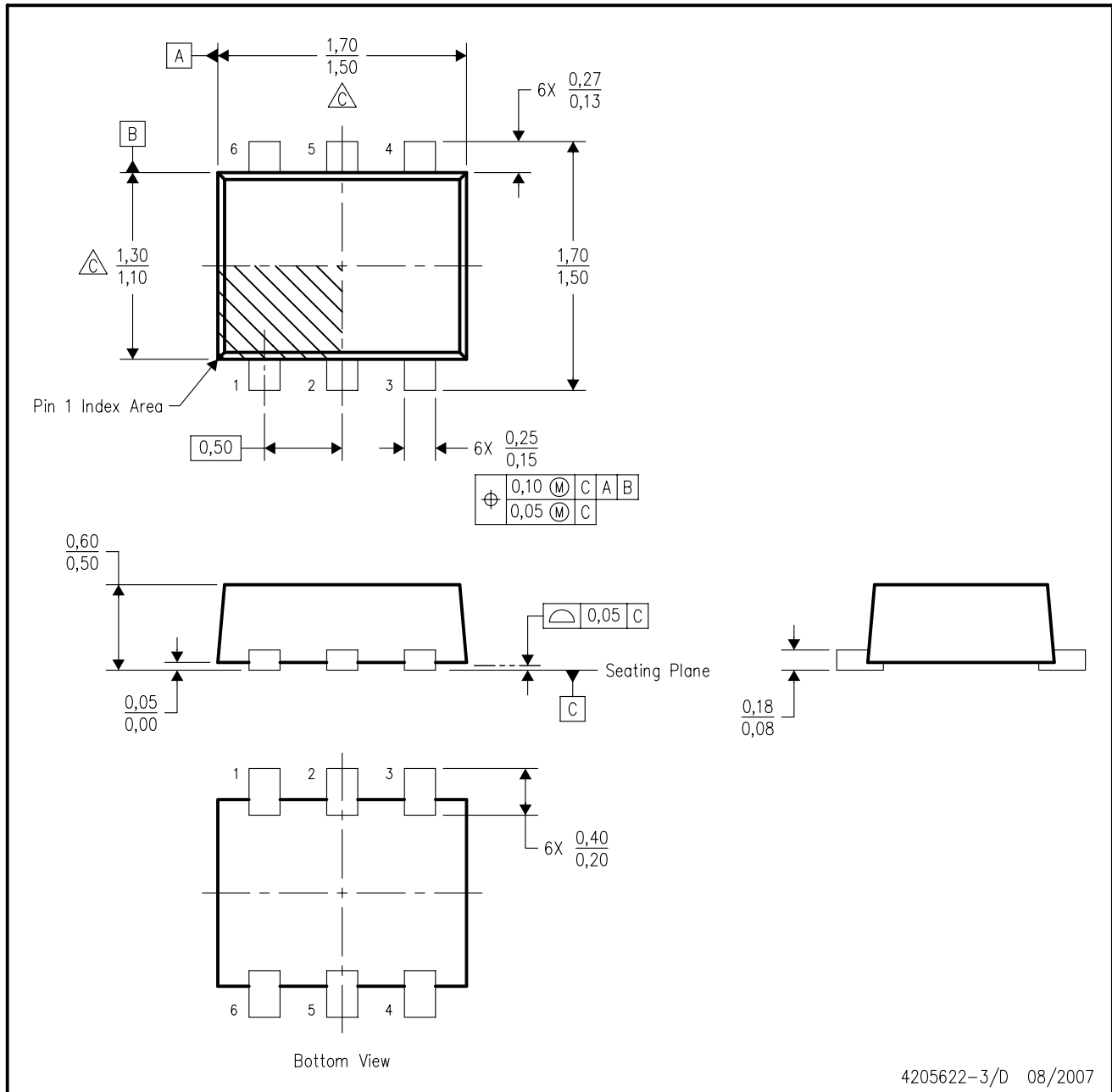
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

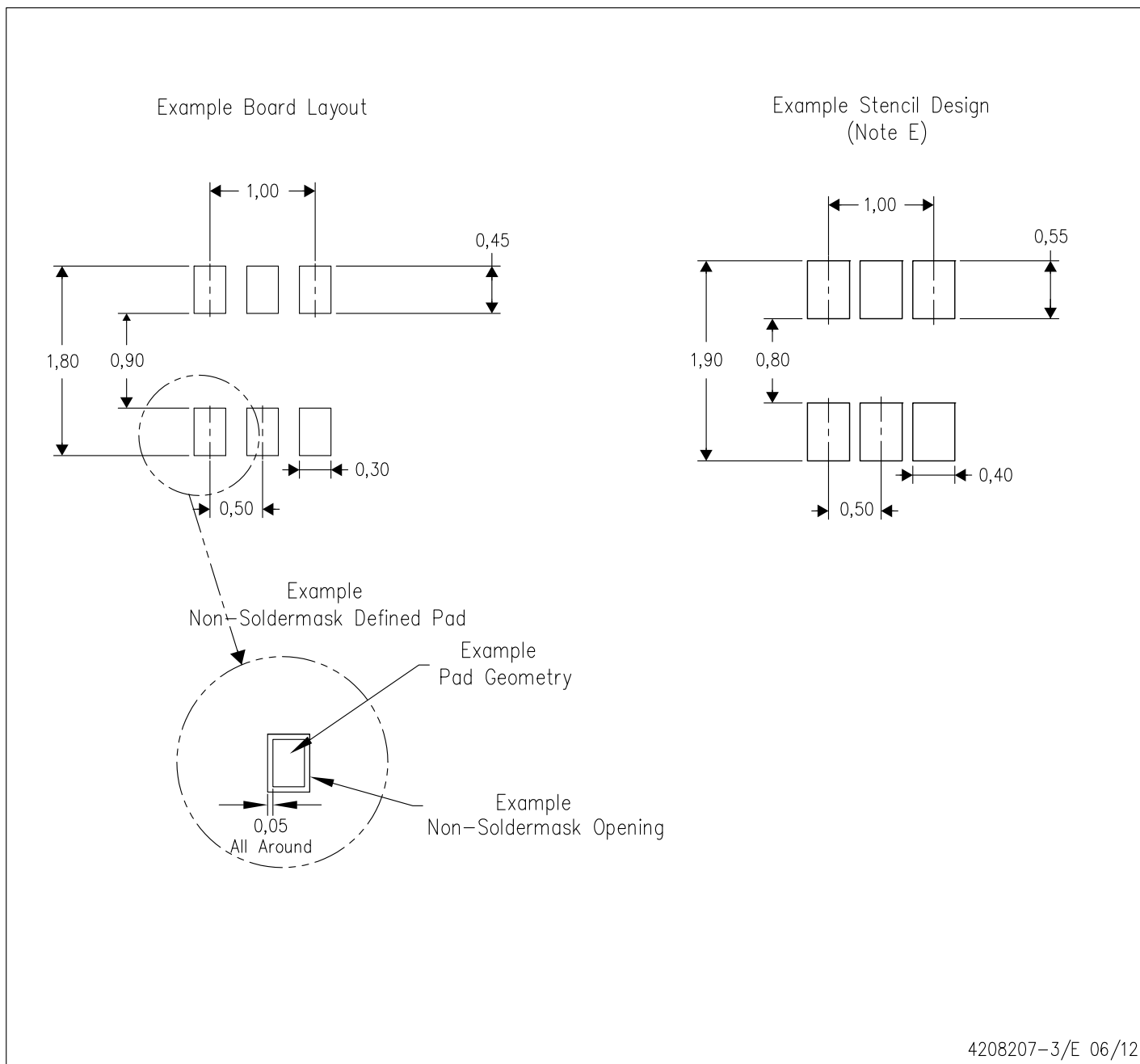
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62585DRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62585DRLR	SOT-5X3	DRL	6	3000	184.0	184.0	19.0
TLV62585DRLT	SOT-5X3	DRL	6	250	184.0	184.0	19.0
TLV62585DRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TLV62585PDRLR	SOT-5X3	DRL	6	3000	184.0	184.0	19.0
TLV62585PDRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62585PDRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TLV62585PDRLT	SOT-5X3	DRL	6	250	184.0	184.0	19.0
TLV62585RWTR	VQFN-HR	RWT	12	3000	210.0	185.0	35.0
TLV62585RWTT	VQFN-HR	RWT	12	250	210.0	185.0	35.0

DRL (R-PDSO-N6)

PLASTIC SMALL OUTLINE

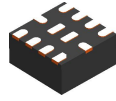


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

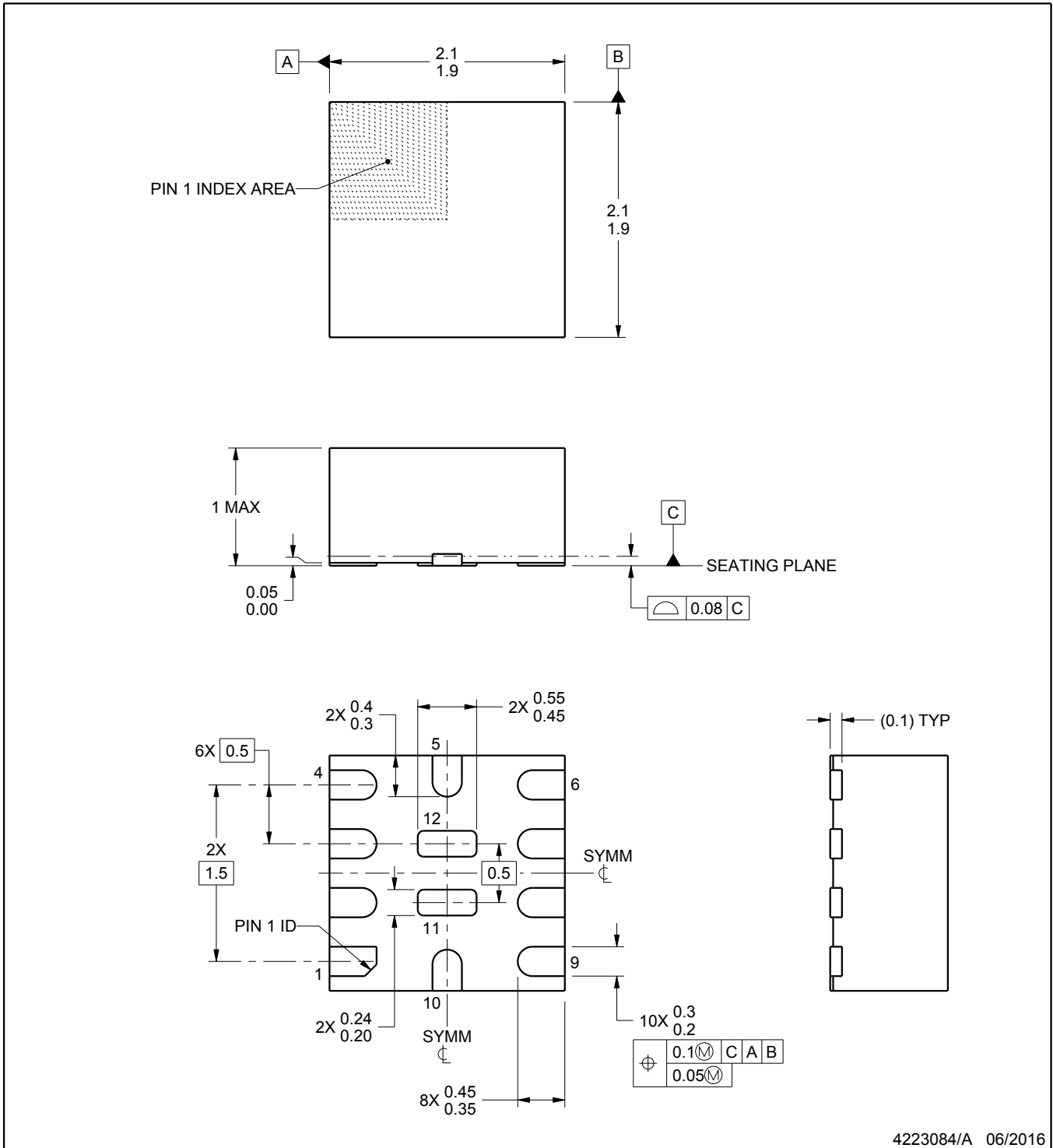
RWT0012A



PACKAGE OUTLINE

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4223084/A 06/2016

NOTES:

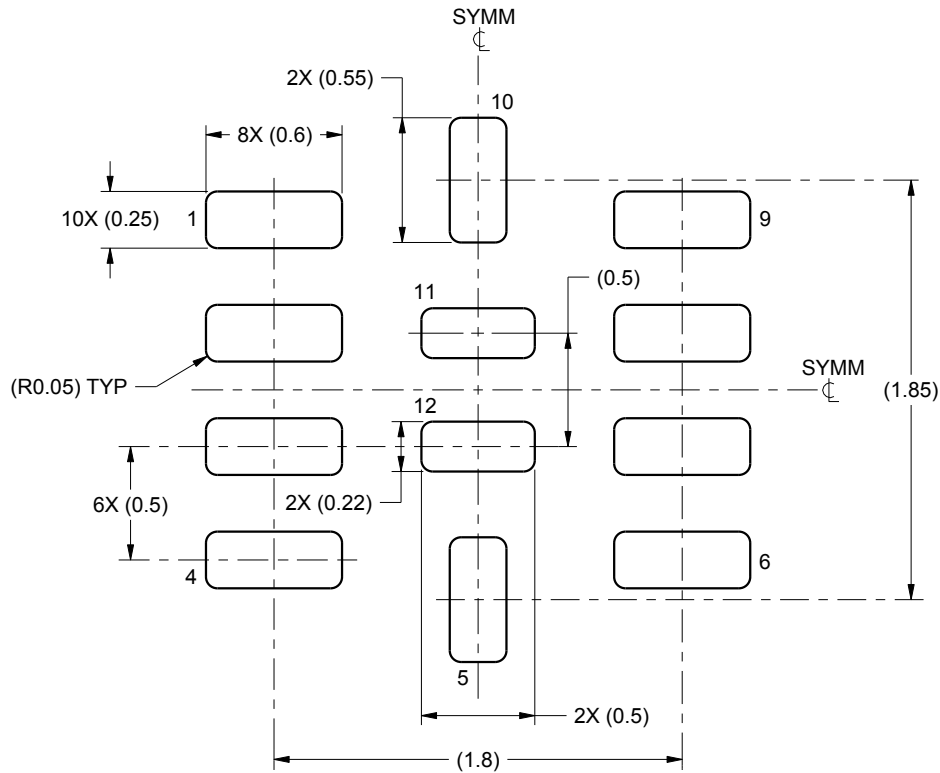
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

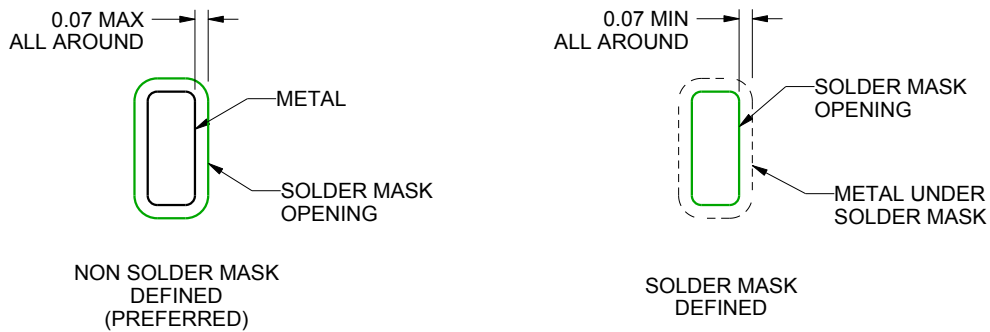
RWT0012A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS

4223084/A 06/2016

NOTES: (continued)

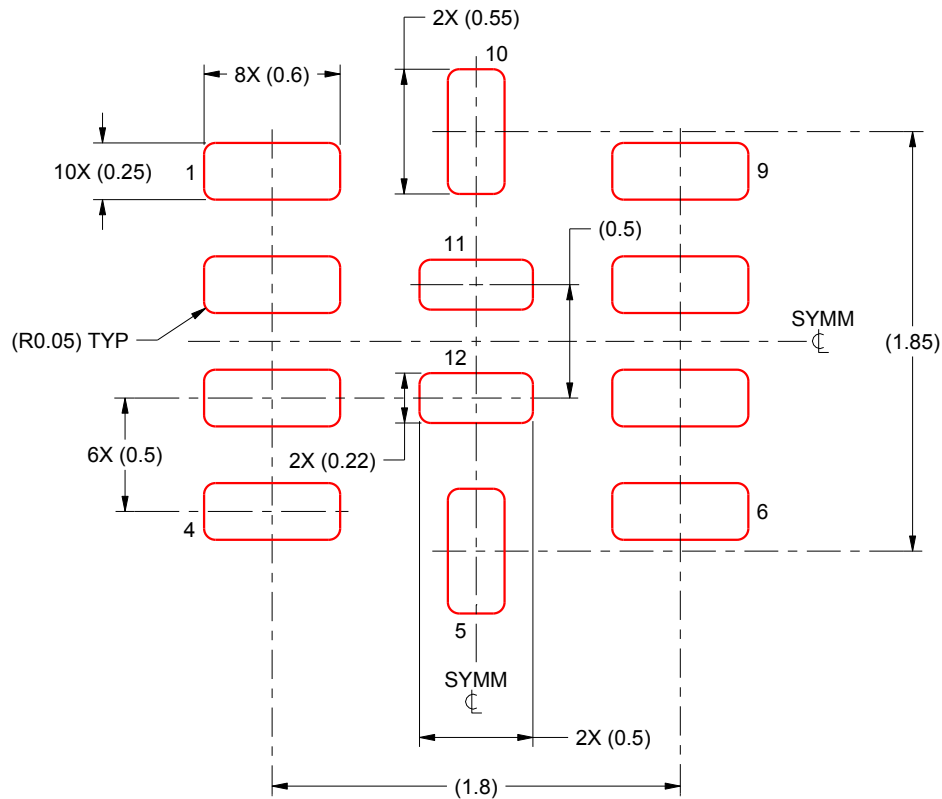
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RWT0012A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223084/A 06/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.