

## SN74LVC1G06 Single Inverter Buffer/Driver With Open-Drain Output

### 1 Features

- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V  $V_{CC}$  Operation
- Input and Open-Drain Output Accept Voltages up to 5.5 V
- Maximum  $t_{pd}$  of 4.5 ns at 3.3 V at 125°C
- Low Power Consumption, 10- $\mu$ A Maximum  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V for open-drain devices
- $I_{off}$  Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Can Be Used For Up or Down Translation
- Schmitt Trigger Action on All Ports

### 2 Applications

- AV Receivers
- Blu-ray Players and Home Theaters
- DVD Recorders and Players
- Desktop or Notebook PCs
- Digital Radio or Internet Radio Players
- Digital Video Cameras (DVC)
- Embedded PCs
- GPS: Personal Navigation Devices
- Mobile Internet Devices
- Network Projector Front-Ends
- Portable Media Players
- Pro Audio Mixers
- Smoke Detectors
- Solid State Drive (SSD): Enterprise
- High-Definition (HDTV)
- Tablets: Enterprise
- Audio Docks: Portable
- DLP Front Projection Systems
- DVR and DVS
- Digital Picture Frame (DPF)
- Digital Still Cameras

### 3 Description

This single inverter buffer and driver is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

The output of the SN74LVC1G06 device is open-drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1G06DBV	SOT-23 (5)	2.90 mm x 1.60 mm
SN74LVC1G06DCK	SC70 (5)	2.00 mm x 1.25 mm
SN74LVC1G06DRL	SOT (5)	1.60 mm x 1.20 mm
SN74LVC1G06DRY	USON (6)	1.45 mm x 1.00 mm
SN74LVC1G06DSF	X2SON (6)	1.00 mm x 1.00 mm
SN74LVC1G06YZP	DSBGA (5)	1.40 mm x 0.90 mm
SN74LVC1G06YZV		0.90 mm x 0.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram (Positive Logic)



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision X (August 2015) to Revision Y</b>	<b>Page</b>
• Changed <i>Logic Diagram (Positive Logic)</i> labels from: A-1, Y-3 to: A-2, Y-4 .....	<b>1</b>
• Added <i>Receiving Notification of Documentation Updates</i> section .....	<b>12</b>

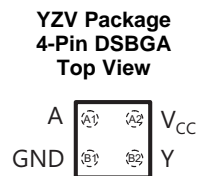
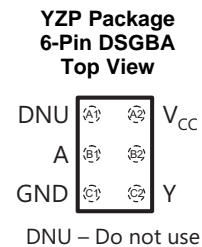
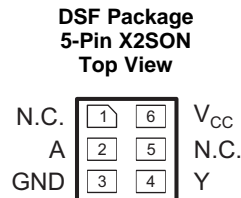
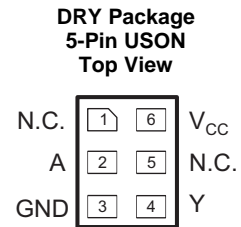
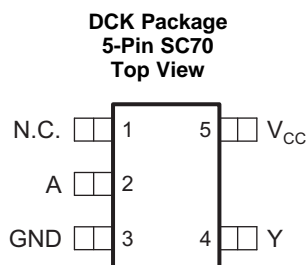
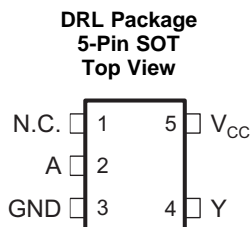
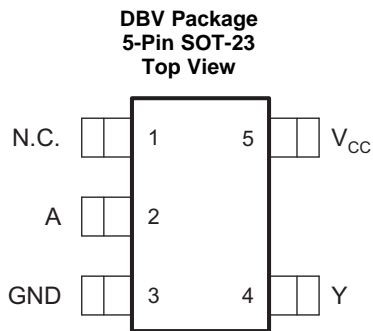
<b>Changes from Revision W (December 2013) to Revision X</b>	<b>Page</b>
• Added <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> section, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>

<b>Changes from Revision V (November 2012) to Revision W</b>	<b>Page</b>
• Updated document to new TI data sheet format .....	<b>1</b>
• Removed <i>Ordering Information</i> table. ....	<b>1</b>
• Updated $I_{off}$ in <i>Features</i> . ....	<b>1</b>
• Updated operating temperature range. ....	<b>6</b>

## 5 Device Comparison Table

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1G06DBV	SOT-23 (5)	2.90 mm × 1.60 mm
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SN74LVC1G06DSF	X2SON (6)	1.00 mm × 1.00 mm
SN74LVC1G06YZP	DSBGA (5)	1.40 mm × 0.90 mm
SN74LVC1G06YZV	DSBGA (4)	0.90 mm × 0.90 mm

## 6 Pin Configuration and Functions



### Pin Functions<sup>(1)(2)</sup>

NAME	PIN				I/O	DESCRIPTION
	DBV, DCK, DRL	DRY, DSF	YZP	YZV		
NC	1	1, 5	A1, B2	–	—	Not connected
A	2	2	B1	A1	I	Input
GND	3	3	C1	B1	—	Ground
Y	4	4	C2	B2	O	Output
V <sub>CC</sub>	5	6	A2	A2	—	Power pin

(1) N.C. – No internal connection

(2) See mechanical drawings for dimensions

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	6.5	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>	-0.5	6.5	V
V <sub>O</sub>	Voltage applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
V <sub>O</sub>	Voltage applied to any output in the high or low state <sup>(2)(3)</sup>	-0.5	6.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-50	mA
I <sub>O</sub>	Continuous output current		±50	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA
T <sub>j</sub>	Junction temperature	-65	150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	+2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	+1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 3 V to 3.6 V	2		
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	
		V <sub>CC</sub> = 3 V to 3.6 V		0.8	
		V <sub>CC</sub> = 4.5 V to 5.5 V		0.3 × V <sub>CC</sub>	
V <sub>I</sub>	Input voltage	0	5.5	V	
V <sub>O</sub>	Output voltage	0	5.5	V	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		4	mA
		V <sub>CC</sub> = 2.3 V		8	
		V <sub>CC</sub> = 3 V		16	
				24	
		V <sub>CC</sub> = 4.5 V		32	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V <sub>CC</sub> = 3.3 V ± 0.3 V		10	
		V <sub>CC</sub> = 5 V ± 0.5 V		5	
T <sub>A</sub>	Operating free-air temperature	-40	125	°C	

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74LVC1G06							UNIT	
	DBV (SOT-23)	DCK (SC70)	DRL (SOT)	DRY (USON)	YZP (DSBGA)	DSF (X2SON)	YZV (DSBGA)		
	5 PINS	5 PINS	5 PINS	6 PINS	5 PINS	6 PINS	4 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	206	252	142	234	132	300	123	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1	V
	I <sub>OL</sub> = 4 mA	1.65 V			0.45	
	I <sub>OL</sub> = 8 mA	2.3 V			0.3	
	I <sub>OL</sub> = 16 mA	3 V			0.4	
	I <sub>OL</sub> = 24 mA				0.55	
	I <sub>OL</sub> = 32 mA	4.5 V			0.55	
I <sub>I</sub>	A input	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V		±1	μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0		±10	μA
I <sub>CC</sub>		V <sub>I</sub> = 5.5 V or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V		10	μA
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V		500	μA

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		4		pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		5		pF

### 7.6 Switching Characteristics, –40°C to +85°C

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	2.2	6.5	1.1	4	1.2	4	1	3	ns

### 7.7 Switching Characteristics, –40°C to +125°C

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

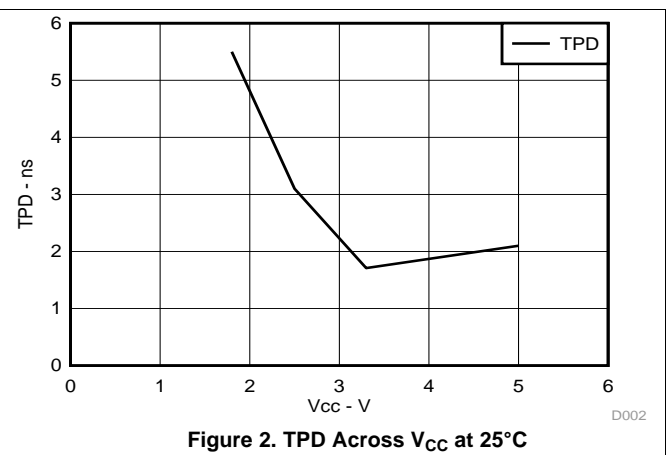
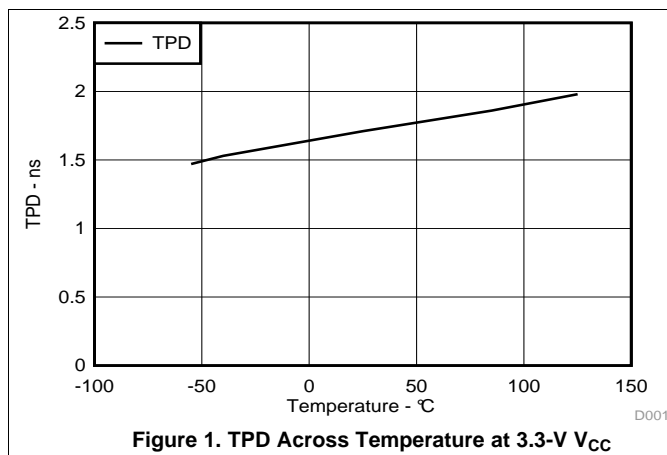
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	2.2	7	1.1	4.5	1.2	4.5	1	3.5	ns

### 7.8 Operating Characteristics

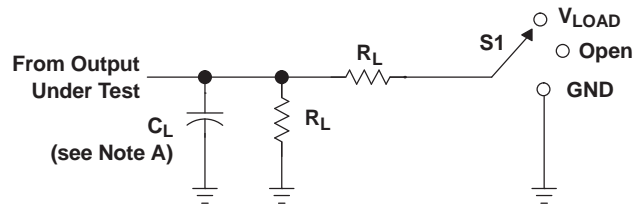
T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
		TYP	TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance f = 10 MHz	3	3	4	6	pF

### 7.9 Typical Characteristics



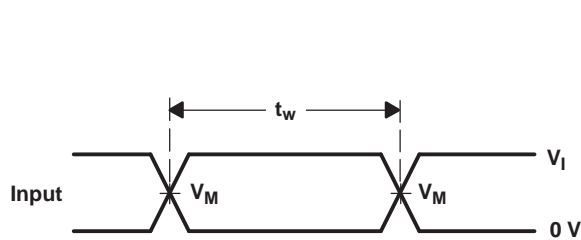
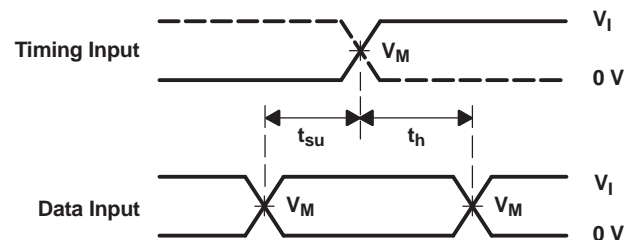
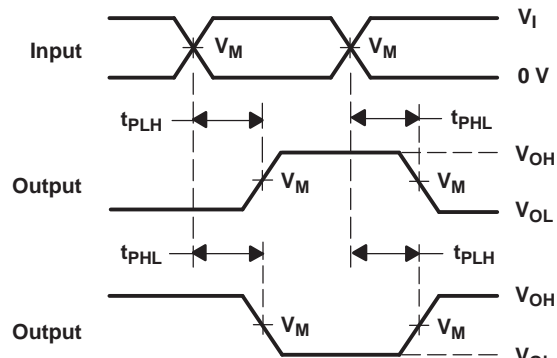
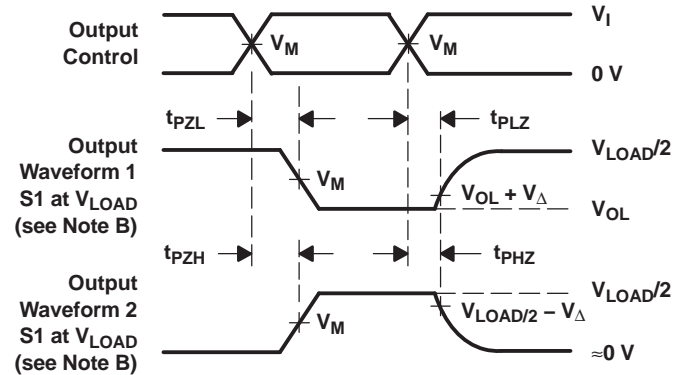
## 8 Parameter Measurement Information



TEST	S1
$t_{PZL}$ (see Notes E and F)	$V_{LOAD}$
$t_{PLZ}$ (see Notes E and G)	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	$V_{LOAD}$

**LOAD CIRCUIT**

$V_{CC}$	INPUT		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V


**VOLTAGE WAVEFORMS  
PULSE DURATION**

**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - Since this device has open-drain outputs,  $t_{PLZ}$  and  $t_{PZL}$  are the same as  $t_{pd}$ .
  - $t_{PZL}$  is measured at  $V_M$ .
  - $t_{PLZ}$  is measured at  $V_{OL} + V_{\Delta}$ .
  - All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms (Open Drain)**



## 9 Detailed Description

### 9.1 Overview

The SN74LVC1G06 device contains one open-drain inverter with a maximum sink current of 32 mA. This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### 9.2 Functional Block Diagram

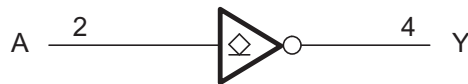


Figure 4. Logic Diagram (Positive Logic)

### 9.3 Feature Description

The wide operating voltage range of 1.65 V to 5.5 V allows the SN74LVC1G06 to be used in systems with many different voltage rails. In addition, the voltage tolerance on the output allows the device to be used for inverting up-translation or down-translation. The  $I_{OFF}$  feature safely allows voltage on the inputs and outputs when no  $V_{CC}$  is present.

### 9.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC1G06.

Table 1. Function Table

INPUT A	OUTPUT Y
L	Hi-Z
H	L

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The SN74LVC1G06 is a high-drive CMOS device that can be used to implement a high output drive buffer, such as an LED application. It can sink 32 mA of current at 4.5 V making it ideal for high-drive applications. It is good for high-speed applications up to 100 MHz. The inputs are 5.5-V tolerant allowing it to translate up or down to  $V_{CC}$ . Below shows a simple LED driver application for a single channel of the device.

### 10.2 Typical Application

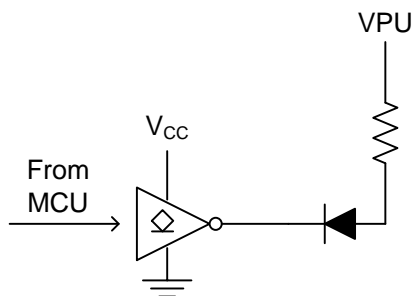


Figure 5. Typical Application Diagram

#### 10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 10.2.2 Detailed Design Procedure

##### 1. Recommended Input Conditions

- Rise time and fall time specs. See  $(\Delta t/\Delta V)$  in the [Recommended Operating Conditions](#) table.
- Specified high and low levels. See  $(V_{IH}$  and  $V_{IL})$  in the [Recommended Operating Conditions](#) table.
- Inputs are overvoltage tolerant allowing them to go as high as  $(V_I \text{ max})$  in the [Recommended Operating Conditions](#) table at any valid  $V_{CC}$ .

##### 2. Recommended Output Conditions

- Load currents should not exceed  $(I_O \text{ max})$  per output and should not exceed (Continuous current through  $V_{CC}$  or GND) total current for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
- Outputs should not be pulled above 5.5 V.

## Typical Application (continued)

### 10.2.3 Application Curve

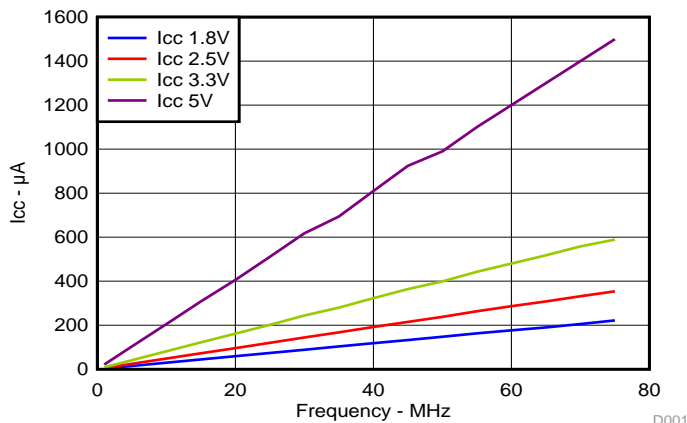


Figure 6. I<sub>CC</sub> vs Frequency

## 11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V<sub>CC</sub> pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended and if there are multiple V<sub>CC</sub> pins then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V<sub>CC</sub> whichever make more sense or is more convenient.

### 12.2 Layout Example

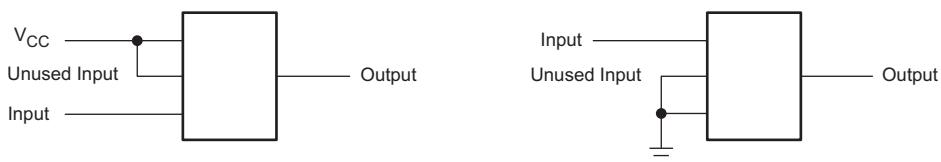


Figure 7. Layout Diagram

## 13 Device and Documentation Support

### 13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.3 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G06DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	(C065 ~ C06F ~ C06R ~ C06T) (C06H ~ C06P ~ C06S)	<a href="#">Samples</a>
SN74LVC1G06DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C06F	<a href="#">Samples</a>
SN74LVC1G06DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C06F	<a href="#">Samples</a>
SN74LVC1G06DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	(C065 ~ C06F ~ C06R) (C06H ~ C06P ~ C06S)	<a href="#">Samples</a>
SN74LVC1G06DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C06F	<a href="#">Samples</a>
SN74LVC1G06DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5 ~ CTF ~ CTK ~ CTR ~ CTT) (CTH ~ CTS)	<a href="#">Samples</a>
SN74LVC1G06DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5 ~ CTF ~ CTK ~ CTR ~ CTT) (CTH ~ CTS)	<a href="#">Samples</a>
SN74LVC1G06DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5 ~ CTF ~ CTK ~ CTR ~ CTT) (CTH ~ CTS)	<a href="#">Samples</a>
SN74LVC1G06DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5 ~ CTF ~ CTK ~ CTR) (CTH ~ CTS)	<a href="#">Samples</a>
SN74LVC1G06DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5 ~ CTF ~ CTK ~ CTR) (CTH ~ CTS)	<a href="#">Samples</a>
SN74LVC1G06DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5 ~ CTF ~ CTK ~ CTR) (CTH ~ CTS)	<a href="#">Samples</a>
SN74LVC1G06DRLR	ACTIVE	SOT-OTHER	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT7 ~ CTR)	<a href="#">Samples</a>
SN74LVC1G06DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G06DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CT	<a href="#">Samples</a>
SN74LVC1G06YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CTN	<a href="#">Samples</a>
SN74LVC1G06YZVR	ACTIVE	DSBGA	YZV	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CT N	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LVC1G06 :**

- Enhanced Product: [SN74LVC1G06-EP](#)

**NOTE: Qualified Version Definitions:**

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



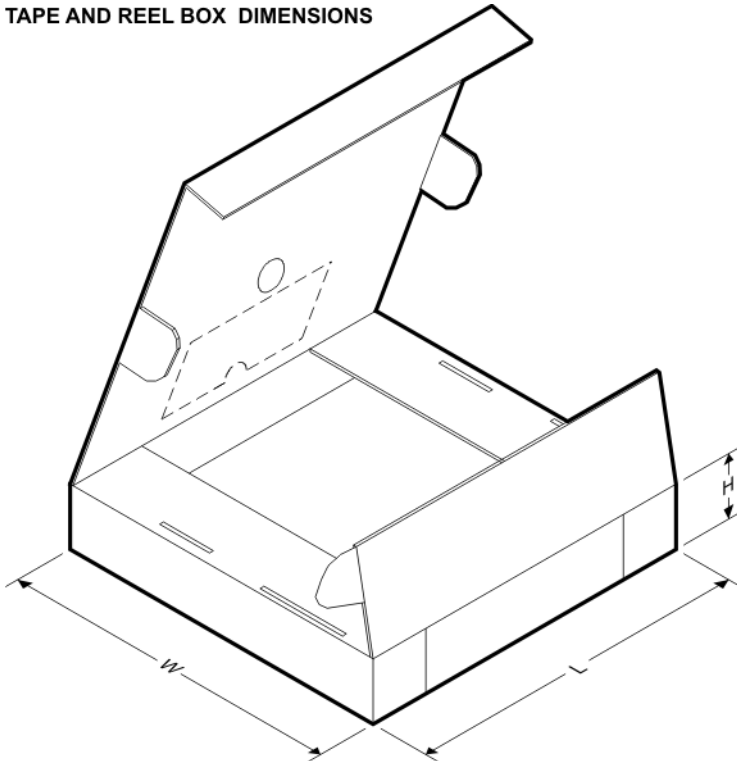
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G06DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G06DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G06DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G06DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G06DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G06DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G06DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G06DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G06DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G06DCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G06DRLR	SOT-OTHER	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G06DRLR	SOT-OTHER	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74LVC1G06DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G06DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G06YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
SN74LVC1G06YZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G06DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LVC1G06DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G06DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G06DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74LVC1G06DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G06DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G06DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G06DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G06DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G06DCKT	SC70	DCK	5	250	205.0	200.0	33.0
SN74LVC1G06DRLR	SOT-OTHER	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G06DRLR	SOT-OTHER	DRL	5	4000	184.0	184.0	19.0
SN74LVC1G06DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G06DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G06YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0
SN74LVC1G06YZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

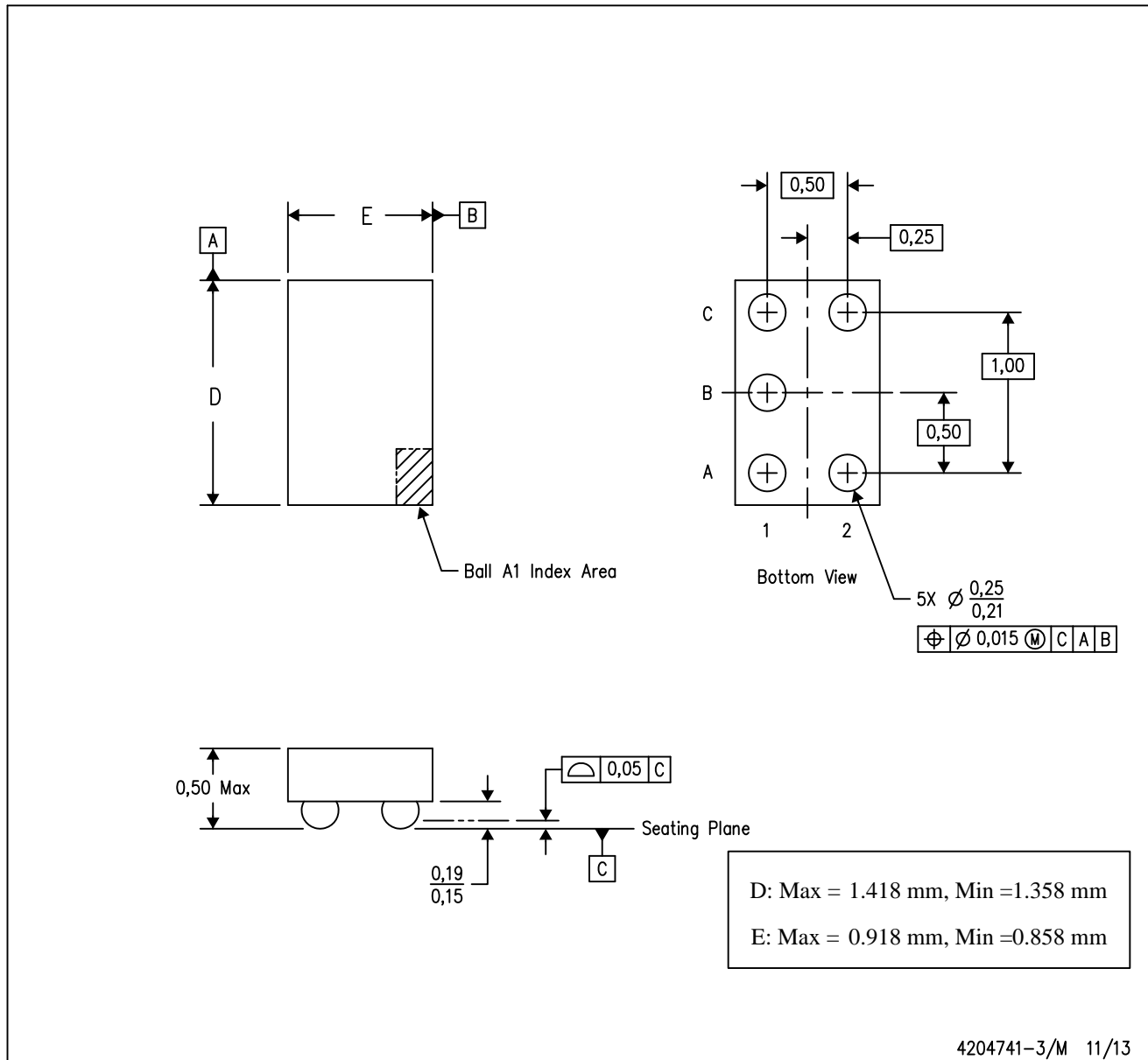
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

YZP (R-XBGA-N5)

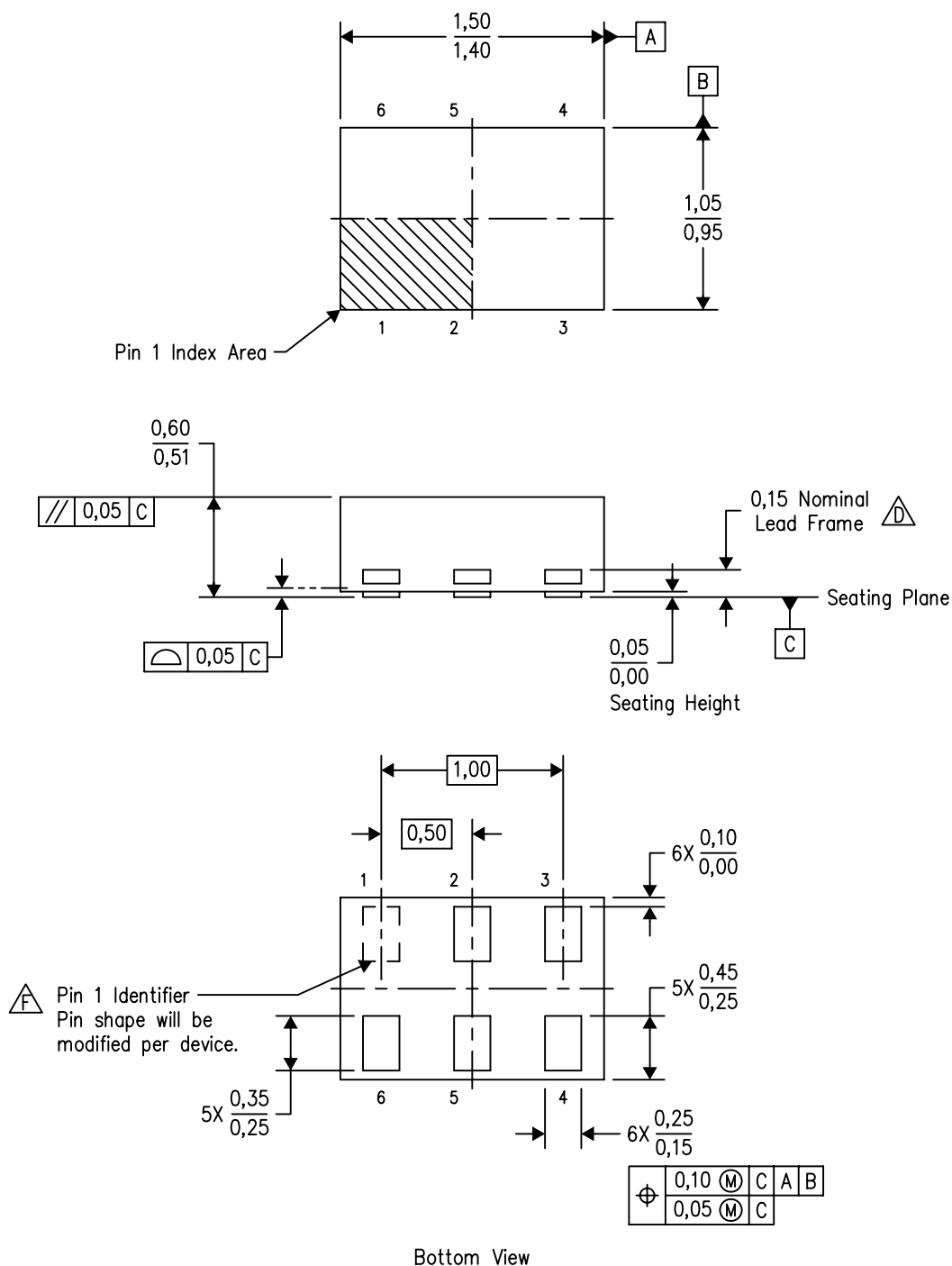
DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

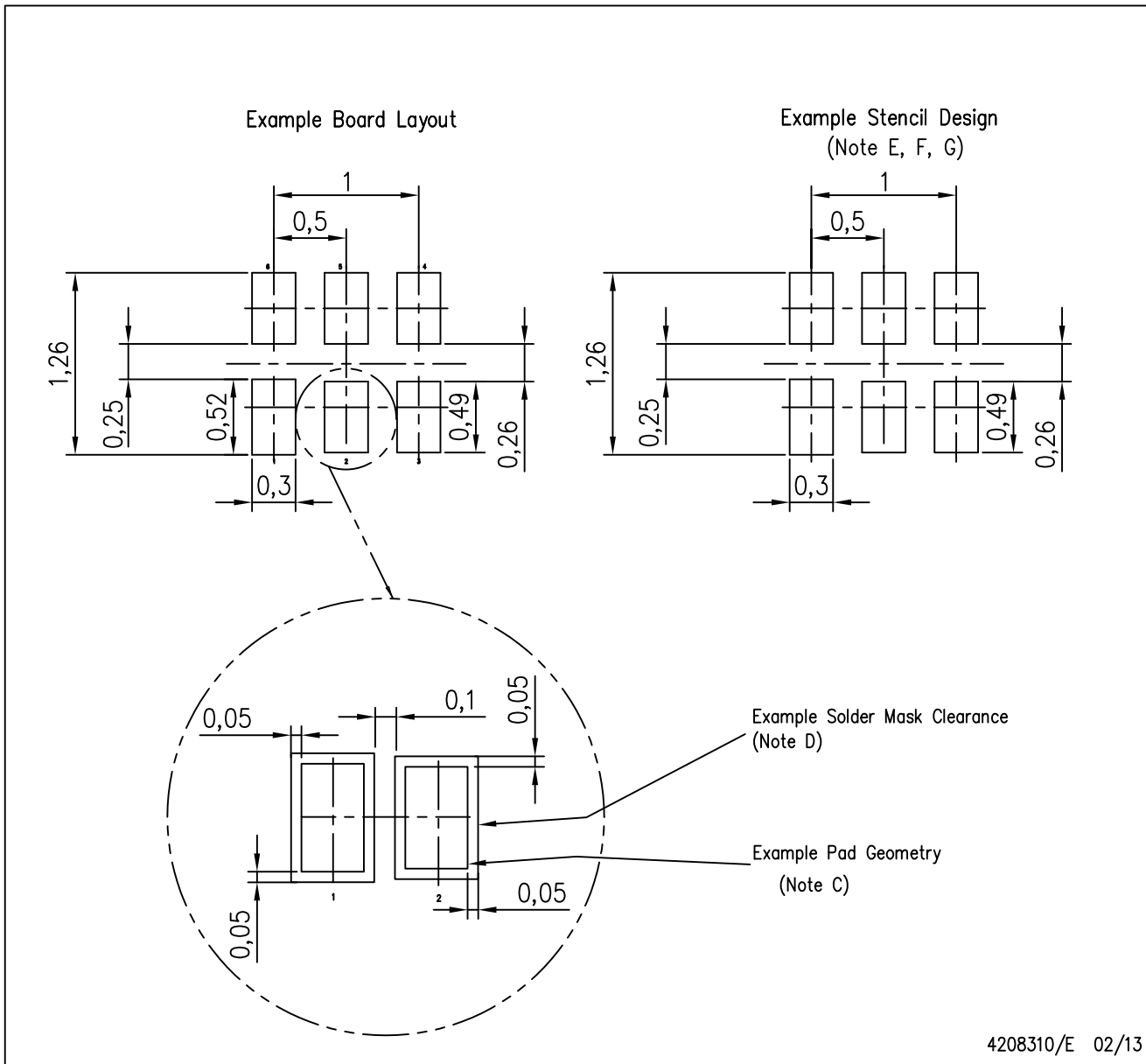


4207181/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  - $\triangle D$  The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
  - E. This package complies to JEDEC MO-287 variation UFAD.
  - $\triangle F$  See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R-PUSON-N6)

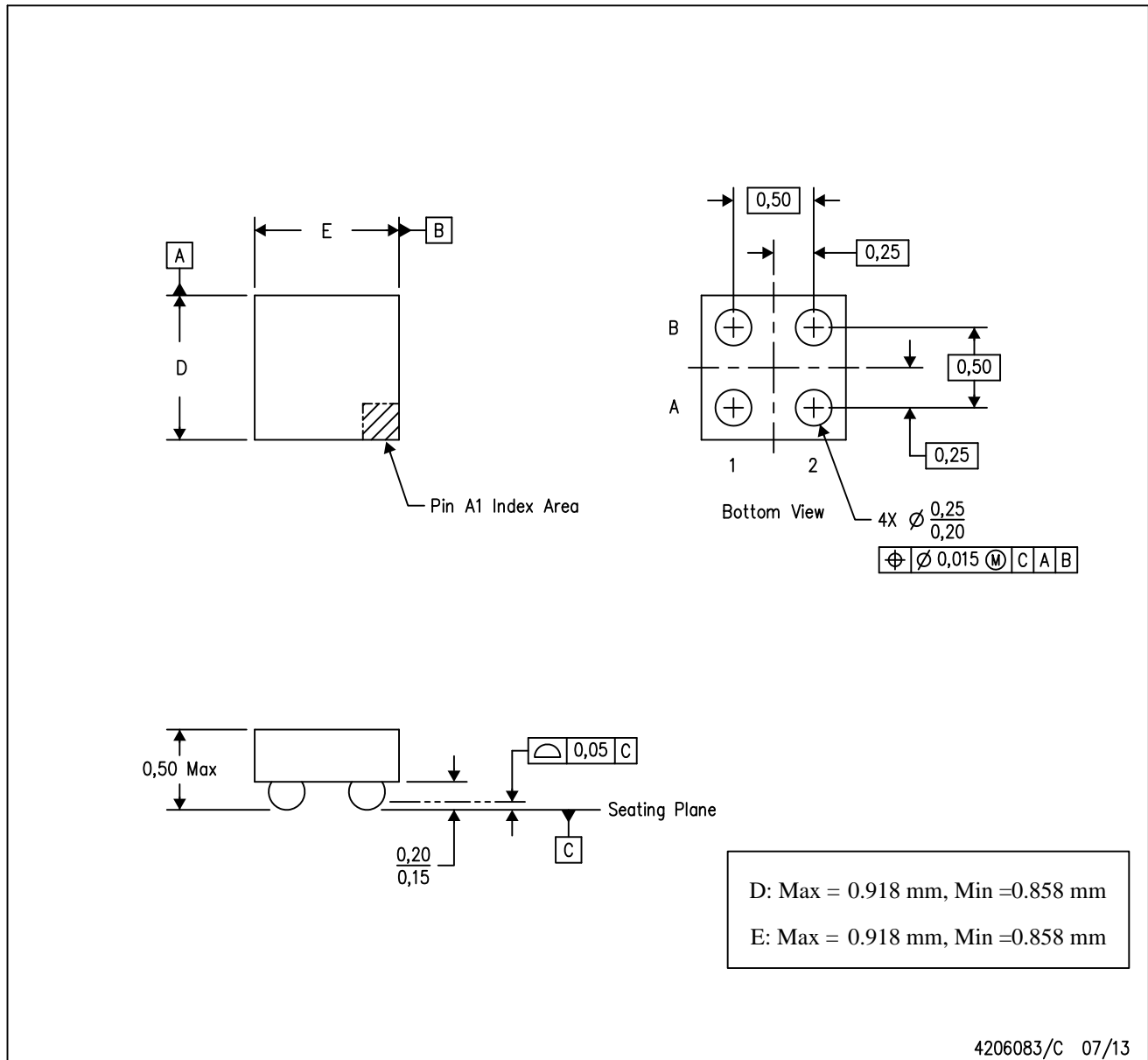
PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

YZV (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.

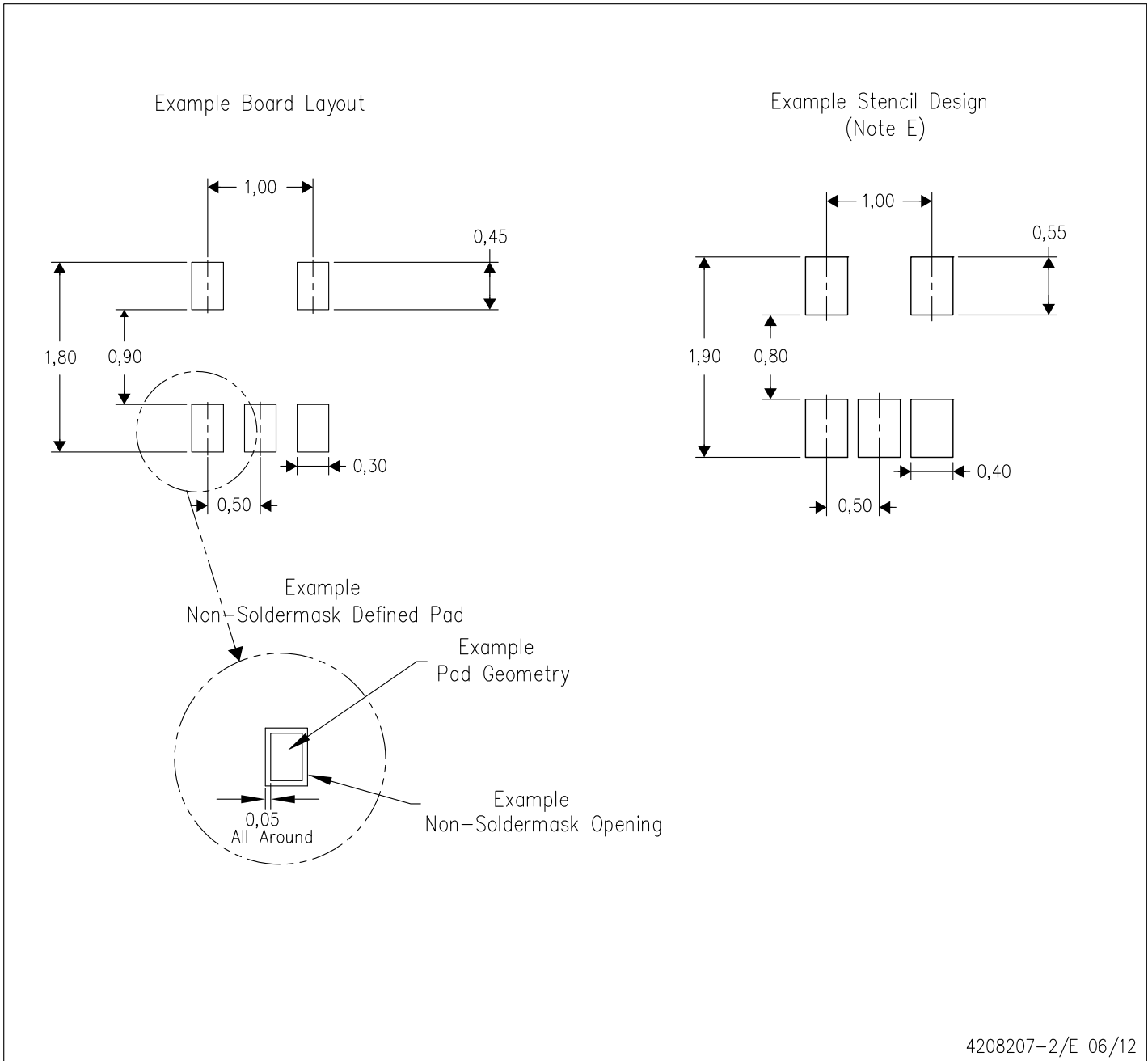
NanoFree is a trademark of Texas Instruments.



4205622-2/D 08/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
  - D. JEDEC package registration is pending.





- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/N 12/14

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE

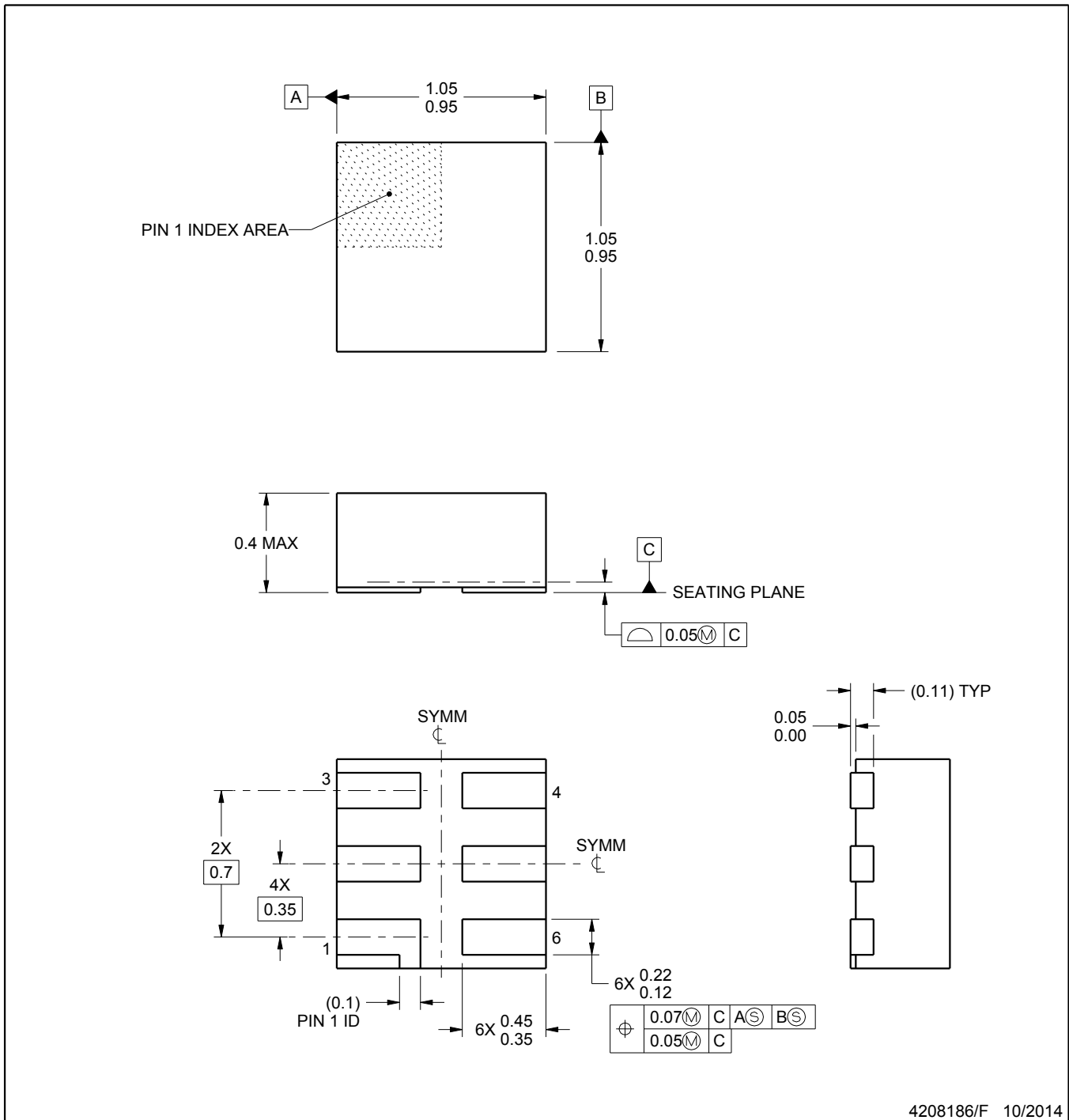


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

# MECHANICAL DATA

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

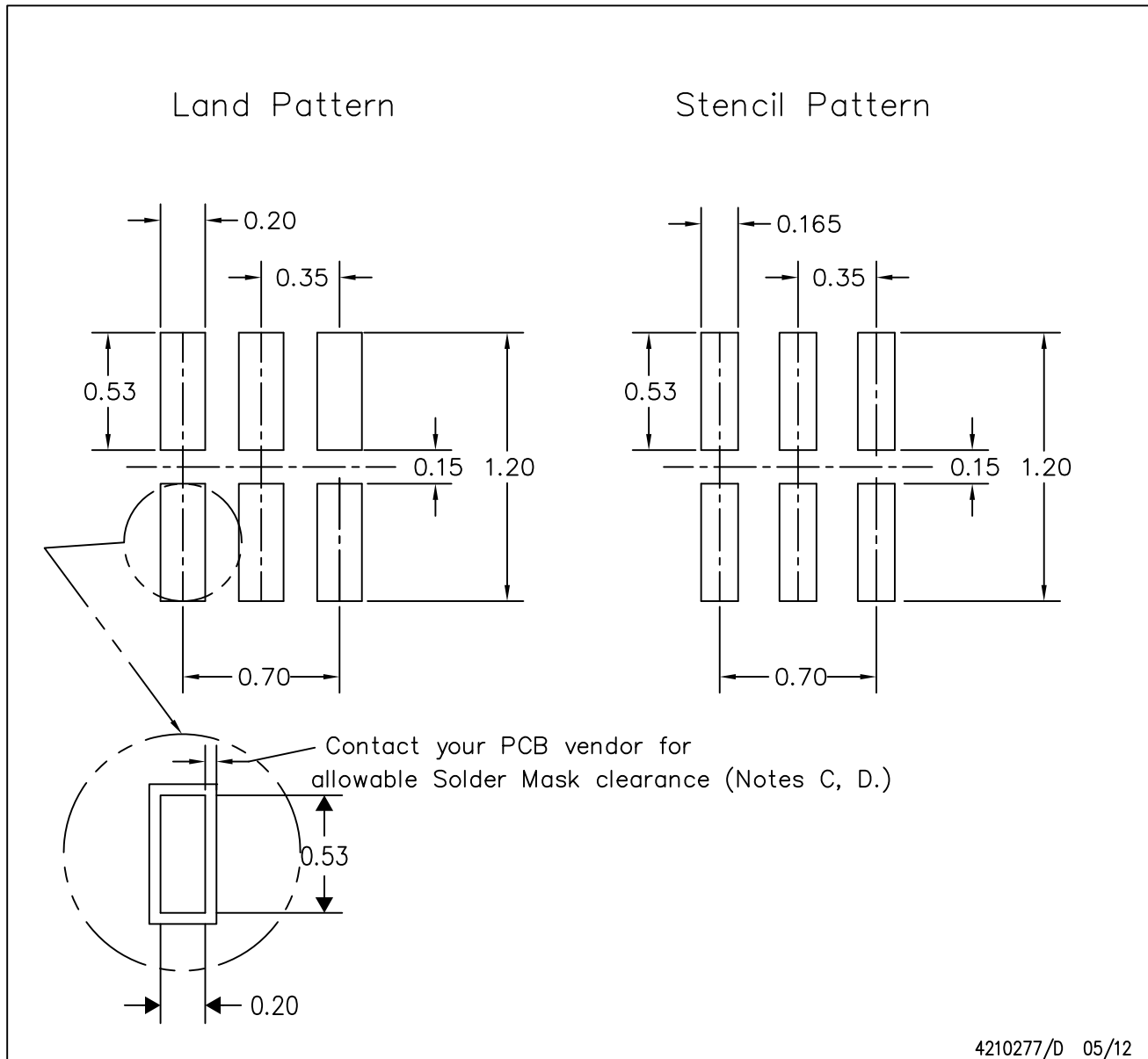


**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4210277/D 05/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
  - E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
  - H. Component placement force should be minimized to prevent excessive paste block deformation.

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