Clock and Timing Solutions

Comprehensive, flexible and easy-to-use clock ICs

Texas Instruments

ti.com/clocks

2017

Accelerate Time-to-Market with Easy-to-Use Clocking Solutions

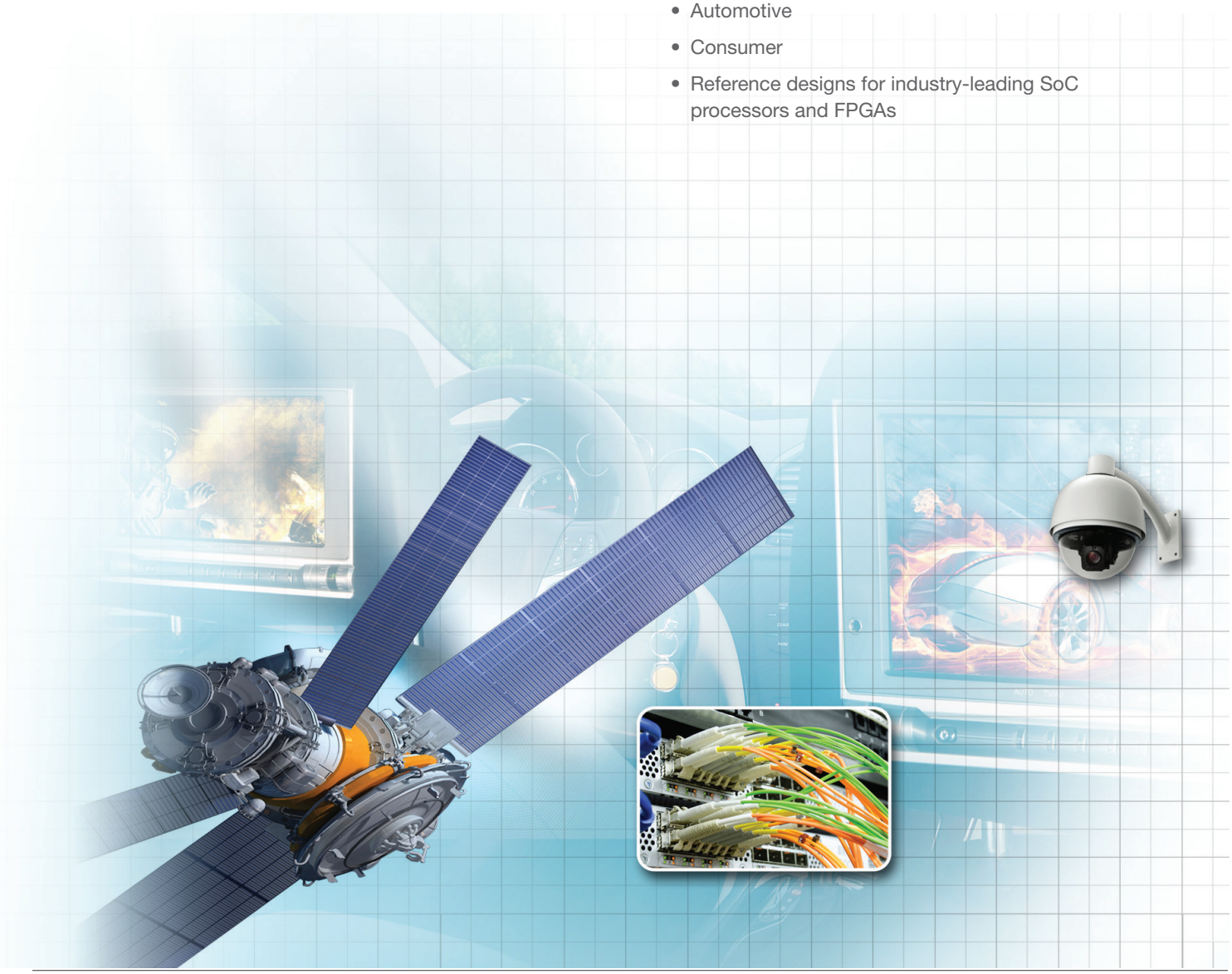
Texas Instruments is the world's #1 supplier of analog semiconductor ICs, and offers a complete clock and timing IC portfolio – from oscillators to clock buffers and generators to jitter attenuators and RF PLLs/synthesizers – targeting a broad spectrum of end-equipment. These easy-to-use, high performance clocking products are supported by a number of innovative, robust online tools that ease design and reduce time-to-market.

Clocking solutions from TI offer:

- Flexible frequency planning
- Universal input and output formats
- Best-in-class jitter and phase noise performance
- Low power consumption
- In-system programming
- Sophisticated clock design tools that automate selection, configuration and simulation of TI clocking devices

Addressing broad applications:

- Wireless communications
  - Base stations
  - Repeaters
  - Satellite communications
- Wired communications
  - Enterprise switches and routers
  - Optical transport networks
  - Servers and storage
- Industrial
  - Industrial automation
  - Test and measurement
  - Medical
  - Video surveillance
  - Energy monitoring
- Automotive
- Consumer
- Reference designs for industry-leading SoC processors and FPGAs



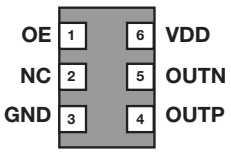
Clock Oscillators

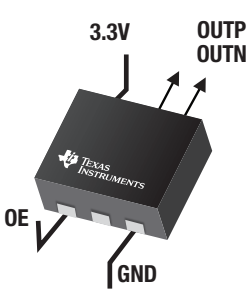
Improve system BER, timing margin, SNR with high performance oscillators from Texas Instruments. TI's high performance differential oscillators offer industry's lowest jitter of 90fs (12 kHz-20 MHz). Offered in the industry standard 7 mm x 5 mm and 5 mm x 3.2 mm package, the LMK6xxx family of oscillators enable high performance and flexible design for the most demanding reference clock requirements.

Portfolio key features

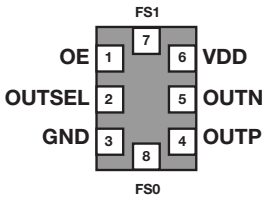
- Typical jitter: 90 fs RMS (12 kHz-20 MHz)
- Total stability: ±25 ppm and ±50 ppm
- LVPECL/LVDS/HCSL formats
- Fmax of 1 GHz
- 3 flavors: fully programmable with EEPROM, pin selectable and fixed frequency versions
- 7 mm x 5 mm and 5 mm x 3.2 mm
- 3.3 V
- PSRR: -70 dBc, robust supply noise immunity
- Best-in-class resistance to vibrations

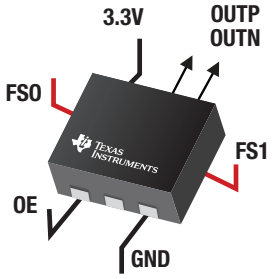
Fixed Freq
LMK61xx-FFFMFF
LMK62xx-FFFMFF
LMK60xx-FFFMFF



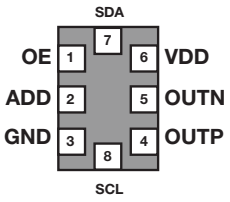


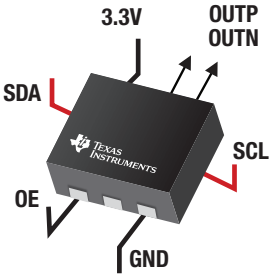
Pin mode
LMK61PDxxx





Programmable XO
LMK61Ex





Featured Clock Oscillators

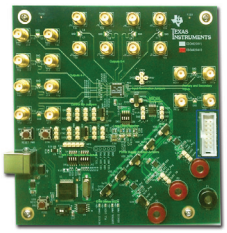
						End-equipment		
Part Number	Special Features	Max Output Frequency (MHz)	Output Format	Jitter (ps)	Package Size (mm x mm)	Wireless	Wired/Networking	Industrial
LMK61E2	Programmable with EEPROM	1000	HCSL, LVDS, LVPECL	0.1	7 x 5	✔	✔	✔
LMK61PD0A2	Pin Select	312.5	HCSL, LVDS, LVPECL	0.1	7 x 5	✔	✔	✔
LMK61E0M	Programmable with EEPROM	200	LVCMOS	0.5	7 x 5		✔	✔
LMK61E2-100M	Fixed Frequency	100	LVPECL	0.1	7 x 5	✔	✔	✔
LMK61E2-312M	Fixed Frequency	312.5	LVPECL	0.1	7 x 5	✔	✔	✔
LMK61A2-125M	Fixed Frequency	125	LVDS	0.1	7 x 5	✔	✔	✔
LMK61A2-156M	Fixed Frequency	156.25	LVDS	0.1	7 x 5		✔	✔
LMK61A2-312M	Fixed Frequency	312.5	LVDS	0.1	7 x 5	✔	✔	✔
LMK62E2-156M	Fixed Frequency	156.25	LVPECL	0.15	5 x 3.2		✔	✔
LMK60E0-156M	Fixed Frequency	156.25	LVPECL	0.15	7 x 5		✔	✔

Clock Generators

Reduce the clutter of crystals and oscillators, simplify your design and reduce your bill-of-materials (BOM) with clock generators from Texas Instruments. TI's clock generator portfolio, ranging from low power to ultra-low jitter (as low as 150 fs RMS), can consolidate multiple crystals in consumer and industrial applications as well as telecom/datacom applications.

Portfolio key features

- Integrated PLL and VCO for smaller BOM
- Integrated LDOs for supply noise rejection
- Multiple clock outputs at very low jitter
- Fractional dividers for ultimate flexibility
- Integrated clock distribution with programmable dividers
- Programmable output formats (CMOS and diff.)
- Spread spectrum clocking to reduce EMI



CDCM6208V1EVM:
Evaluation module for 8-output clock generator

Featured Clock Generators

						End-equipment				
Device	**Description**	**Input:Output**	**Output Type**	**Jitter**	**Programmability**	**Wireless**	**Wired/Networking**	**Industrial**	**Automotive**	**Consumer**
LMK03328	Ultra low jitter, 8 output clock generator with Integrated EEPROM	2:8	CML, LVPECL, LVDS, HCSL, LVCMOS	0.1ps RMS	I²C,EEPROM, pin	✔	✔	✔		
CDCM6208	Any frequency, 2 input, 8 output with integer and fractional dividers	2:8	CML, LVPECL, LVDS, HCSL, LVCMOS	0.265 ps RMS**	SPI, I²C, pin	✔	✔	✔		
LMK03806	1 input, 14 outputs, ultra-low jitter with integer dividers	1:14	LVDS, LVPECL, LVCMOS	0.15 ps RMS**	µWire (SPI)	✔	✔	✔		
CDCE62005	3 input, 5 output with integrated dual VCOs	3:5	LVPECL, LVDS, LVCMOS	0.35 ps RMS**	SPI, EEPROM	✔	✔	✔		
CDCM6100x	1 input, 1-4 output, crystal oscillator replacement	1:1 (CDCM61001) 1:2 (CDCM61002) 1:4 (CDCM61004)	LVPECL, LVDS, LVCMOS	0.5 ps RMS**	Pin	✔	✔	✔		
CDCM9102	Low jitter, 2 channel, 100 MHz PCIe Gen-3, Gen-2, Gen-1	1:2	LVPECL, LVDS, LVCMOS	0.5 ps RMS**	Pin		✔	✔		✔
CDCE(L)913	1 PLL, integrated VCXO, spread spectrum clocking, 1.8 V/2.5 V/3.3 V outputs	1:3*	LVCMOS	60 ps peak-to-peak period	I²C, EEPROM, pin	✔	✔	✔		✔
CDCE(L)949	4 PLL, integrated VCXO, spread spectrum clocking, 1.8 V/2.5 V/3.3 V outputs	1:9*	LVCMOS	60 ps peak-to-peak period	I²C, EEPROM, pin	✔	✔	✔	✔	✔
CDCE706	3 PLL, spread spectrum clocking, ultra flexible output switching matrix	1:6	LVCMOS	65 ps cycle-to-cycle	SMBus, EEPROM	✔	✔	✔		✔
CDCS501/2/3	Spread spectrum clock generator	1:1	LVCMOS	110 ps cycle-to-cycle	Pin				✔***	✔
CDCE6214	Low power, high performance, easy to use general purpose clock generator with EEPROM	2:4	LVDS, LVPECL, HCSL, LVCMOS	0.7ps RMS	I²C, Pin, EEPROM	✔	✔	✔	✔	✔

* 2 PLL/5 outputs and 3 PLL/7 outputs also available
** as measured from 12 kHz to 20 MHz
*** Available for CDCS503-Q1

*Products listed in **teal** are available 3Q 2017.*

Clock Distribution/Fanout Buffers

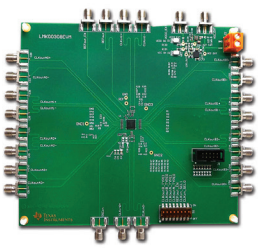
Simplify your clock tree designs with pin-programmable universal clock buffers that support any input and any output format. TI's unique family of clock buffers and distributors offers maximum design flexibility with no compromise on performance and includes advanced features such as dividers and delays, addressing a broad range of communications, industrial and consumer applications.

Portfolio key features

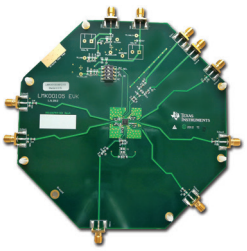
- Lowest additive jitter to maintain performance in clock tree
- GHz range input and output clock frequency
- Integrated LDOs for improved supply noise rejection
- Multiple output banks that can be configured independently
- Programmable divider and output formats for higher flexibility
- Adjustable analog delay to accommodate board traces

Clock Distribution/ Fan-out Buffers/ Zero Delay Buffer

						End-Equipment					
Device	Description	Input:Output	Input Type	Output Type	Max Frequency (MHz)	Wireless	Wired/Networking	Industrial	Automotive	Consumer	Computing
LMK0030x	Ultra-low jitter configurable differential buffer/level translator, crystal oscillator	3:4 (LMK00304) 3:6 (LMK00306) 3:8 (LMK00308) 3:10 (LMK00301)	Differential, single ended, crystal	LVPECL, LVDS, HCSL + 1 LVCMOS	3100	✔	✔	✔			
LMK033xx	Ultra-low jitter PCIe Gen 1/2/3 HCSL buffers	3:4(LMK00334) and 3:8(LMK00338)	Differential, single ended, crystal	HCSL	400	✔	✔	✔			✔
CDCLVPxxxx	LVPECL buffer	from 1:2 to 2:16	Differential	LVPECL	2000 / 3500	✔	✔	✔			
CDCLVDxxxx	LVDS buffer	from 2:4 to 2:16	Differential	LVDS	800 / 1100	✔	✔	✔			
LMK0010x	Ultra-low jitter configurable LVCMOS buffer/level translator, crystal oscillator	3:5 (LMK00105) 3:10 (LMK00101)	Differential, single ended, crystal	LVCMOS	200	✔	✔	✔		✔	
CDCLVCxxxx	LVCMOS buffer	from 1:2 to 1:12	LVCMOS	LVCMOS	250	✔	✔	✔		✔	
CDCM1802	Programmable divider	1:2	Differential	LVPECL, LVCMOS	800 LVPECL 200 LVCMOS	✔	✔	✔			
CDCM1804	Programmable divider	1:4	Differential	LVPECL, LVCMOS	800 LVPECL 200 LVCMOS	✔	✔	✔			
LMK0180x	Dual clock divider buffer, digital and analog delay programming	from 2:14 to 2:20	Differential, single ended	LVPECL, LVDS, LVCMOS	3100	✔	✔	✔			
CDCFR83A	3.3 V zero delay buffer phase aligner	1:1	Differential	Differential	533		✔	✔		✔	✔
CDCVF2505	3.3 V zero delay buffer	1:4	Single ended	LVCMOS	200		✔	✔	✔	✔	✔
CDCVF2510A	3.3 V zero delay buffer	1:10	Single ended	LVCMOS	175		✔	✔		✔	✔
CDCVF85x	2.5 V zero delay buffer	1:4 (CDCVF855) 1:10 (CDCVF857)	Differential	Differential	220		✔	✔		✔	✔
CDCU(A)877	1.8 V zero delay buffer	1:10	Differential	Differential	400 / 410		✔	✔		✔	✔



LMK00308EVM:
Evaluation module for 3 GHz, 8-output clock buffer/level translator



LMK00105BEVAL:
Evaluation module for 5-output fanout buffer/level translator

Clock Jitter Cleaners

Get the most out of your system with the industry's cleanest clocks. TI's clock jitter cleaners deliver the lowest phase noise and a wide range of output frequencies.

Portfolio key features

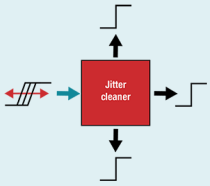
- Industry's best phase noise performance
- Single or dual loop PLL to reduce BOM
- Frequency hold-over and redundancy
- Programmable divider and output formats for higher flexibility

Featured Clock Jitter Cleaners

					End-equipment				
Device	Description	Jitter (fs)*	Max Output Frequency (MHz)	Number of Outputs	Wireless	Wired/Networking	Industrial	Automotive	Consumer
LMK04610	Dual PLL, ultra-low phase noise and ultra-low power, JESD204B compliant, integrated loop filters and LDOs, 2 selectable inputs, 10 outputs, frequency holdover mode, programmable delay	65	2000	10	✔	✔	✔		
LMK04616	Dual PLL, ultra-low phase noise and ultra-low power, JESD204B compliant, integrated loop filters and LDOs, 4 selectable inputs, 16 outputs, frequency holdover mode, programmable delay	65	2000	16	✔		✔		
CDCM7005	Low phase noise with frequency holdover, available in BGA package	230	2200	5	✔				
LMK0480x	Dual PLL, ultra-low phase noise, 2 selectable inputs, 14 outputs, frequency holdover mode, programmable delay	100	3072	14	✔		✔		
LMK0482x	Dual PLL, lowest phase noise, JESD204B compliant, frequency holdover mode, programmable delay	88	3100	15	✔		✔		
LMK04832**	3.2 GHz max. output frequency, Dual PLL, lowest phase noise and noise floor, JESD204B compliant, frequency holdover mode, programmable delay	80	3200	15	✔		✔		
LMK04906	Dual PLL, ultra-low phase noise, 3 selectable inputs, 7 outputs, frequency holdover mode, programmable delay	100	2600	7		✔	✔		
LMK04816	Dual PLL, ultra-low phase noise, 3 selectable inputs, 13 outputs, frequency holdover mode, programmable delay	100	2600	13	✔	✔	✔		

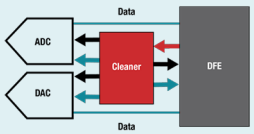
* As measured between 12 kHz to 20 MHz
** Sample available in March 2017

Industry's best performance



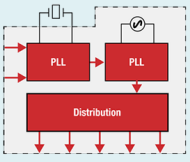
- Ultra low jitter: 65 fs typ 12 K-10 M
- Ultra low inband phase noise through leading BiCMOS technology

JESD204B made easy



- Industry's first and most popular JESD204B jitter cleaner family LMK0482x
- Supports JESD204B and non-JESD204B applications with a single device
- Full SYSREF support reduces SoC complexity and cost

PLLATINUM™ dual loop PLL



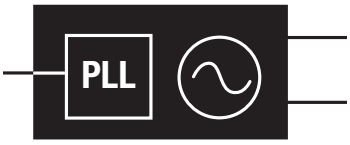
- PLLATINUM dual phase locked loop (PLL) concept reduces cost and improves performance
- Generates frequencies up to 3 GHz with an integrated high performance VCO

LMX25xx RF Synthesizer Family

The LMX25xx family of RF synthesizers integrates low noise VCOs along with low noise PLLs. The low power LMX2531 and LMX2571 enables energy efficient and mobile solutions, while still having best-in-class performance to meet industry standards. The high performance LMX2541, LMX2581, LMX2582, and LMX2592 covers up to 9.8GHz at the best noise figures in the industry to enable high performance solutions.

Portfolio key features

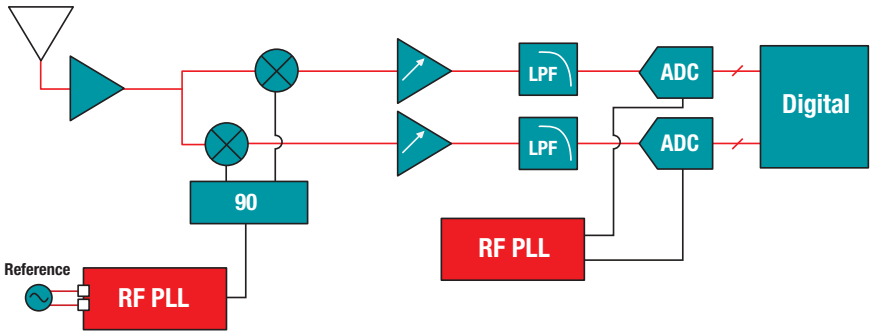
- Industry's highest performance, MC-GSM, compliant, integrated VCOs
- Industry's best PLL figure of merit for noise
- Integrated jitter <60 fsec for clocking high performance data converters



High performance synthesizer family with integrated VCO

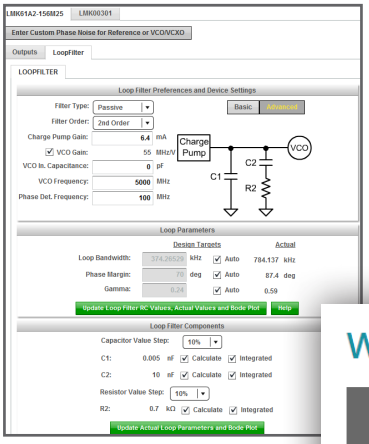
Device	Output Frequency(Min) (MHz)	Output Frequency(Max) (MHz)	VCO Phase Noise Normalized to 1 GHz at 100 kHz Offset (dBc/Hz)	Normalized PLL Phase Noise (dBc/Hz)	1/f Noise (10 kHz offset at 1 GHz carrier) (dBc/Hz)	Current Consumption (mA)	PFD frequency (MHz)
LMX2592	20	9800	-129	-231	-126	250	200
LMX2582	20	5500	-129	-231	-126	250	200
LMX2571	10	1344	-115	-231	-124	39	130
LMX2581E	50	3800	-121	-229	-121	178	200
LMX2541	32	4000	-120	-226	-125	120	104
LMX2531	553	3132	-126	-212	-104	34	32
LMX2522	1619.62	1649.62	-117			17	
LMX2512	954.42	1077.57	-117			17	

Frequent use case for RF PLLs and Synthesizers

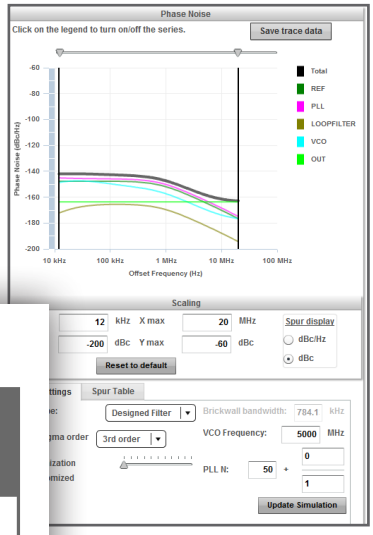


WEBENCH® Clock Architect

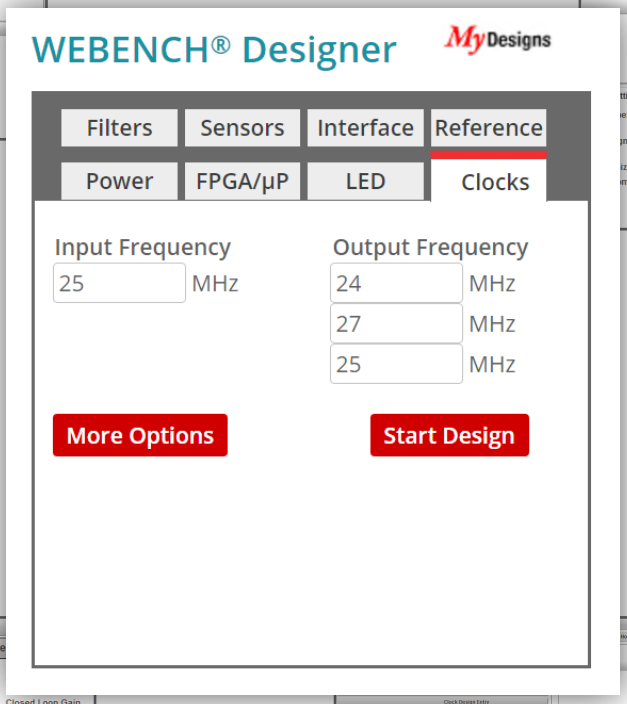
Complete, optimized clock tree solutions in minutes

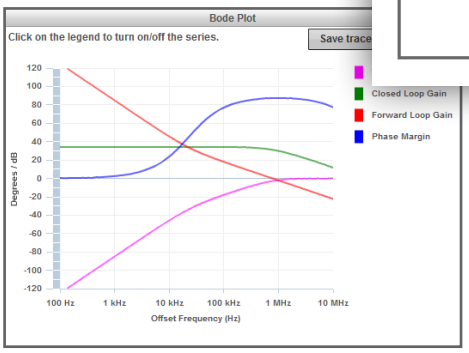


Loop Filter Design screenshot

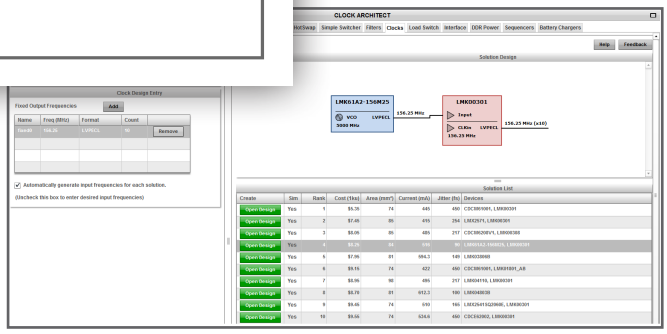


Phase Noise Plot





Bode Plot



Main Clock Architect screenshot

Get more information on TI's family of clocking products at **ti.com/clocks**

E2E Clocks & Timing Forum
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TI E2E™ Community

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