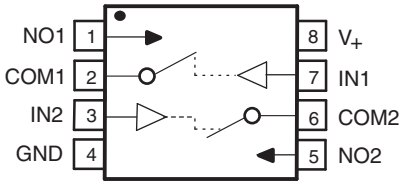
DUAL-CHANNEL 10-Ω SPST ANALOG SWITCH

Check for Samples: TS5A2066

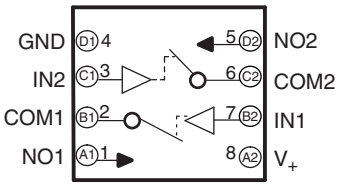
FEATURES

- **Low ON-State Resistance (10 Ω)**
- **Control Inputs Are 5-V Tolerant**
- **Low Charge Injection**
- **Excellent ON-State Resistance Matching**
- **Low Total Harmonic Distortion (THD)**
- **1.65-V to 5.5-V Single-Supply Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

DCT OR DCU PACKAGE
(TOP VIEW)



YZP PACKAGE
(BOTTOM VIEW)



APPLICATIONS

- **Sample-and-Hold Circuits**
- **Battery-Powered Equipment**
- **Audio and Video Signal Routing**
- **Communication Circuits**
- **Cell Phones**
- **Low-Voltage Data-Acquisition Systems**
- **PDAs**

DESCRIPTION/ORDERING INFORMATION

The TS5A2066 is a dual single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals, and signals up to V_+ can be transmitted in either direction.

Table 1. Summary of Characteristics(1)

Configuration	Dual Single Pole Single Throw (2 × SPST)
Number of channels	2
ON-state resistance (r_{on})	7.5 Ω
ON-state resistance match (Δr_{on})	0.4 Ω
ON-state resistance flatness ($r_{on(flat)}$)	3.5 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	5.8 ns/3.6 ns
Charge injection (Q_C)	1 pC
Bandwidth (BW)	400 MHz
OFF isolation (O_{ISO})	–68 dB
Crosstalk (X_{TALK})	–66 dB
Total harmonic distortion (THD)	0.01%
Leakage current ($I_{COM(OFF)}/(I_{NC(OFF)}$	±50 nA
Power-supply current (I_+)	0.1 μA
Package options	8-pin DSBGA, SSOP, or VSSOP

(1) V_+ = 5 V and T_A = 25°C

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	TS5A2066YZPR	_ _ _J4_
	SSOP – DCT	Reel of 3000	TS5A2066DCTR	JAG_ _ _
	VSSOP – DCU	Reel of 3000	TS5A2066DCUR	JAG_

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DCT: The actual top-side marking has three additional characters that designate the year, month, and wafer fab/assembly site.
DCU: The actual top-side marking has one additional character that designates the wafer fab/assembly site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

FUNCTION TABLE

IN	NO TO COM, COM TO NO
L	OFF
H	ON

Absolute Minimum and Maximum Ratings(1) (2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(3)		–0.5	6.5	V
V_{NO} V_{COM}	Analog voltage range(3) (4) (5)		–0.5	V_+ + 0.5	V
I_K	Analog port diode current	V_{NO}, V_{COM} < 0 or V_{NO}, V_{COM} > V_+	–50	50	mA
I_{NO} I_{COM}	On-state switch current	V_{NO}, V_{COM} = 0 to V_+	–50	50	mA
V_I	Digital input voltage range(3) (4)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100	100	mA
θ_{JA}	Package thermal impedance(6)	DCT package		220	°C/W
		DCU package		227	
		YZP package		102	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Characteristics for 5-V Supply(1)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}					0		V_+	V
ON-state resistance	r_{on}	0 ≤ V_{NO} ≤ V_+, I_{COM} = –32 mA,	Switch ON, See Figure 13	25°C	4.5 V		7.5	10	Ω
				Full				15	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 3.15 V, I_{COM} = –32 mA,	Switch ON, SeeFigure 13	25°C	4.5 V		0.4	1	Ω
				Full				3	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NO} ≤ V_+, I_{COM} = –32 mA,	Switch ON, See Figure 13	25°C	4.5 V	2	3.5	5	Ω
				Full		4		8	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 1 V, V_{COM} = 4.5 V, or V_{NO} = 4.5 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	5.5 V	–30	–10	30	nA
				Full		–40		40	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NO} = 4.5 V, or V_{COM} = 4.5 V, V_{NO} = 1 V,	Switch OFF, See Figure 14	25°C	5.5 V	–50	–8	50	nA
				Full		–50		50	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 4.5 V, V_{COM} = Open	Switch ON, See Figure 15	25°C	5.5 V	–40	–12	40	nA
				Full		–4		40	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 4.5 V, V_{NO} = Open,	Switch ON, See Figure 15	25°C	5.5 V	–70	–30	70	nA
				Full		–70		70	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		V_+ × 0.7		5.5	V
Input logic low	V_{IL}			Full		0		V_+ × 0.3	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	5.5 V	–0.1	0.05	0.1	μA
				Full		–1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 5-V Supply (1) (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	5 V	4.4	5.2	5.8	ns
				Full	4.5 V to 5.5 V	3.4		6.1	
Turn-off time	t_{OFF}	V_{COM} = 3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	5 V	1.7	2.6	3.6	ns
				Full	4.5 V to 5.5 V	1.3		4.2	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 21	25°C	5 V		1		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 16	25°C	5 V		5.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_+ or GND, Switch OFF,	See Figure 16	25°C	5 V		5.5		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_+ or GND, Switch ON,	See Figure 16	25°C	5 V		13.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	5 V		13.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	5 V		2.5		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	5 V		300		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	5 V		–68		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	5 V		–66		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 22	25°C	5 V		0.01		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	5.5 V		0.1	1	μA
				Full				5	

Electrical Characteristics for 3.3-V Supply(1)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}					0		V_+	V
ON-state resistance	r_{on}	0 ≤ V_{NO} ≤ V_+, I_{COM} = –24 mA,	Switch ON, See Figure 13	25°C	3 V	10	12	15	Ω
				Full		12		20	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 2.1 V, I_{COM} = –24 mA,	Switch ON, See Figure 13	25°C	3 V	0.04	0.5	1.5	Ω
				Full		0.01		3.5	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NO} ≤ V_+, I_{COM} = –24 mA,	Switch ON, See Figure 13	25°C	3 V	6	7	8	Ω
				Full		9		12	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 1 V, V_{COM} = 3 V, or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	–30	–6	30	nA
				Full		–40		40	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NO} = 3 V, or V_{COM} = 3 V, V_{NO} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	–50	–7	50	nA
				Full		–50		50	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–40	–7	40	nA
				Full		–40		40	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 3 V, V_{NO} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–70	–20	70	nA
				Full		–70		70	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		V_+ × 0.7		5.5	V
Input logic low	V_{IL}			Full		0		V_+ × 0.3	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 3.3-V Supply (1) (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	4.9	5.6	6.4	ns
				Full	3 V to 3.6 V	4.3		7.1	
Turn-off time	t_{OFF}	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	2	2.7	3.7	ns
				Full	3 V to 3.6 V	1.3		4.7	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 21	25°C	3.3 V		0.5		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		5.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_+ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		6		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_+ or GND, Switch ON,	See Figure 16	25°C	3.3 V		14		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	3.3 V		14		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	3.3 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	3.3 V		300		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	3.3 V		–68		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	3.3 V		–66		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 22	25°C	3.3 V		0.065		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V		0.1	1	μA
				Full				5	

Electrical Characteristics for 2.5-V Supply(1)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}					0		V_+	V
ON-state resistance	r_{on}	0 ≤ V_{NO} ≤ V_+, I_{COM} = –8 mA,	Switch ON, See Figure 13	25°C	2.3 V	20	22		Ω
				Full				30	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 1.6 V, I_{COM} = –8 mA,	Switch ON, SeeFigure 13	25°C	2.3 V	0.04	0.5	1.5	Ω
				Full		0.02		5	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NO} ≤ V_+, I_{COM} = –8 mA,	Switch ON, See Figure 13	25°C	2.3 V	12	16	18	Ω
				Full		15		25	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0.5 V, V_{COM} = 2.2 V, or V_{NO} = 2.2 V, V_{COM} = 0.5 V,	Switch OFF, See Figure 14	25°C	2.7 V	–30	–5.5	30	nA
				Full		–40		40	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0.5 V, V_{NO} = 2.2 V, or V_{COM} = 2.2 V, V_{NO} = 0.5 V,	Switch OFF, See Figure 14	25°C	2.7 V	–50	–7.5	50	nA
				Full		–50		50	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0.5 V, V_{COM} = Open, or V_{NO} = 2.2 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–40	–5	40	nA
				Full		–40		40	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 0.5 V, V_{NO} = Open, or V_{COM} = 2.2 V, V_{NO} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–70	–12	70	nA
				Full		–70		70	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		V_+ × 0.7		5.5	V
Input logic low	V_{IL}			Full		0		V_+ × 0.3	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 2.5-V Supply (1) (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 1.5 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	2.5 V	5.7	6.4	8.1	ns
				Full	2.3 V to 2.7 V	4.4		8.5	
Turn-off time	t_{OFF}	V_{COM} = 1.5 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	2.5 V	2.1	3.1	4.3	ns
				Full	2.3 V to 2.7 V	1.8		4.8	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 20	25°C	2.5 V		0.5		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		6		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_+ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		6		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_+ or GND, Switch ON,	See Figure 16	25°C	2.5 V		14		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	2.5 V		14		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	2.5 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	2.5 V		300		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	2.5 V		–68		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	2.5 V		–66		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 22	25°C	2.5 V		0.35		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.7 V		0.1	1	μA
				Full				5	

Electrical Characteristics for 1.8-V Supply(1)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch								
Analog signal range	V_{COM}, V_{NO}				0		V_+	V
ON-state resistance	r_{on}	0 ≤ V_{NO} ≤ V_+, I_{COM} = –4 mA, Switch ON, See Figure 13	25°C	1.65 V	80	85		Ω
			Full		90		120	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 1.15 V, I_{COM} = –4 mA, Switch ON, See Figure 13	25°C	1.65 V	0	0.9	2	Ω
			Full		0		6	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NO} ≤ V_+, I_{COM} = –4 mA, Switch ON, See Figure 13	25°C	1.65 V	70	75	85	Ω
			Full		85		100	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0.3 V, V_{COM} = 1.65 V, or V_{NO} = 1.65 V, V_{COM} = 0.3 V, Switch OFF, See Figure 14	25°C	1.95 V	–30	–6	30	nA
			Full		–40		40	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 0.3 V, V_{NO} = 1.65 V, or V_{COM} = 1.65 V, V_{NO} = 0.3 V, Switch OFF, See Figure 14	25°C	1.95 V	–50	–7	50	nA
			Full		–50		50	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0.3 V, V_{COM} = Open, or V_{NO} = 1.65 V, V_{COM} = Open, Switch ON, See Figure 15	25°C	1.95 V	–40	7	40	nA
			Full		–40		40	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 0.3 V, V_{NO} = Open, or V_{COM} = 1.65 V, V_{NO} = Open, Switch ON, See Figure 15	25°C	1.95 V	–70	–8.5	70	nA
			Full		–70		70	
Digital Control Input (IN)								
Input logic high	V_{IH}		Full		V_+ × 0.65		5.5	V
Input logic low	V_{IL}		Full		0		V_+ × 0.35	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0	25°C	1.95 V	–0.1	0.05	0.1	µA
			Full		–1		1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 1.8-V Supply (1) (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = 1.3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	1.8 V	9.3	10.4	11.5	ns
				Full	1.65 V to 1.95 V	6.8		12.9	
Turn-off time	t_{OFF}	V_{COM} = 1.3 V, R_L = 300 Ω,	C_L = 35 pF, See Figure 17	25°C	1.8 V	3.3	4.3	5.2	ns
				Full	1.65 V to 1.95 V	2.4		6.5	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 0.1 nF, See Figure 21	25°C	1.8 V		0.5		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		6		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_+ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		6		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_+ or GND, Switch ON,	See Figure 16	25°C	1.8 V		14.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 16	25°C	1.8 V		14.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 16	25°C	1.8 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 18	25°C	1.8 V		293		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 10 MHz,	Switch OFF, See Figure 19	25°C	1.8 V		–68		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 10 MHz,	Switch ON, See Figure 20	25°C	1.8 V		–66		dB
Total harmonic distortion	THD	R_L = 10 kΩ, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 22	25°C	1.8 V		2.7		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	1.95 V		0.1	1	µA
				Full				5	

TYPICAL PERFORMANCE

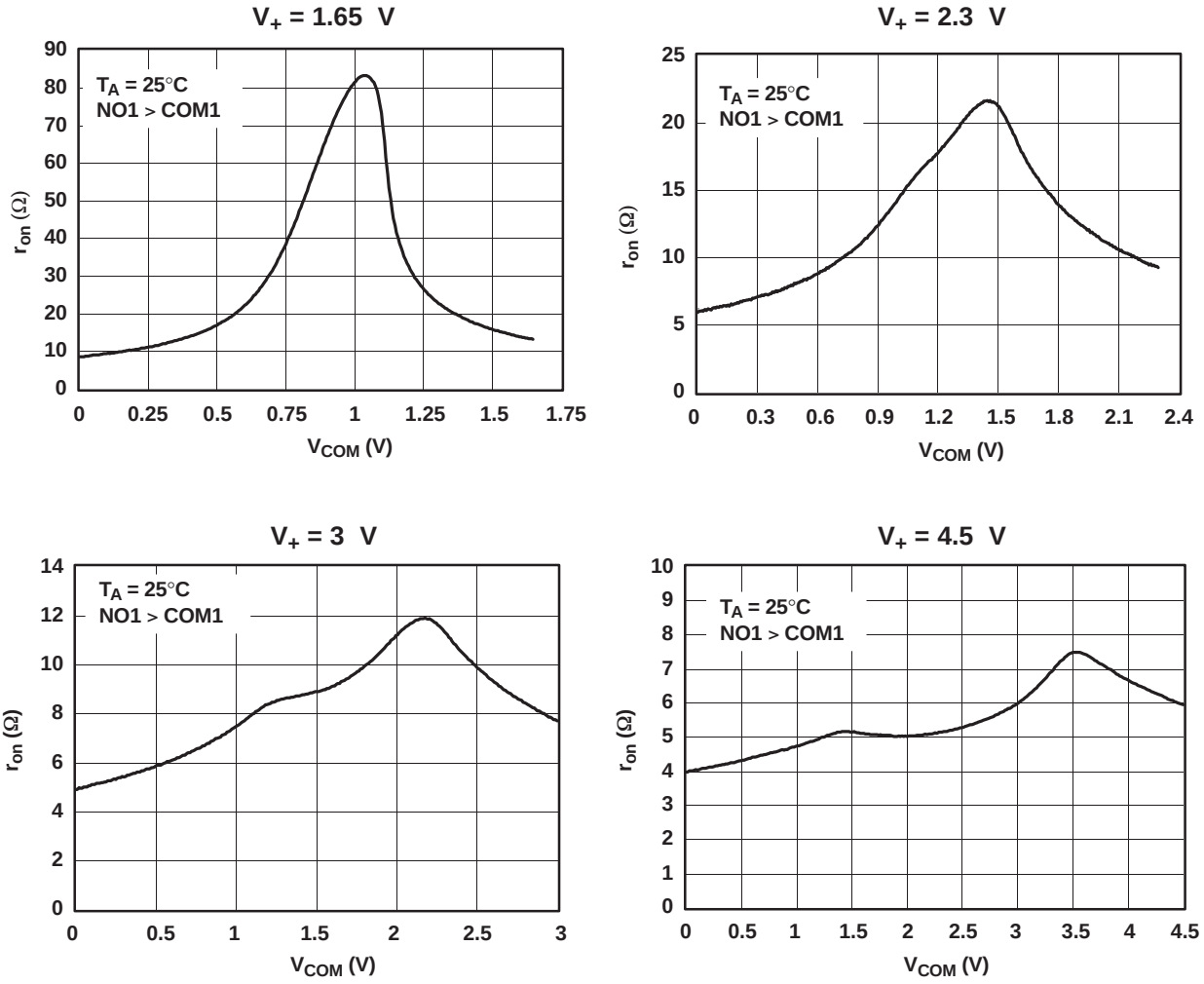


Figure 1. r_{on} vs V_{COM}

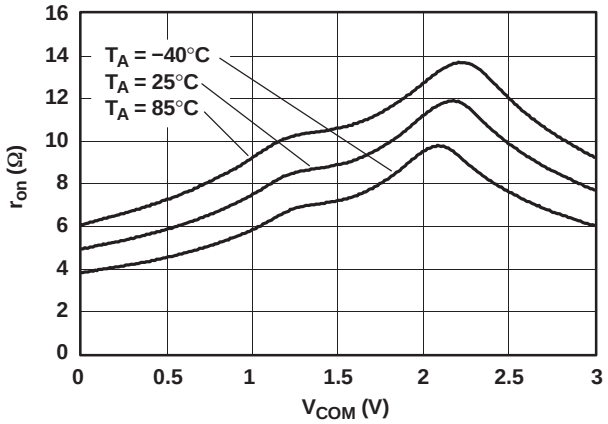


Figure 2. r_{on} vs V_{COM} (V_+ = 3 V)

TYPICAL PERFORMANCE (continued)

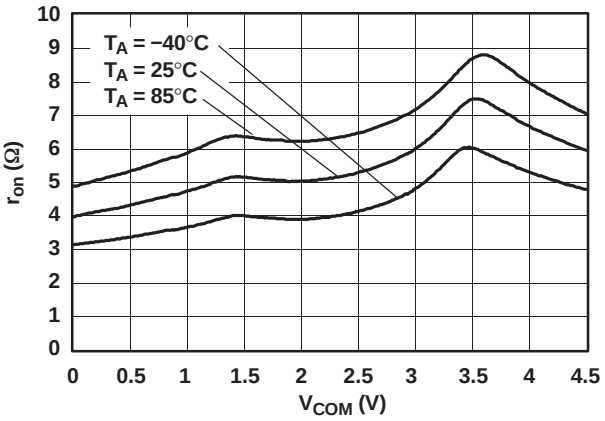


Figure 3. r_{on} vs V_{COM} (V_+ = 4.5 V)

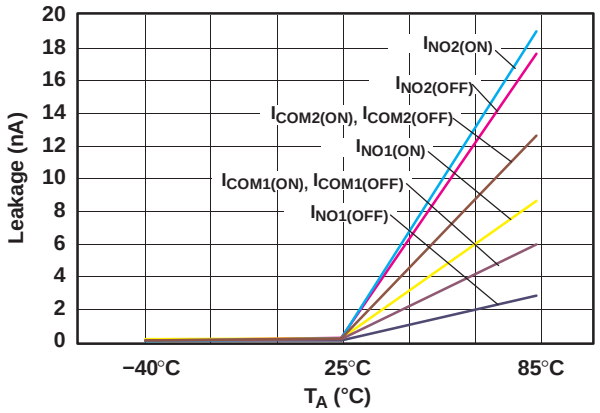


Figure 4. Leakage Current vs Temperature

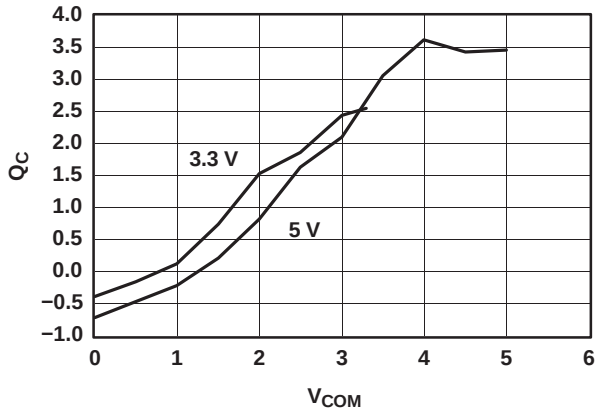


Figure 5. Charge Injection (Q_C) vs V_{COM}

TYPICAL PERFORMANCE (continued)

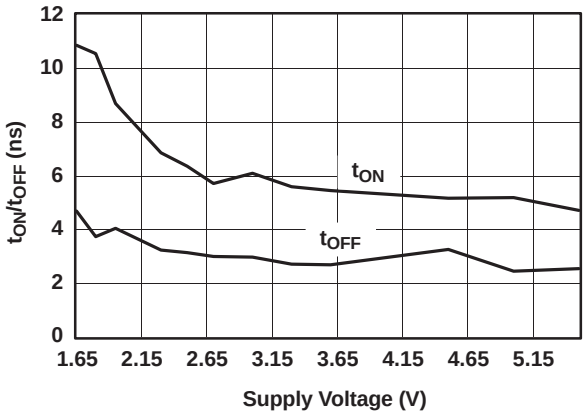


Figure 6. t_{ON} and t_{OFF} vs V_+

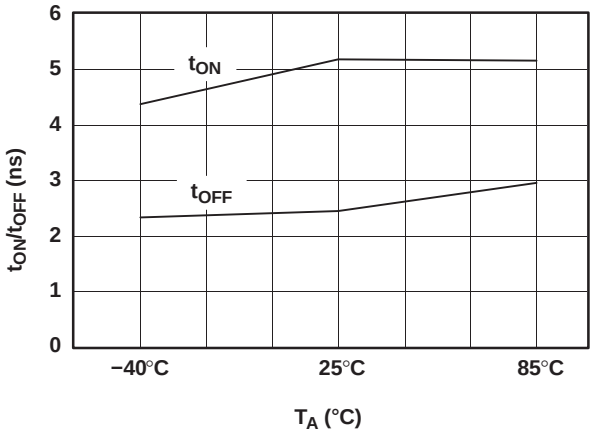


Figure 7. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

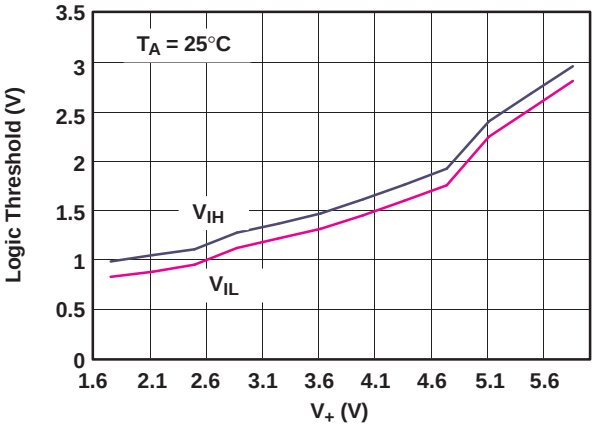


Figure 8. Logic Threshold vs V_+

TYPICAL PERFORMANCE (continued)

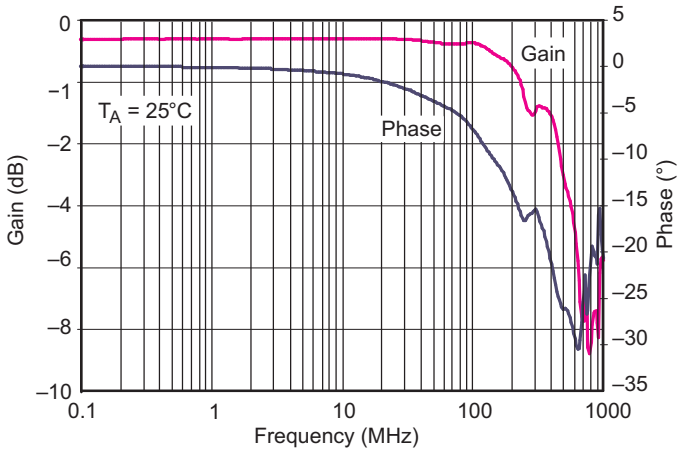


Figure 9. Bandwidth (V_+ = 5 V)

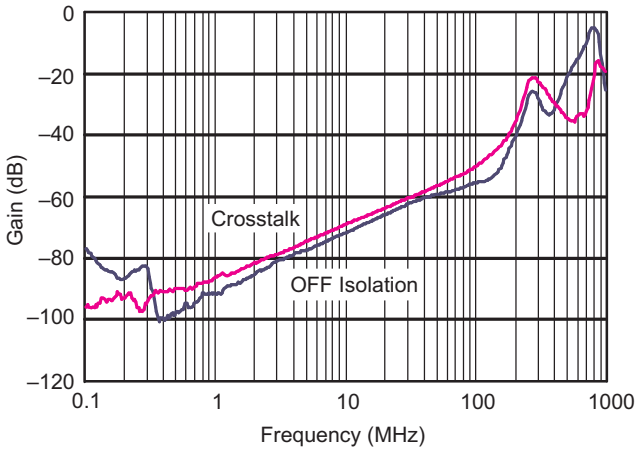


Figure 10. OFF Isolation and Crosstalk (V_+ = 5 V)

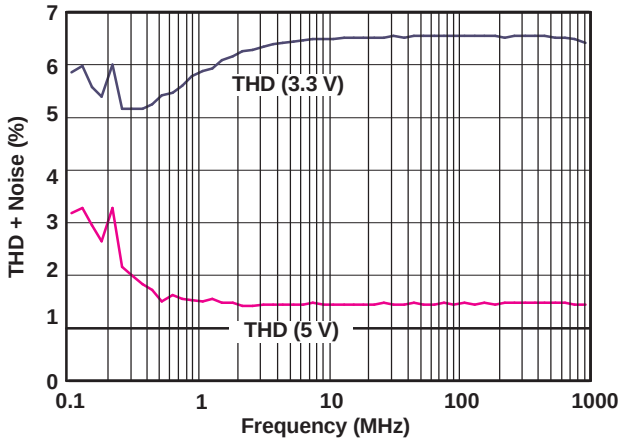


Figure 11. Total Harmonic Distortion vs Frequency

TYPICAL PERFORMANCE (continued)

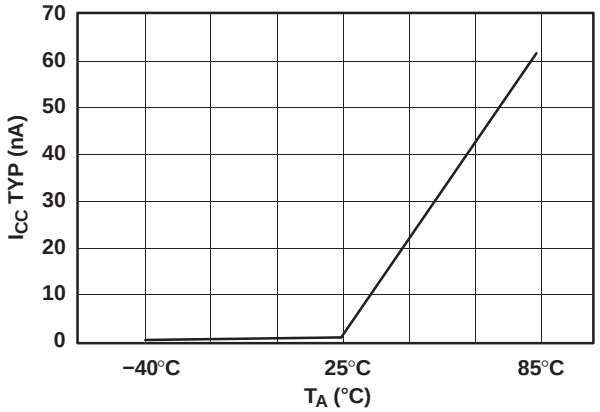


Figure 12. Power-Supply Current vs Temperature (V_+ = 5 V)

Table 2. PIN DESCRIPTION

NO.	NAME	DESCRIPTION
1	NO1	Normally open
2	COM1	Common
3	IN2	Digital control to connect COM to NO
4	GND	Digital ground
5	NO2	Normally open
6	COM2	Common
7	IN1	Digital control to connect COM to NO
8	V_+	Power supply

Table 3. PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NO ports when the channel is ON
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the OFF state
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON state and the output (NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input.Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C_I	Capacitance of IN
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an adjacent ON channel (NC1 to NC2). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion is defined as the ratio of the root mean square (RMS) value of the second, third, and higher harmonics to the magnitude of fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

PARAMETER MEASUREMENT INFORMATION

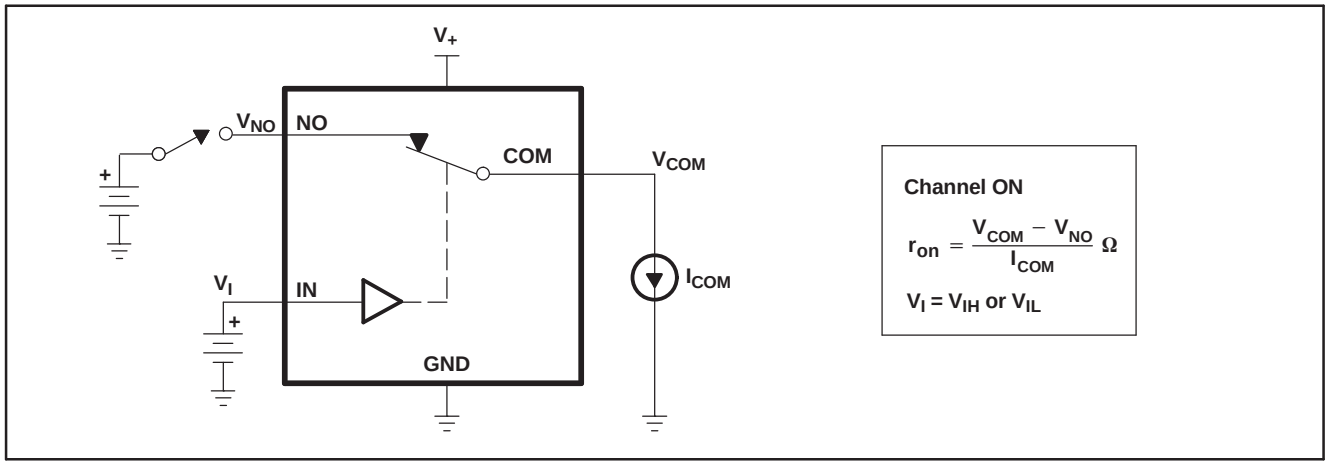


Figure 13. ON-State Resistance (r_{on})

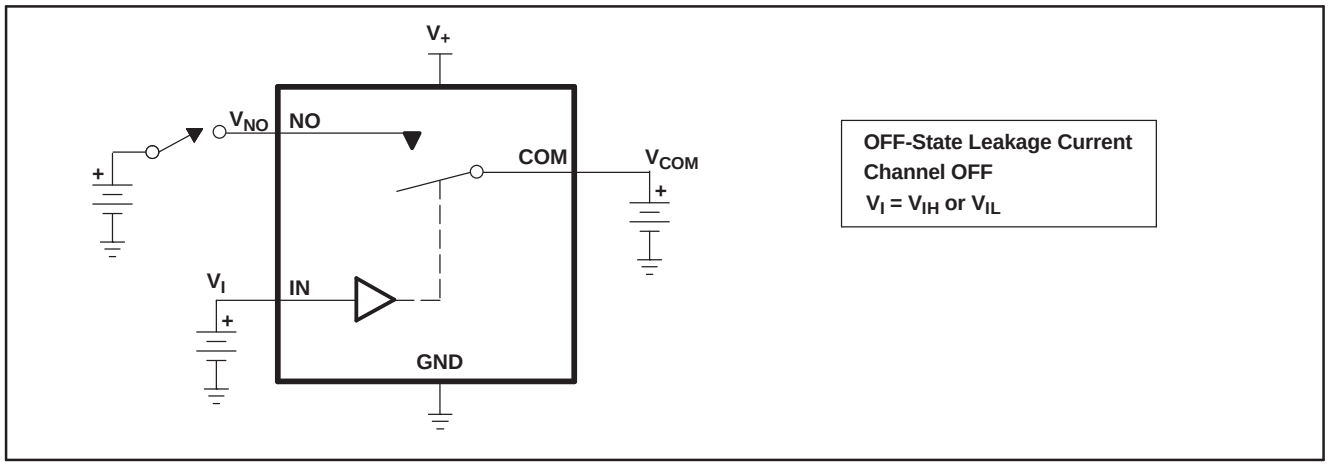


Figure 14. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NO(OFF)}$)

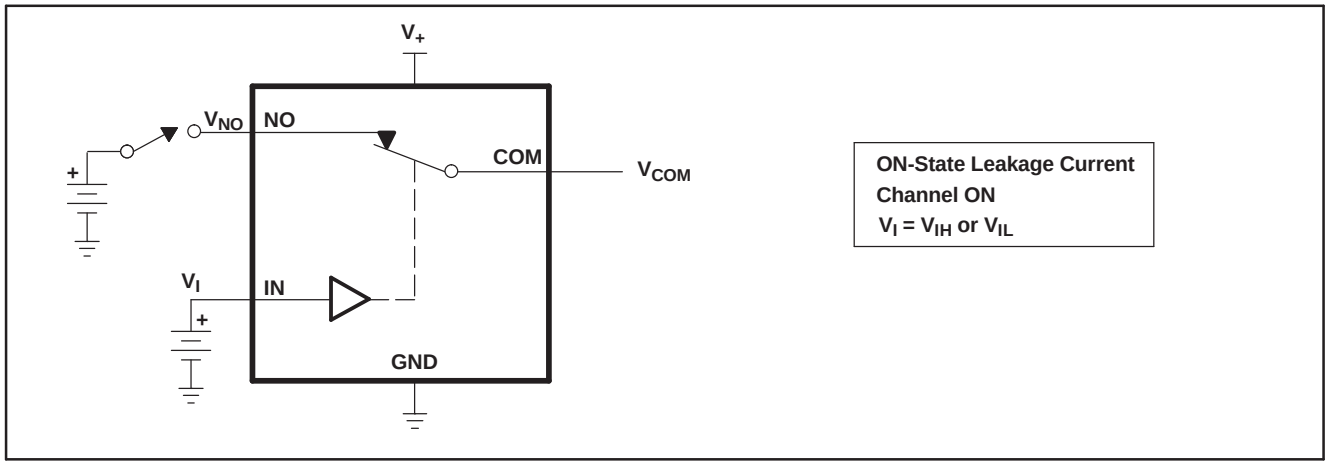


Figure 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NO(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

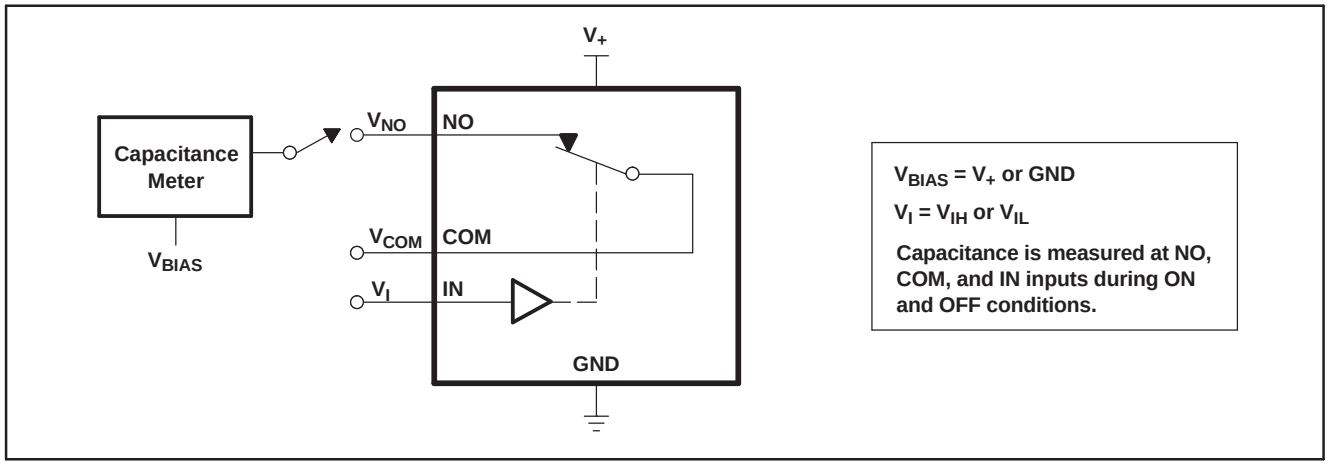


Figure 16. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{NO(ON)}$)

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

(3) See Electrical Characteristics for V_{COM}.

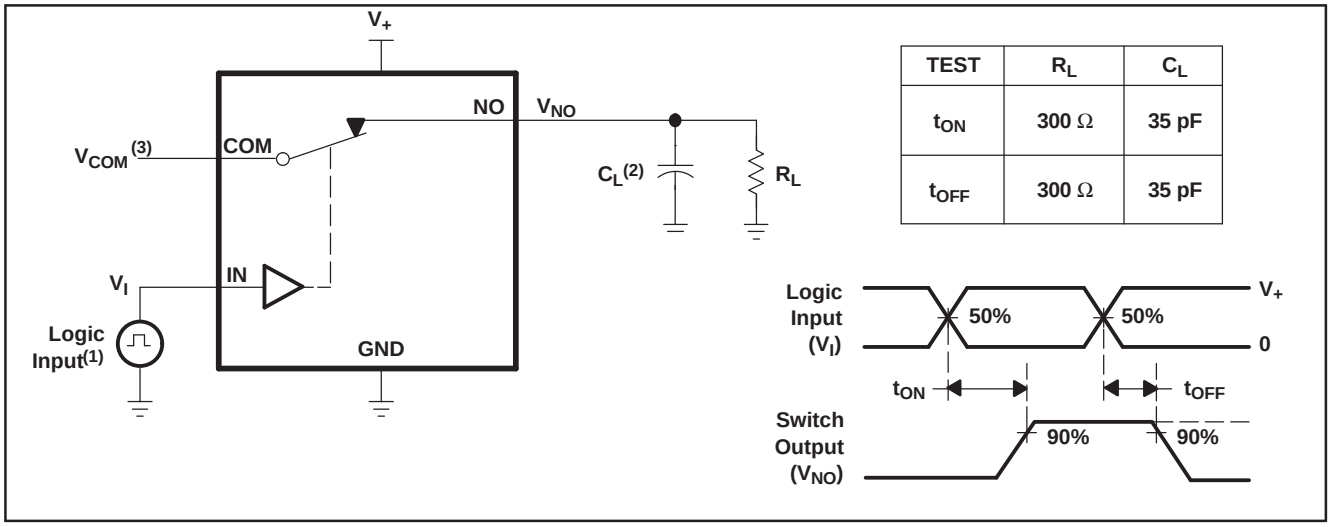


Figure 17. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

PARAMETER MEASUREMENT INFORMATION (continued)

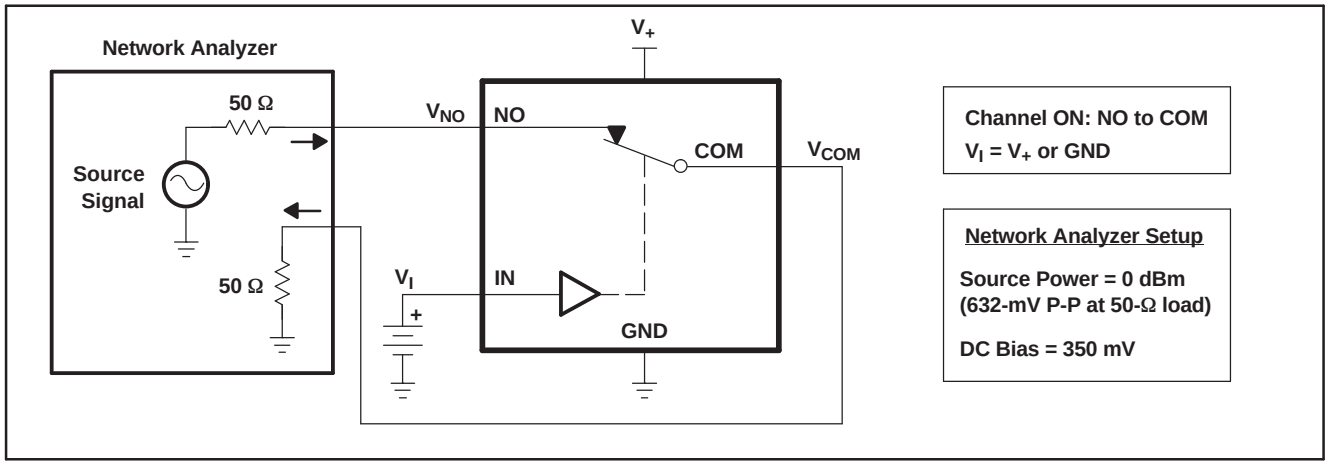


Figure 18. Bandwidth (BW)

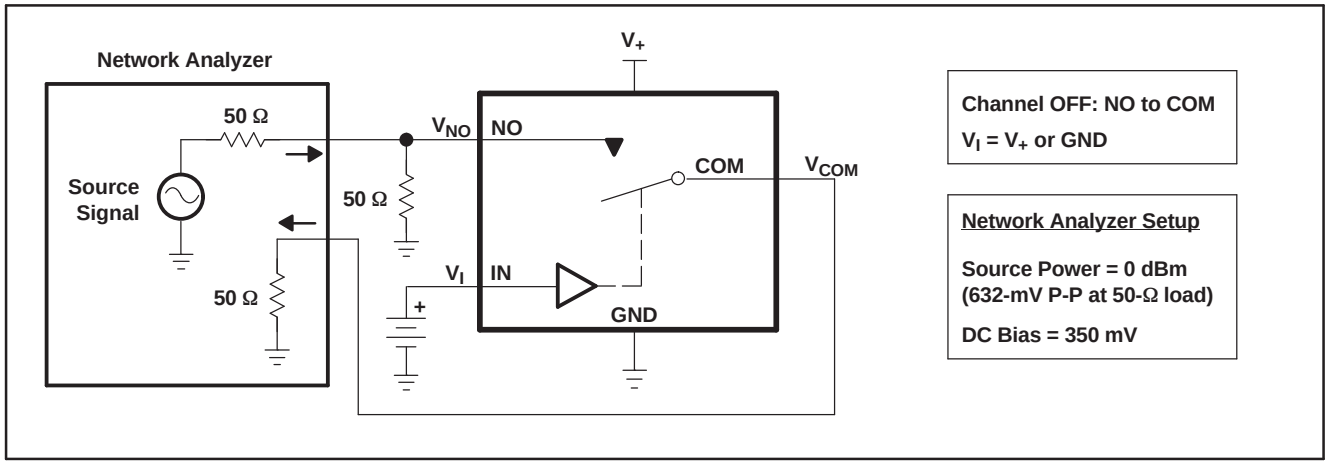


Figure 19. OFF Isolation (O_{ISO})

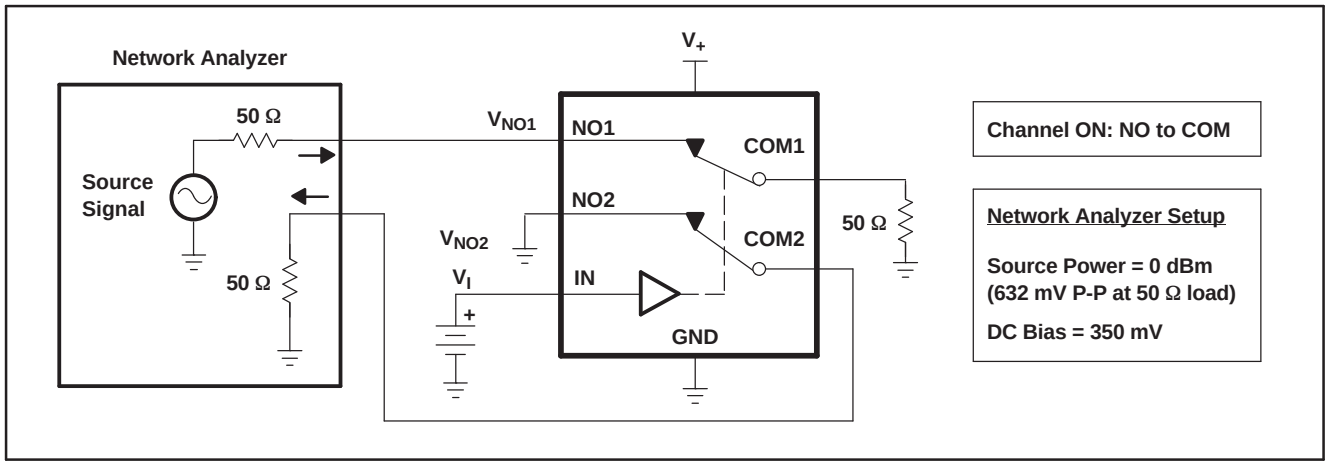


Figure 20. Crosstalk (X_{TALK})

(4) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(5) C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION (continued)

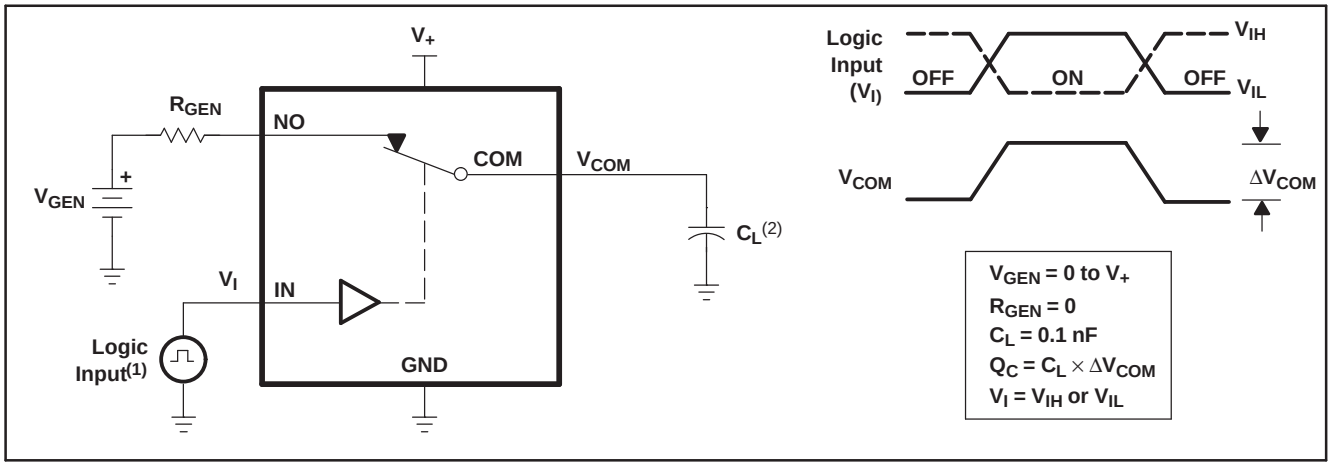


Figure 21. Charge Injection (Q_C)

(6) C_L includes probe and jig capacitance.

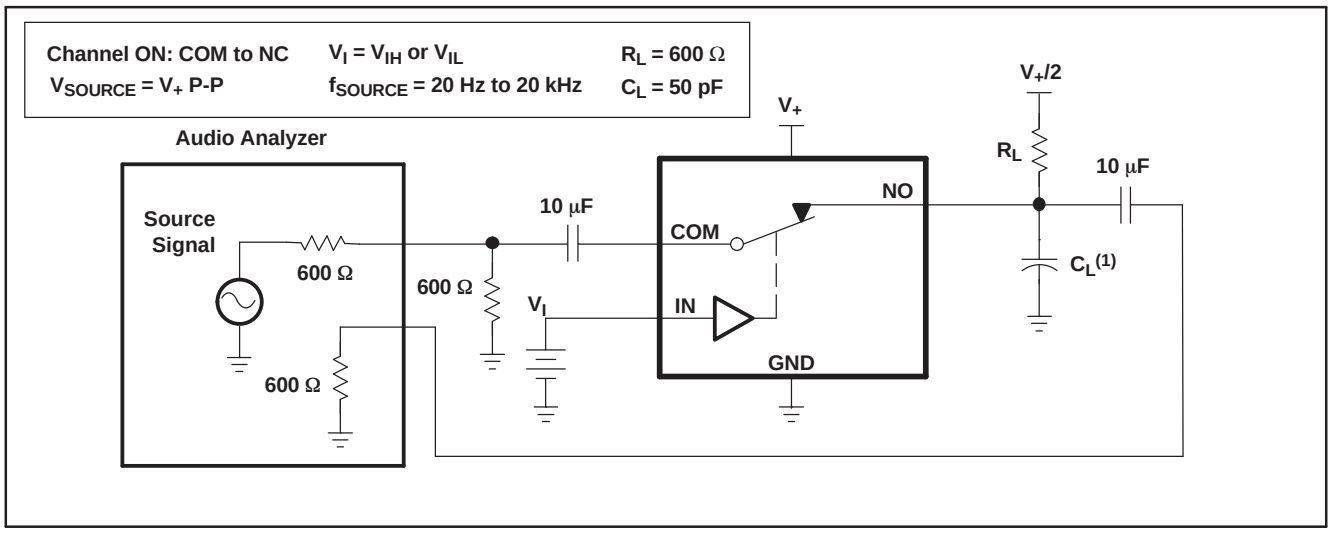


Figure 22. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A2066DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAG Z	Samples
TS5A2066DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAG Z	Samples
TS5A2066DCUR	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAGR	Samples
TS5A2066DCURE4	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAGR	Samples
TS5A2066DCURG4	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAGR	Samples
TS5A2066YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(J47 ~ J4N)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

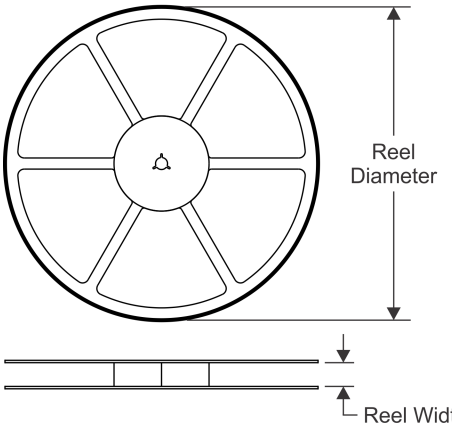
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

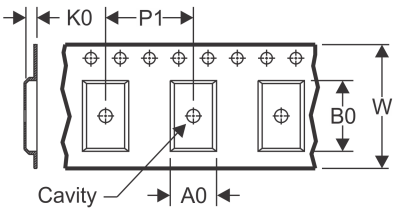
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

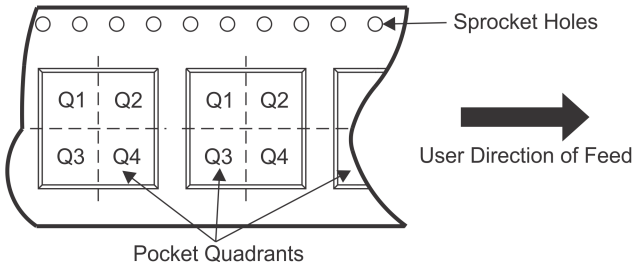


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

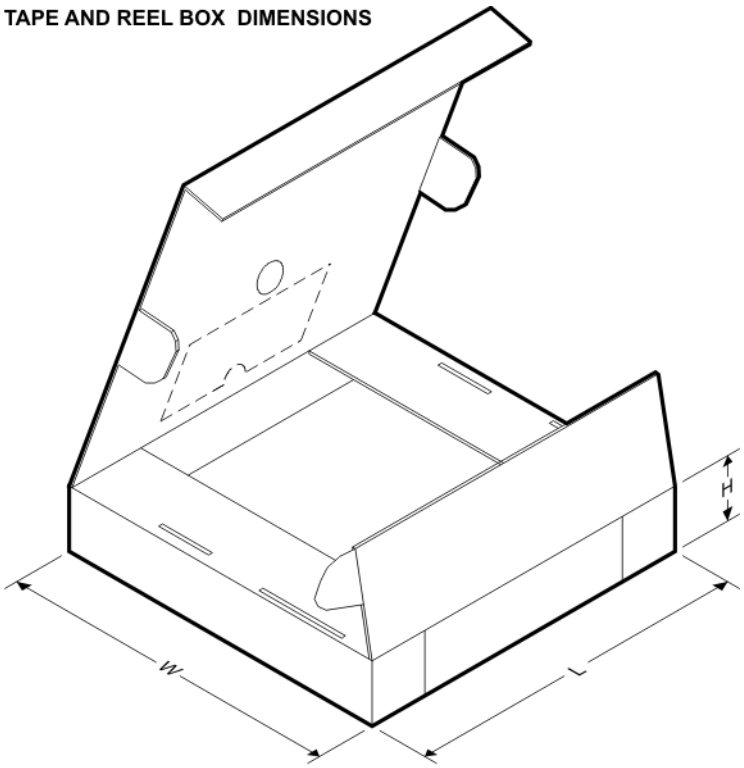
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A2066DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
TS5A2066DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A2066DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A2066YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

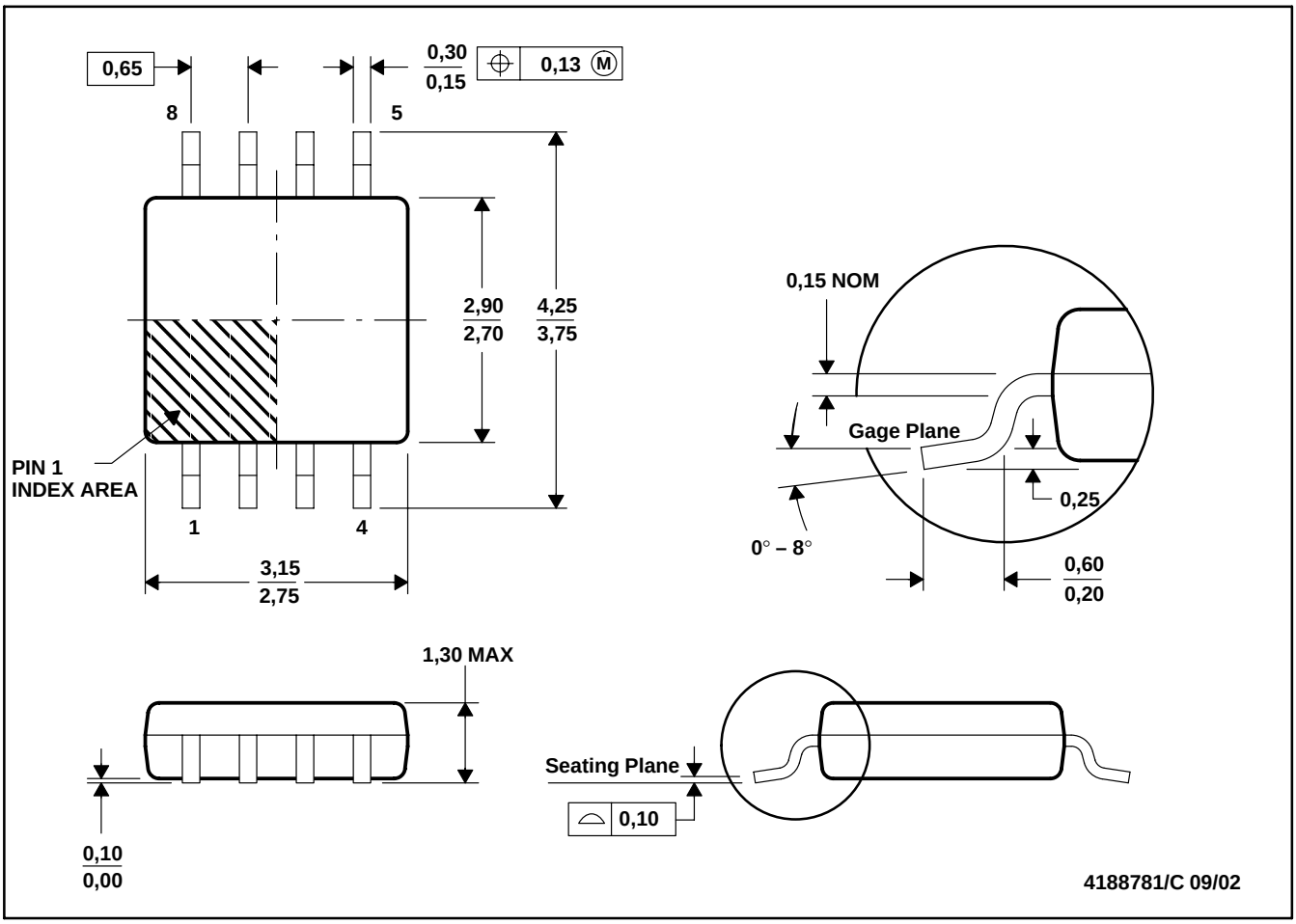


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A2066DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
TS5A2066DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A2066DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A2066YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

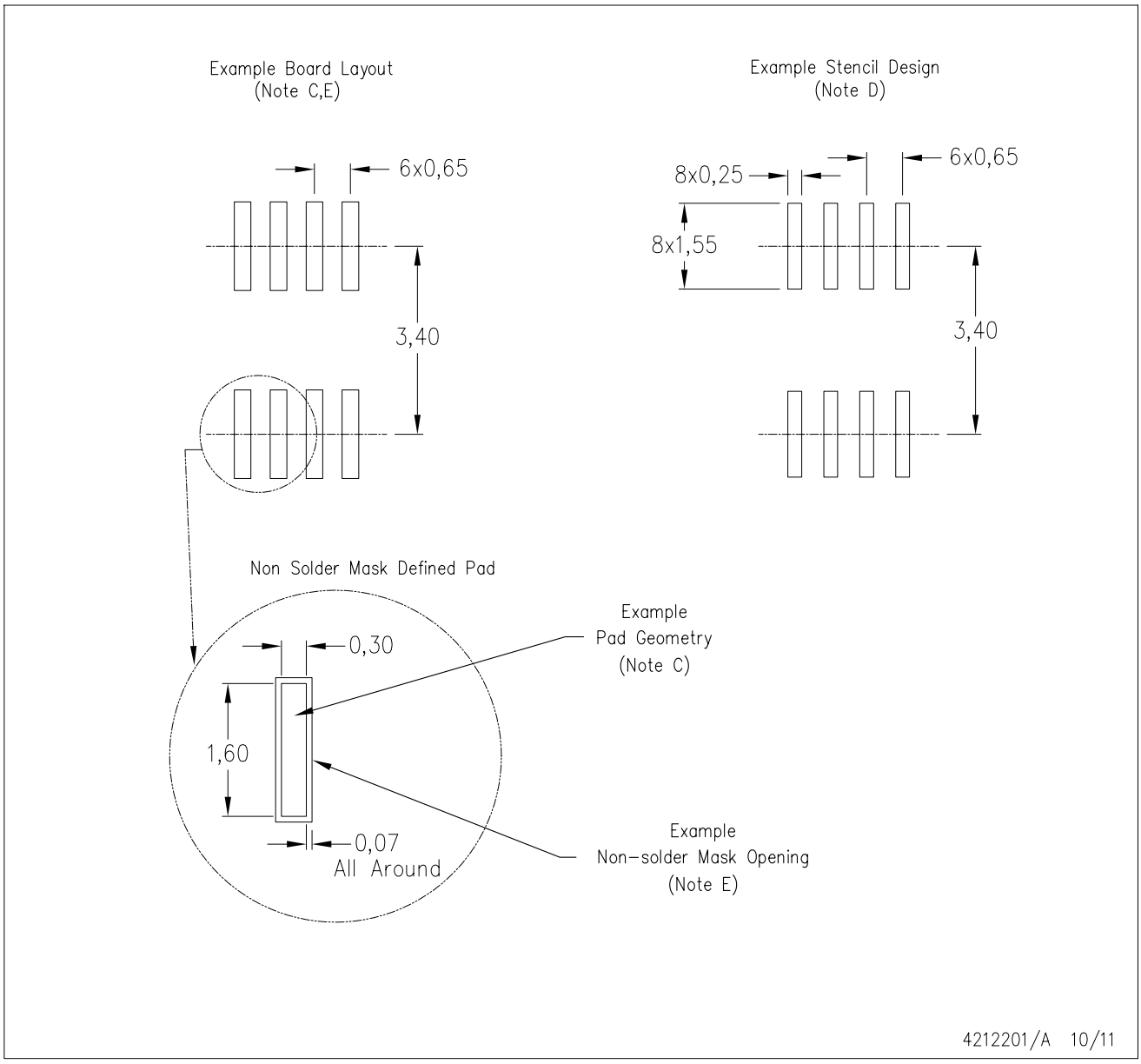
MPDS049B – MAY 1999 – REVISED OCTOBER 2002

DCT (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. Falls within JEDEC MO-187 variation DA.

DCT (R–PDSO–G8) PLASTIC SMALL OUTLINE



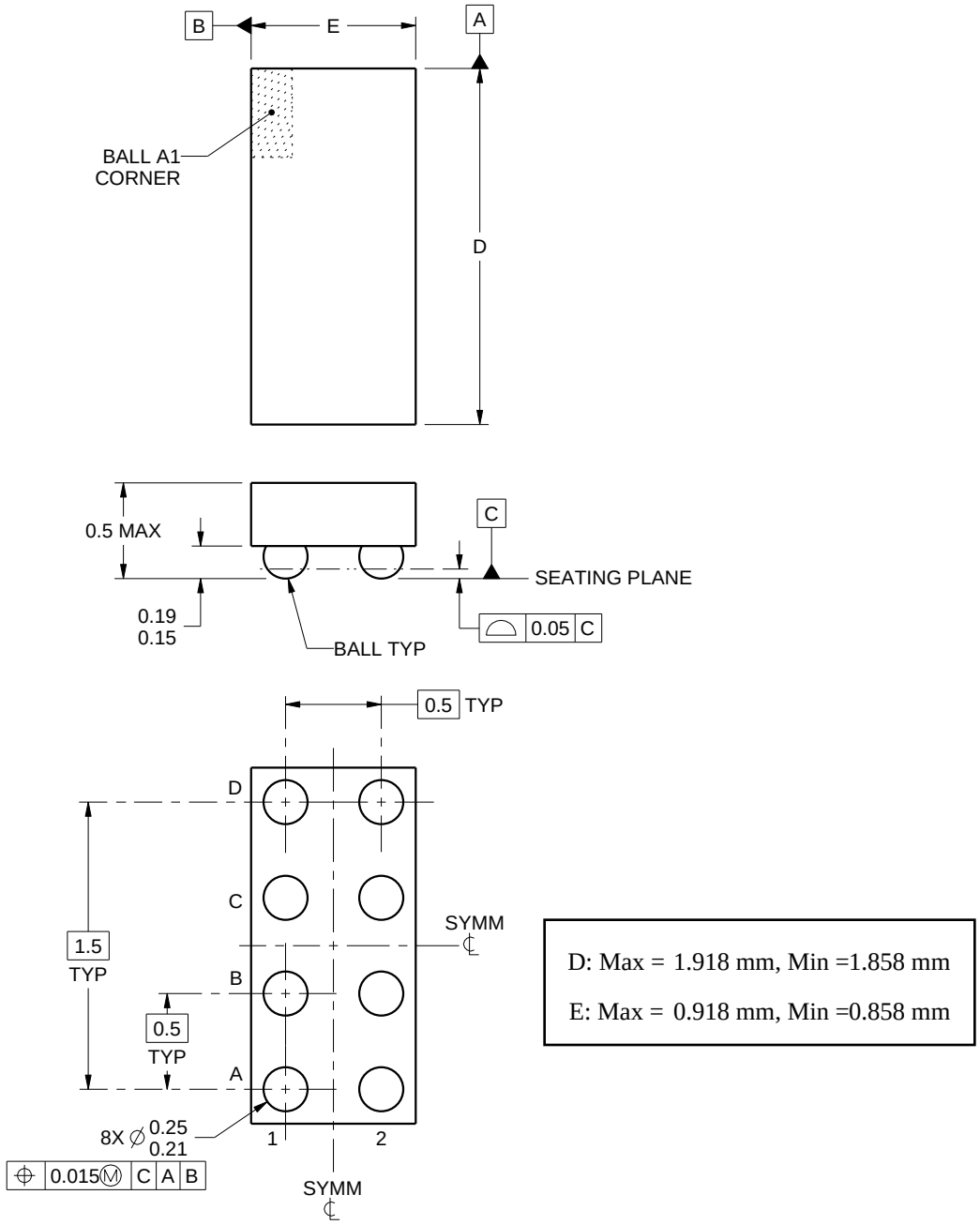
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

YZP0008

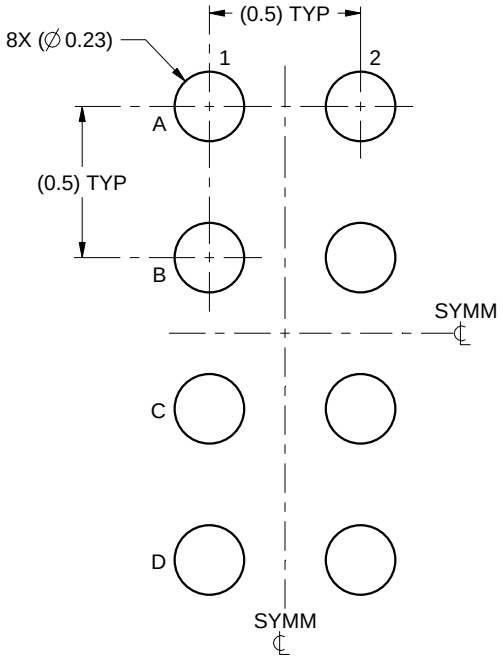
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

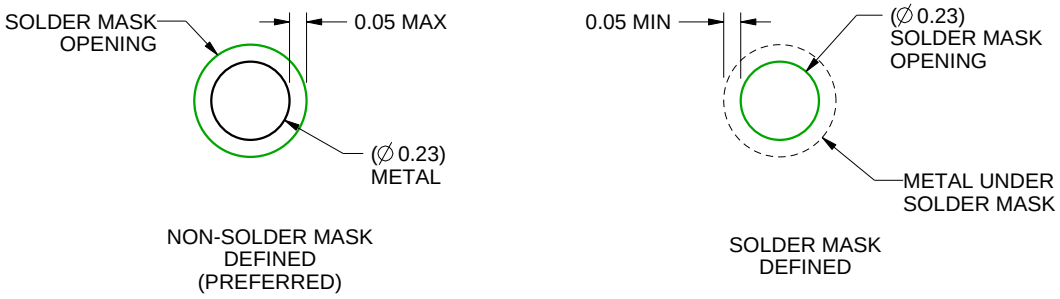


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

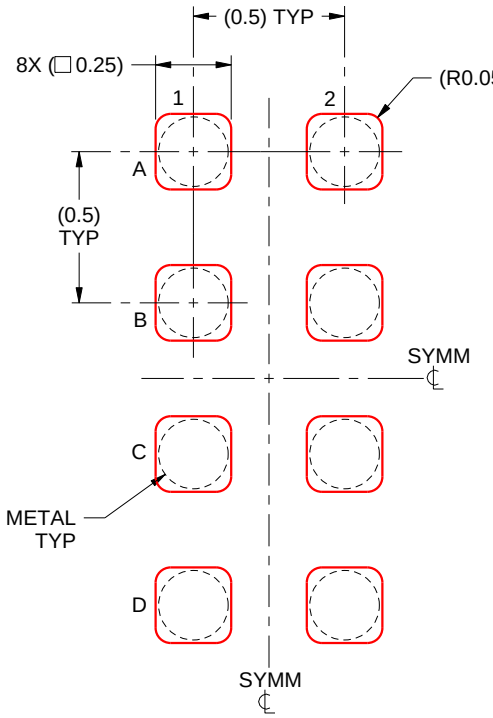


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



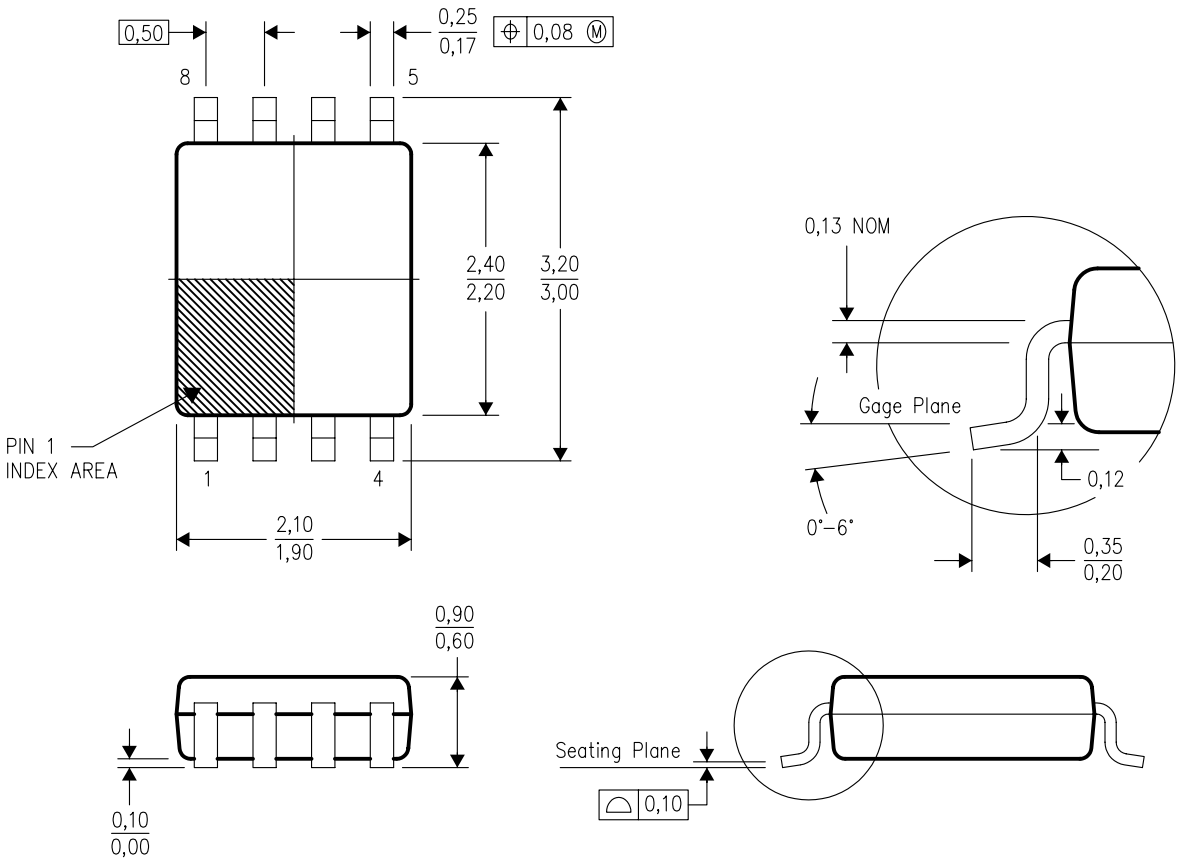
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

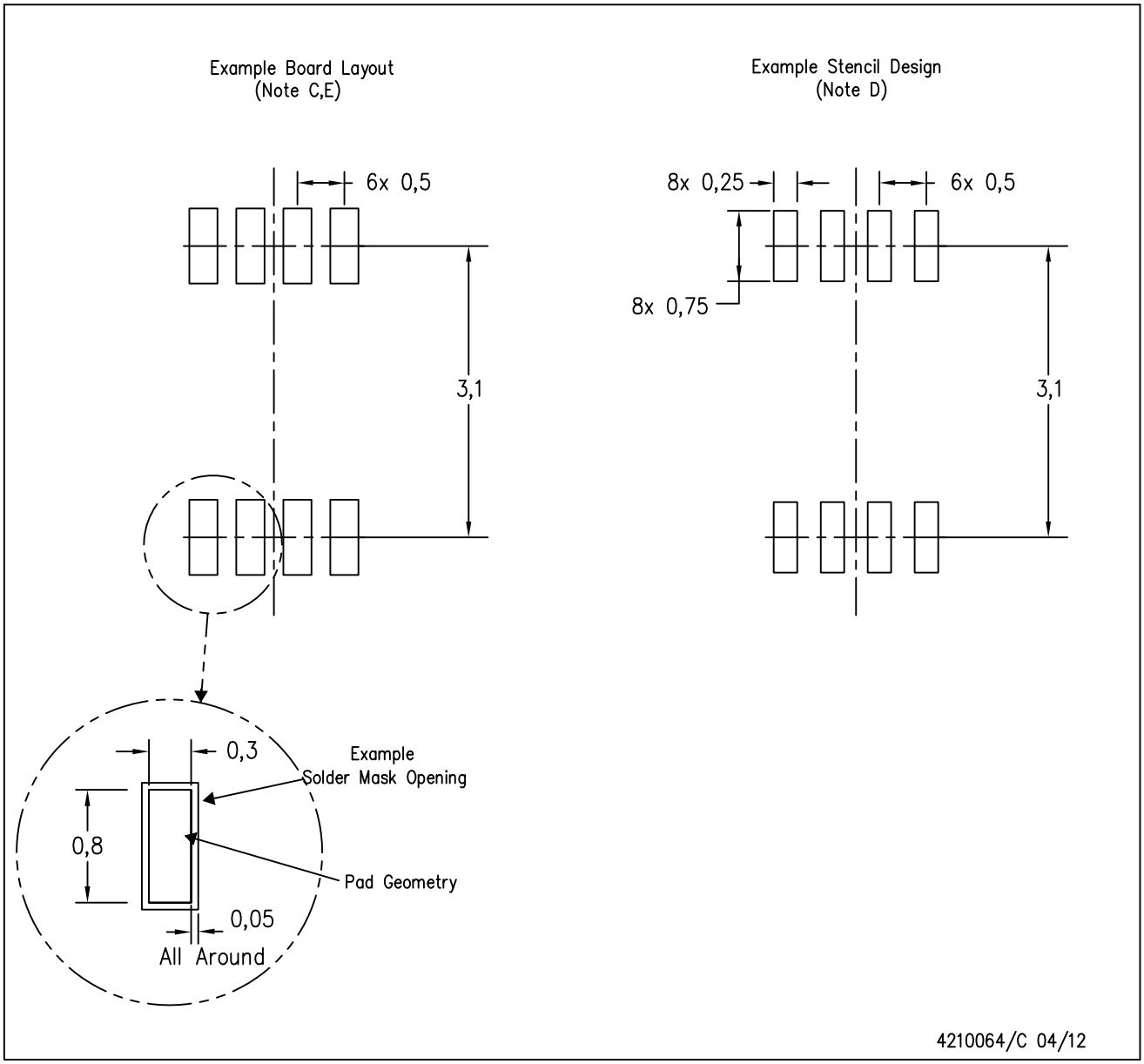
DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



4200503/F 07/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

DCU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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