TAS3251 175-W Stereo, 350-W Mono Ultra-HD Digital-Input Class-D Amplifier with Advanced DSP Processing

1 Features

- Flexible Audio Inputs
  - I^2S, TDM, Left-Justified, Right-Justified
  - 32 kHz, 44.1 kHz, 48 kHz, 96 kHz
  - Supports 3-Wire Digital Input (No MCLK)
- Total Output Power at 10% THD+N
  - 175-W Stereo into 4 Ω in BTL Configuration
  - 220-W Stereo into 3 Ω in BTL Configuration
  - 350-W Mono into 2 Ω in PBTL Configuration
- Total Output Power at 1% THD+N
  - 140-W Stereo into 4 Ω in BTL Configuration
  - 175-W Stereo into 3 Ω in BTL Configuration
  - 285-W Mono into 2 Ω in PBTL Configuration
- Advanced Integrated Closed-Loop Design
  - Ultra Low 0.01% THD+N at 1 W into 4 Ω
  - <0.01% THD+N to Clipping
  - 60 dB PSRR (BTL, No Input Signal)
  - <95 µV Output Noise (A-Weighted)
  - >108 dB SNR (A-Weighted)
- Fixed-Function Processing Features
  - SmartEQ (15x BiQuads)
  - Crossover EQ (2x 5 BiQuads)
  - 3-Band Advanced DRC + AGL
  - Dynamic EQ and SmartBass
  - Sample Rate Conversion
- Control Features
  - I^2C Software Mode Control
  - Address Select Pin
- 90% Efficient Class-D Operation (4 Ω)
- Wide 12-V to 36-V Supply Voltage Operation
- Integrated Protection with Error Reporting: Undervoltage, Cycle-by-cycle Current Limit, Short Circuit, Clipping detection, Overtemperature Warning and Shutdown and DC Speaker Protection

2 Applications

- Bluetooth and WiFi Speakers
- Soundbars
- Subwoofers
- Bookshelf Stereo Systems
- Professional and Public Address (PA) Speakers
- Active Crossover and Two-Way Speakers

3 Description

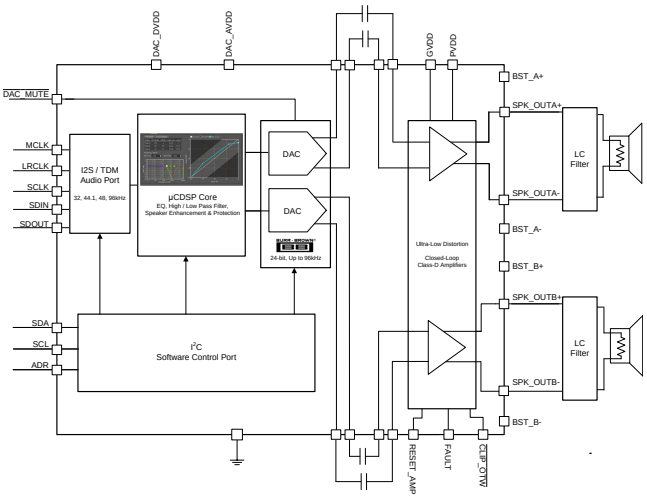
TAS3251 is a digital-input, high-performance Class-D audio amplifier that enables true premium sound quality with Class-D efficiency. The digital front-end features a high-performance Burr-Brown™ DAC with integrated DSP for advanced audio processing, including SmartAmp and SmartEQ. The first high-power single-chip solution reduces overall system solution size and cost. The DSP is supported by TI PurePath™ Console Graphical tuning software for quick and easy speaker tuning and control. The Class-D power stage features advanced integrated feedback and proprietary high-speed gate drive error correction for ultra-low distortion and noise across the audio band. The device operates in AD-mode and can drive up to 2 x 175 W into 4 Ω load and 2 x 220 W into 3 Ω load.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TAS3251	HSSOP (56)	18.41 mm × 7.49 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2018	*	Initial release.

5 Device Comparison Table

DEVICE NAME	DESCRIPTION	AUDIO INPUT INTERFACE	PAD LOCATION
TAS3251	175-W Stereo, 350-W Mono Ultra-HD Digital-Input Class-D Amplifier with Advanced DSP Processing	Digital	Top
TAS3245	115-W Stereo, 230-W Mono Ultra-HD Digital-Input Class-D Amplifier with Advanced DSP Processing	Digital	Top
TAS5782M	30-W Stereo, 60-W Mono Digital-Input Class-D Amplifier with Advanced DSP Processing	Digital	Bottom
TPA3244	60-W Stereo, 100-W Peak Ultra-HD Pad-Down Class-D Amplifier	Analog	Bottom
TPA3245	115-W Stereo, 230-W Mono Ultra-HD Analog-Input Class-D Amplifier	Analog	Top
TPA3250	70-W Stereo, 130-W Peak Ultra-HD Pad-Down Class-D Amplifier	Analog	Bottom
TPA3251	175-W Stereo, 350-W Mono Ultra-HD Analog-Input Power Stage	Analog	Top
TPA3255	315-W Stereo, 600-W Mono Ultra-HD Analog-Input Class-D Amplifier	Analog	Top

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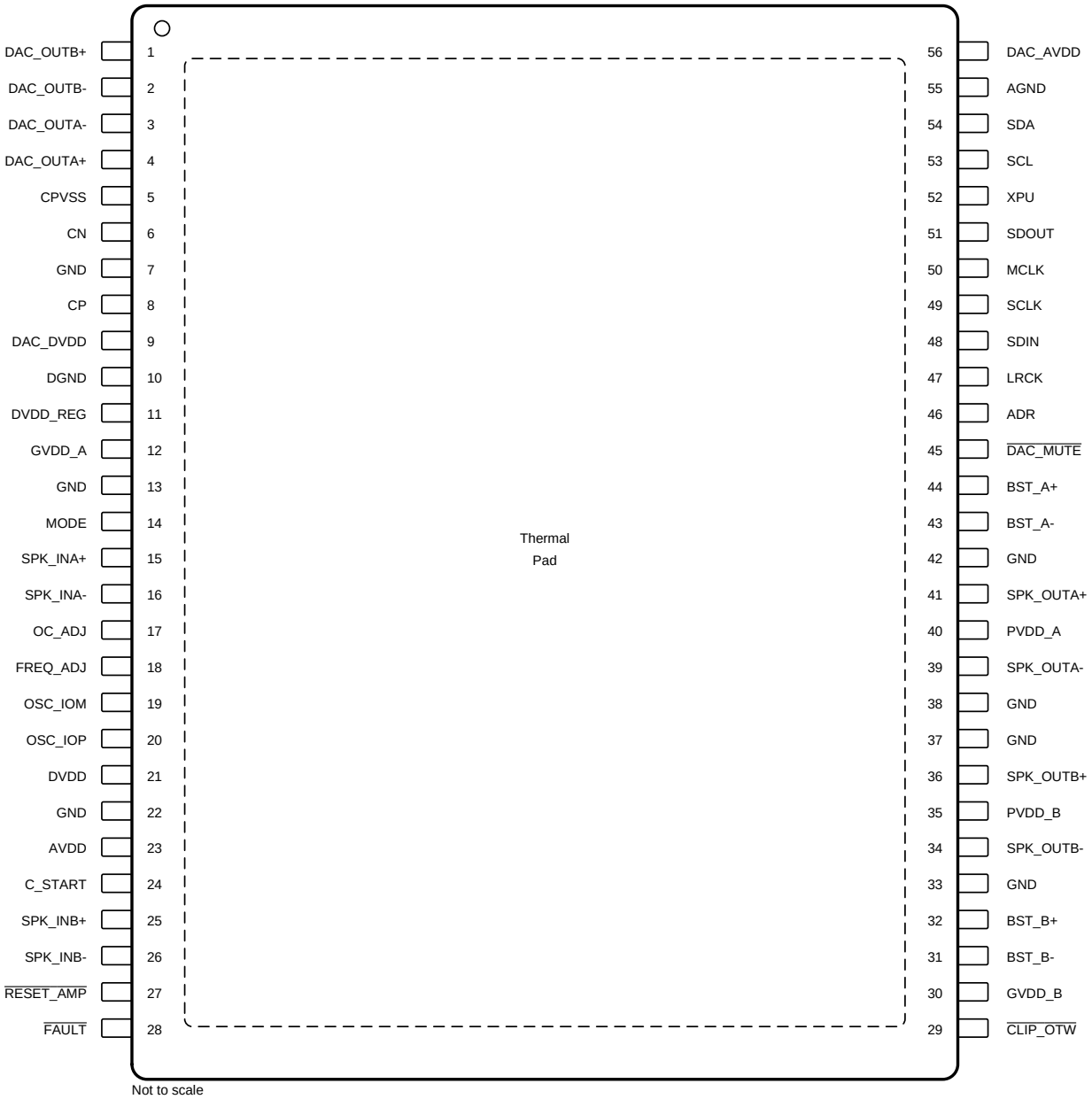
6 Pin Configuration and Functions

DKQ Package
56-Pin HSSOP with PowerPAD™
Top View



Not to scale

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Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	DAC_OUTB+	O	Differential DAC output B+.
2	DAC_OUTB-	O	Differential DAC output B-.
3	DAC_OUTA-	O	Differential DAC output A-.
4	DAC_OUTA+	O	Differential DAC output A+.
5	CPVSS	P	–3.3 V negative charge pump supply output for DAC. Connect 1 µF ceramic capacitor to GND. Refer to section: Power Supply Recommendations
6	CN	P	Negative pin for capacitor connection used in the line-driver charge pump. Connect 1 µF ceramic capacitor from CN to CP. Refer to section: Power Supply Recommendations
7	GND	G	Ground pin for device.
8	CP	P	Positive pin for capacitor connection used in the line-driver charge pump. Connect 1 µF capacitor from CN to CP. Refer to section: Power Supply Recommendations
9	DAC_DVDD	P	DAC power supply input for digital logic and charge pump. Connect 3.3 V and a 1 uF ceramic capacitor to GND. Refer to section: DAC_DVDD and DAC_AVDD Supplies
10	DGND	G	Ground reference for digital circuitry. Connect this pin to the system ground.
11	DVDD_REG	P	DAC voltage regulator output derived from DAC_DVDD supply for use for internal digital circuitry (1.8 V). This pin is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry. Connect 1 µF ceramic capacitor to GND. Refer to section: DAC_DVDD and DAC_AVDD Supplies
12	GVDD_A	P	Gate drive supply input for amplifier channel A. Connect 12 V and a 0.1 µF capacitor to GND. Refer to section: GVDD_X Supply
13	GND	G	Ground pin for device.
14	MODE	I	Output configuration mode selection. BTL = 0, PBTL = 1. Refer to table: Mode Selection Pins
15	SPK_INA+	I	Input signal for half-bridge A+.
16	SPK_INA-	I	Input signal for half-bridge A-.
17	OC_ADJ	I / O	Over-Current threshold programming pin. Refer to section: Overload and Short Circuit Current Protection
18	FREQ_ADJ	I / O	Oscillator frequency programming pin. Refer to section: Oscillator for Output Power Stage
19	OSC_IOM	I / O	PWM switching oscillator synchronization interface. Optional. Do not connect if unused. Refer to section: Oscillator Synchronization and Slave Mode
20	OSC_IOP	O	PWM switching oscillator synchronization interface. Optional. Do not connect if unused. Refer to section: Oscillator Synchronization and Slave Mode
21	DVDD	P	Internal voltage regulator, amplifier digital section. Connect 1 µF ceramic capacitor to GND. Refer to section: VDD Supply
22	GND	G	Ground pin for device.
23	AVDD	P	Internal voltage regulator, amplifier analog section. Connect 1 µF ceramic capacitor to GND. Refer to section: VDD Supply
24	C_START	O	Startup ramp, requires a charging capacitor to GND. Connect 10 nF to GND for best pop prevention. Refer to section: Pop and Click Free Startup and Shutdown
25	SPK_INB+	I	Input signal for half-bridge B+.
26	SPK_INB-	I	Input signal for half-bridge B-.
27	$\overline{\text{RESET\_AMP}}$	I	Device reset, active low. Use for amplifier reset and mute. Refer to section: Output Power Stage Reset
28	$\overline{\text{FAULT}}$	O	Shutdown signal, open drain; active low. Internal pull-up resistor to DVDD. Do not connect if unused. Refer to section: Device Output Stage Protection System
29	$\overline{\text{CLIP\_OTW}}$	O	Clipping warning and over-temperature warning; open drain; active low. Internal pull-up resistor to DVDD. Do not connect if unused. Refer to section: Device Output Stage Protection System
30	GVDD_B	P	Gate drive supply input for amplifier channel B. Connect 12 V and a 0.1 µF capacitor to GND. Refer to section: GVDD_X Supply
31	BST_B-	P	HS bootstrap supply (BST), external 0.033 µF capacitor to SPK_OUTB-. Refer to section: BST Supply
32	BST_B+	P	HS bootstrap supply (BST), external 0.033 µF capacitor to SPK_OUTB+. Refer to section: BST Supply
33	GND	G	Ground pin for device.
34	SPK_OUTB-	O	Output, half bridge B-.
35	PVDD_B	P	PVDD supply for channel B. Connect large bulk capacitor and 1 µF ceramic decoupling capacitor to GND and place near pin. Refer to section: PVDD Supply
36	SPK_OUTB+	O	Output, half bridge B+.
37	GND	G	Ground pin for device.
38	GND	G	Ground pin for device.

(1) I=Input, O=Output, I/O= Input/Output, P=Power, G=Ground

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Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
39	SPK_OUTA-	O	Output, half bridge A-.
40	PVDD_A	P	PVDD supply for channel A. Connect large bulk capacitor and 1 µF ceramic decoupling capacitor to GND and place near pin. Refer to section: PVDD Supply
41	SPK_OUTA+	O	Output, half bridge A+.
42	GND	G	Ground pin for device.
43	BST_A-	P	HS bootstrap supply (BST), external 0.033 µF capacitor to SPK_OUTA-. Refer to section: BST Supply
44	BST_A+	P	HS bootstrap supply (BST), external 0.033 µF capacitor to SPK_OUTA+. Refer to section: BST Supply
45	$\overline{\text{DAC\_MUTE}}$	I	Hardware controlled DAC mute function. Pull low (connected to DGND) to mute the device and pull high (connected to DAC_DVDD) to unmute the device. Refer to section: Mute with DAC_MUTE or Clock Error
46	ADR	I	Sets the LSB of the I²C address to 0 if pulled to GND, to 1 if pulled to DAC_DVDD. Refer to table: Slave Address Select
47	LRCK	I	Left-Right Word (I²S) or Frame (TDM) select clock for digital audio signal. In I²S, LJ, and RJ, this corresponds to the left channel and right channel boundary. In TDM mode, this corresponds to the frame sync boundary. Refer to section: Serial Audio Port
48	SDIN	I	Audio data serial port, data in. Refer to section: Serial Audio Port
49	SCLK	I	Serial or bit clock for the digital signal that is active on the input data line of the serial data port. Refer to section: Serial Audio Port
50	MCLK	I	Master clock used for internal clock tree and sub-circuit and state machine clocking. Refer to section: Serial Audio Port
51	SDOUT	I / O	Audio data serial port, data output. Refer to section: SDOUT Port and Hardware Control Pin
52	XPU	I	External pull-up, logic level pin. For normal operation, this pin should be connected directly to 3.3 V (DAC_DVDD or DAC_AVDD).
53	SCL	I	I²C serial control port clock. Refer to section: I2C Communication Port
54	SDA	I / O	I²C serial control port data. Refer to section: I2C Communication Port
55	AGND	G	Ground reference for analog circuitry. Connect to system ground.
56	DAC_AVDD	P	DAC power supply input for DAC internal analog circuitry. Connect 3.3 V and a 1 uF ceramic capacitor to GND. Refer to section: DAC_DVDD and DAC_AVDD Supplies
	PowerPAD™	G	Ground, connect to grounded heat sink.

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Table 1. Mode Selection Pins

Output Configuration	Input Mode	MODE Pin	SPK_INB+ Pin	SPK_INB- Pin	Description
2 x BTL	2N + 1	0	X	X	Stereo BTL output configuration
1 x PBTL	2N + 1	1	0	0	Paralleled BTL configuration pre-filter or post-filter. Connect SPK_INB+ and INPUT_B- to GND with no DC blocking capacitor.

Table 2. I²C Device Slave Address

ADR Pin		Hex	Binary
0	7-bit Address	0x4A	1001 010
	7-bit Address + Write Bit	0x94	1001 0100
	7-bit Address + Read Bit	0x95	1001 0101
1	7-bit Address	0x4B	1001 011
	7-bit Address + Write Bit	0x96	1001 0110
	7-bit Address + Read Bit	0x97	1001 0111

7 Specifications

7.1 Absolute Maximum Ratings

Free-air room temperature 25°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage	PVDD_X to GND(2)	-0.3	50	V
	BST_X to GVDD_X(2)	-0.3	50	V
	BST_X to GND(2)	-0.3	62.5	V
	VDD to GND	-0.3	13.2	V
	GVDD_X to GND(2)	-0.3	13.2	V
	DVDD to GND	-0.3	4.2	V
	AVDD to GND	-0.3	8.5	V
	DAC_DVDD, DAC_AVDD	-0.3	3.9	V
Analog Interface Pins	SPK_OUTX to GND(2)	-0.3	50	V
	SPK_INX to GND	-0.3	7	V
Digital Interface Pins	OC_ADJ, MODE, OSC_IOP, OSC_IOM, FREQ_ADJ, C_START to GND	-0.3	4.2	V
	$\overline{\text{RESET\_AMP}}$, $\overline{\text{FAULT}}$, $\overline{\text{CLIP\_OTW}}$ to GND	-0.3	4.2	V
	Continuous sink current $\overline{\text{RESET\_AMP}}$, $\overline{\text{FAULT}}$, $\overline{\text{CLIP\_OTW}}$ to GND		9	mA
	ADR, $\overline{\text{DAC\_MUTE}}$, LRCK, MCLK, SCL, SCLK, SDA, SDIN, SDOUT, XPU to GND	-0.5	V_{DAC_DVDD} + 0.5	V
T_J	Operating junction temperature range, power die	-40	165	°C
	Operating junction temperature, digital die	-40	125	°C
T_{stg}	Storage temperature range	-40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, and functional operation of the device at these or any other conditionsbeyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions forextended periods may affect device reliability.
(2) These voltages represents the DC voltage + peak AC waveformmeasured at the terminal of the device in all conditions..

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 2000-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safemanufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

Free-air room temperature 25°C (unless otherwise noted)

			MIN	TYP	MAX	UNIT
PVDD_X	Half-bridge supply	DC supply voltage	12	36	38	V
GVDD_X	Supply for logic regulators and gate-drive circuitry	DC supply voltage	10.8	12	13.2	V
VDD	Digital regulator supply voltage	DC supply voltage	10.8	12	13.2	V
DAC_AVDD	Power supply for DAC internal analog circuitry.	DC supply voltage	2.9	3.3	3.63	V
DAC_DVDD(1)	DAC digital power supply and power supply for charge pump	DC supply voltage	2.9	3.3	3.63	V
R_L(BTL)	Load impedance	Output filter inductance within recommended value range	2.7	4		Ω
R_L(PBTL)			1.6	2		
L_{OUT}(BTL)	Output filter inductance	Minimum output inductance at IOC	5			µH
L_{OUT}(PBTL)			5			
F_{PWM}	PWM frame resistor tolerance selectable for AM interference avoidance; 1% Resistor tolerance	Nominal	575	600	625	kHz
		AM1	475	500	525	
		AM2	430	450	470	
$R_{(FREQ\_ADJ)}$	PWM frame rate programming resistor	Nominal; Master mode	9.9	10	10.1	kΩ
		AM1; Master mode	19.8	20	20.2	
		AM2; Master mode	29.7	30	30.3	
C_{PVDD}	PVDD close decoupling capacitors		1.0			µF
R_{OC}	Over-current programming resistor	Resistor tolerance = 5%	22		30	kΩ
$R_{OC(LATCHED)}$	Over-current programming resistor	Resistor tolerance = 5%	47		64	kΩ
$V_{(FREQ\_ADJ)}$	Voltage on FREQ_ADJ pin for slave mode operation	Slave mode		3.3		V
$V_{IH(DigIn)}$	Input logic high for DAC_DVDD referenced digital inputs(1) (2)		0.9 × V_{DAC_DVDD}		V_{DAC_DVDD}	V
$V_{IL(DigIn)}$	Input logic low for DAC_DVDD referenced digital inputs(1) (3)		V_{DAC_DVDD}	0	0.1 × V_{DAC_DVDD}	V
T_J	Junction temperature		0		125	°C

(1) DAC_DVDD referenced digital pins include: ADR, LRCK, MCLK, $\overline{\text{DAC\_MUTE}}$, SCL, SCLK, SDA, SDIN, SDOUT and XPU.
(2) Front-end (DAC and DSP) pins should be referenced to DAC_DVDD. Power stage digital pins should be referenced to DVDD.
(3) All TAS3251 ground pins should be referenced to the system ground.

7.4 Thermal Information

THERMAL METRIC(1)		TAS3251 DKQ 56-PIN (HSSOP) JEDEC STANDARD 4-LAYER PCB	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and ICPackage Thermal Metrics* application report.

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7.5 Amplifier Electrical Characteristics

PVDD_X = 36 V, GVDD_X = 12 V, VDD = 12 V, T_C (Case temperature) = 75°C, f_s = 600 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AMPLIFIER INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION						
DVDD	Voltage regulator for internal use	VDD = 12 V	3	3.3	3.6	V
AVDD	Voltage regulator for internal use	VDD = 12 V		7.8		V
$I_{GVDD\_A + GVDD\_B + VDD}$	GVDD and VDD supply current	50% duty cycle		90		mA
		Reset mode		19		mA
I_{PVDD_X}	PVDD idle current	50% duty cycle with recommended output filter		20		mA
		Reset mode, no switching		0.0048		mA
ANALOG INPUTS						
R_{IN}	Input resistance			24		kΩ
V_{IN}	Maximum input voltage swing, SPK_INx pins			7		V
I_{IN}	Maximum input current, SPK_INx pins			1		mA
G	Inverting voltage gain	Amplifier VOUT/VIN		20		dB
AMPLIFIER OSCILLATOR						
$f_{OSC(IO+)}$	Nominal, Master Mode	F_{PWM} × 6	3.45	3.6	3.75	MHz
	AM1, Master Mode	F_{PWM} × 6	2.85	3	3.15	MHz
	AM2, Master Mode	F_{PWM} × 6	2.58	2.7	2.82	MHz
V_{IH}	High level input voltage		1.86			V
V_{IL}	Low level input voltage				1.45	V
OUTPUT-STAGE MOSFETs						
$R_{DS(on)}$	Drain-to-source resistance, low-side (LS)	T_J = 25°C, Includes metallization resistance, GVDD = 12 V		60	100	mΩ
	Drain-to-source resistance, high-side (HS)	T_J = 25°C, Includes metallization resistance, GVDD = 12 V		60	100	mΩ
AMPLIFIER I/O PROTECTION						
$V_{uvp,VDD,GVDD}$	Undervoltage protection limit, GVDD_X and VDD			9.5		V
$V_{uvp,VDD,\ GVDD,hyst}$	Undervoltage protection hysteresis, GVDD_X and VDD			0.6		V
OTW	Over-temperature warning, $\overline{CLIP\_OTW}$ (1)		115	125	135	°C
OTW_{hyst}	Temperature drop required to remove OTW event on $\overline{CLIP\_OTW}$			25		°C
OTE	Over-temperature error		145	155	165	°C
$OTE\text{-}OTW_{(differential)}$	OTE - OTW differential			30		°C
OTE_{hyst}	A reset is required to clear an OTE event			25		°C
OLPC	Overload protection counter for CB3C mode	F_{PWM} = 600 kHz (1024 PWM cycles for all F_{PWM})		1.7		ms
I_{OC}	Overcurrent limit for CB3C mode	Resistor – programmable, nominal peak current in 1Ω load, R_{OCP} = 22 kΩ		14		A
$I_{OC(LATCHED)}$	Overcurrent limit for latched mode	Resistor – programmable, peak current in 1Ω load, R_{OCP} = 47kΩ		14		A
I_{DCspkr}	DC speaker protection current threshold	BTL current imbalance threshold		1.5		A
I_{OCT}	Overcurrent response time	Time from switching transition to flip-state induced by overcurrent		150		ns
I_{PD}	Output pulldown current of each half-bridge	Connected when $\overline{RESET}$ is active to provide bootstrap charge		3		mA

(1) Specified by design.

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Amplifier Electrical Characteristics (continued)

PVDD_X = 36 V, GVDD_X = 12 V, VDD = 12 V, T_C (Case temperature) = 75°C, f_s = 600 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AMPLIFIER STATIC DIGITAL SPECIFICATIONS						
V_{IH}	High-level input voltage	MODE, OSC_IOP, OSC_IOM, RESET_AMP	1.9			V
V_{IL}	Low-level input voltage	MODE, OSC_IOP, OSC_IOM, RESET_AMP			0.8	V
I_{lkg}	Input leakage current	MODE, OSC_IOP, OSC_IOM, RESET_AMP			100	μA
AMPLIFIER OTW/SHUTDOWN (FAULT)						
R_{INT_PU}	Internal pullup resistance, $\overline{\text{CLIP\_OTW}}$ to DVDD, $\overline{\text{FAULT}}$ to DVDD		20	26	32	kΩ
V_{OH}	High-level output voltage	Internal pullup resistor	3	3.3	3.6	V
V_{OL}	Low-level output voltage	IO = 4 mA		200	500	mV
Device fanout	$\overline{\text{CLIP\_OTW}}$, $\overline{\text{FAULT}}$	No external pullup		30		devices

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7.6 DAC Electrical Characteristics

Free-air room temperature 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL I/O						
V_{IH1}	Input logic high threshold for DAC_DVDD referenced digital inputs (1)		70%			V_{DAC_DVDD}
V_{IL1}	Input logic low threshold for DAC_DVDD referenced digital inputs (1)				30%	V_{DAC_DVDD}
I_{IH1}	Input logic high current level for DAC_DVDD referenced digital input pins (1)	$V_{IN(DigIn)} = V_{DAC\_DVDD}$			10	µA
I_{IL1}	Input logic low current level for DAC_DVDD referenced digital input pins (1)	$V_{IN(DigIn)}$ = 0 V			–10	µA
$V_{OH(DigOut)}$	Output logic high voltage level (1)	I_{OH} = 4 mA	80%			V_{DAC_DVDD}
$V_{OL(DigOut)}$	Output logic low voltage level (1)	I_{OH} = –4 mA			22%	V_{DAC_DVDD}
I²C CONTROL PORT						
$C_{L(I2C)}$	Allowable load capacitance for each I²C Line				400	pF
$f_{SCL(fast)}$	Support SCL frequency	No wait states, fast mode			400	kHz
$f_{SCL(slow)}$	Support SCL frequency	No wait states, slow mode			100	kHz
V_{NH}	Noise margin at High level for each connected device (including hysteresis)		0.2 × V_{DAC_DVDD}			V
MCLK AND PLL SPECIFICATIONS						
D_{MCLK}	Allowable MCLK duty cycle		40%		60%	
f_{MCLK}	Supported MCLK frequencies	Up to 50 MHz	128		512	f_S (2)
f_{PLL}	PLL input frequency	Clock divider uses fractional divide D > 0, P = 1	6.7		20	MHz
		Clock divider uses integer divide D = 0, P = 1	1		20	
SERIAL AUDIO PORT						
t_{DLY}	Required LRCK/FS to SCLK rising edge delay		5			ns
D_{SCLK}	Allowable SCLK duty cycle		40%		60%	
f_S	Supported input sample rates		8		96	kHz
f_{SCLK}	Supported SCLK frequencies		32		64	f_S (2)
f_{SCLK}	SCLK frequency	Either master mode or slave mode			24.576	MHz

(1) DAC_DVDD referenced digital pins include: ADR, LRCK, MCLK, $\overline{\text{DAC\_MUTE}}$, SCL, SCLK, SDA, SDIN, SDOUT and XPU.
(2) A unit of f_S indicates that the specification is the value listed in the table multiplied by the sample rate of the audio used in the TAS3251 device.

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7.7 Audio Characteristics (BTL)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 600 kHz, R_{OC} = 22 kΩ, T_C= 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, MODE = 0, AES17 + AUX-0025 measurement filters, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 3 Ω, 10% THD+N		220		W
		R_L = 4 Ω, 10% THD+N		175		
		R_L = 3 Ω, 1% THD+N		175		
		R_L = 4 Ω, 1% THD+N		140		
THD+N	Total harmonic distortion + noise	1 W		0.008		%
V_n	Output integrated noise	A-weighted, AES17 filter, input capacitor grounded		95		µV
$\|V_{OS}\|$	Output offset voltage	Inputs AC coupled to GND		20	60	mV
SNR	Signal-to-noise ratio(1)			108		dB
DNR	Dynamic range			110		dB
P_{idle}	Power dissipation due to Idle losses (I_{PVDD_X})	P_O = 0, 4 channels switching(2)		0.75		W

(1) SNR is calculated relative to 1% THD+N outputlevel.
(2) Actual system idle losses also are affected by core losses of output inductors.

7.8 Audio Characteristics (PBTL)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 2 Ω, f_S = 600 kHz, R_{OC} = 22 kΩ, T_C= 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, MODE = 1, outputs paralleled after LC filter, AES17 + AUX-0025 measurement filters, unlessotherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 2 Ω, 10% THD+N		355		W
		R_L = 3 Ω, 10% THD+N		250		
		R_L = 4 Ω, 10% THD+N		195		
		R_L = 2 Ω, 1% THD+N		285		
		R_L = 3 Ω, 1% THD+N		200		
		R_L = 4 Ω, 1% THD+N		155		
THD+N	Total harmonic distortion + noise	1 W		0.009		%
V_n	Output integrated noise	A-weighted, AES17 filter, input capacitor grounded		95		µV
SNR	Signal to noise ratio(1)	A-weighted		108		dB
DNR	Dynamic range	A-weighted		108		dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0, 4 channels switching(2)		0.75		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses are affected by core losses of output inductors.

ADVANCE INFORMATION

7.9 MCLK Timing

See Figure 1.

PARAMETER		MIN	MAX	UNIT
t_{MCLK}	MCLK period	20	1000	ns
t_{MCLKH}	MCLK pulse width, high	9		ns
t_{MCLKL}	MCLK pulse width, low	9		ns

7.10 Serial Audio Port Timing – Slave Mode

See Figure 2.

PARAMETER		MIN	MAX	UNIT
f_{SCLK}	SCLK frequency	1.024		MHz
t_{SCLK}	SCLK period	40		ns
t_{SCLKL}	SCLK pulse width, low	16		ns
t_{SCLKH}	SCLK pulse width, high	16		ns
t_{SL}	SCLK rising to LRCK/FS edge	8		ns
t_{LS}	LRCK/FS Edge to SCLK rising edge	8		ns
t_{SU}	Data setup time, before SCLK rising edge	8		ns
t_{DH}	Data hold time, after SCLK rising edge	8		ns
t_{DFS}	Data delay time from SCLK falling edge		15	ns

7.11 Serial Audio Port Timing – Master Mode

See Figure 3.

PARAMETER		MIN	MAX	UNIT
t_{SCLK}	SCLK period	40		ns
t_{SCLKL}	SCLK pulse width, low	16		ns
t_{SCLKH}	SCLK pulse width, high	16		ns
t_{LRD}	LRCK/FS delay time from to SCLK falling edge	–10	20	ns
t_{SU}	Data setup time, before SCLK rising edge	8		ns
t_{DH}	Data hold time, after SCLK rising edge	8		ns
t_{DFS}	Data delay time from SCLK falling edge		15	ns

ADVANCE INFORMATION

7.12 I²C Bus Timing –Standard

		MIN	MAX	UNIT
f_{SCL}	SCL clock frequency		400	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7		µs
t_{LOW}	Low period of the SCL clock	4.7		µs
t_{HI}	High period of the SCL clock	4		µs
t_{RS-SU}	Setup time for (repeated) START condition	4.7		µs
t_{S-HD}	Hold time for (repeated) START condition	4		µs
t_{D-SU}	Data setup time	250		ns
t_{D-HD}	Data hold time	0	900	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$	1000	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$	1000	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$	1000	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$	1000	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$	1000	ns
t_{P-SU}	Setup time for STOP condition	4		µs

7.13 I²C Bus Timing –Fast

See Figure 4.

		MIN	MAX	UNIT
f_{SCL}	SCL clock frequency		400	kHz
t_{BUF}	Bus free time between a STOP and START condition	1.3		µs
t_{LOW}	Low period of the SCL clock	1.3		µs
t_{HI}	High period of the SCL clock	600		ns
t_{RS-SU}	Setup time for (repeated)START condition	600		ns
t_{RS-HD}	Hold time for (repeated)START condition	600		ns
t_{D-SU}	Data setup time	100		ns
t_{D-HD}	Data hold time	0	900	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$	300	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$	300	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$	300	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$	300	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$	300	ns
t_{P-SU}	Setup time for STOP condition	600		ns
t_{SP}	Pulse width of spike suppressed		50	ns

ADVANCE INFORMATION

7.14 Timing Diagrams

This section contains timing diagrams for I^2C and I^2S / TDM.

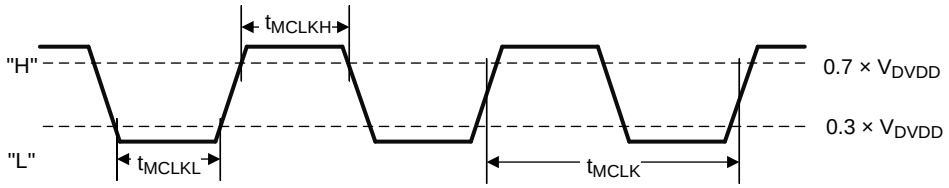


Figure 1. Timing Requirements for MCLK Input

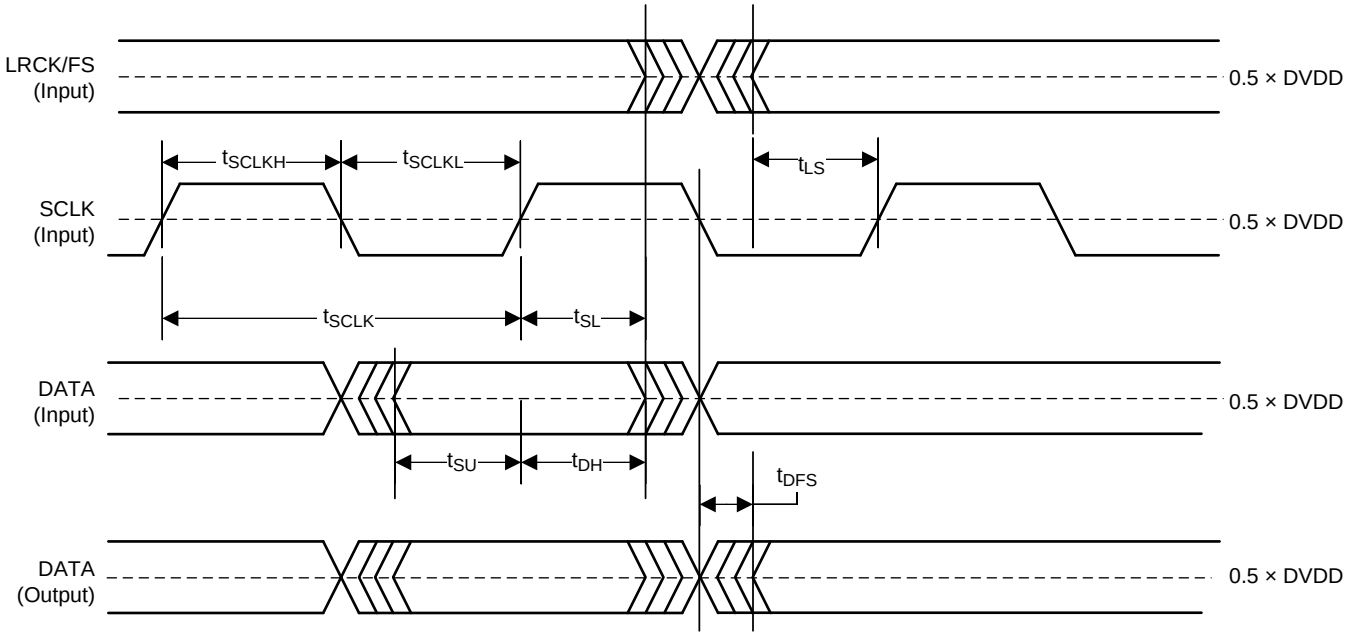


Figure 2. MCLK Timing Diagram in Slave Mode

ADVANCE INFORMATION

Timing Diagrams (continued)

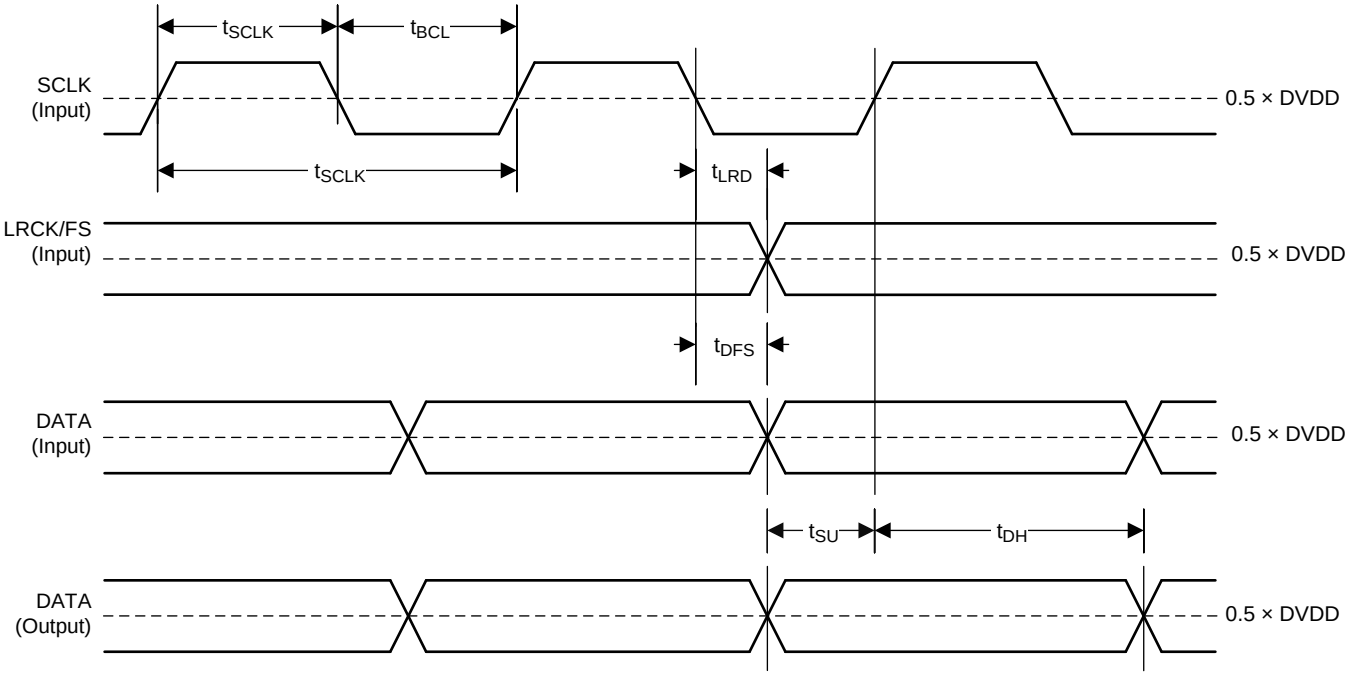


Figure 3. MCLK Timing Diagram in Master Mode

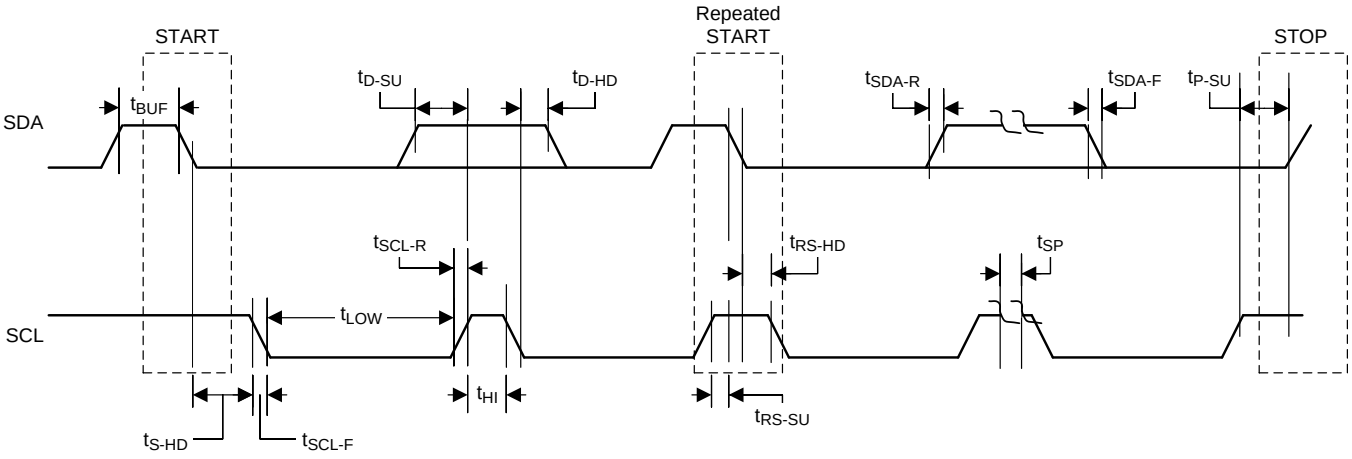
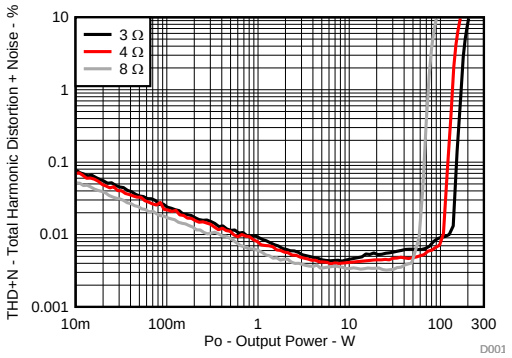


Figure 4. I²C Communication Port Timing Diagram

7.15 Typical Characteristics

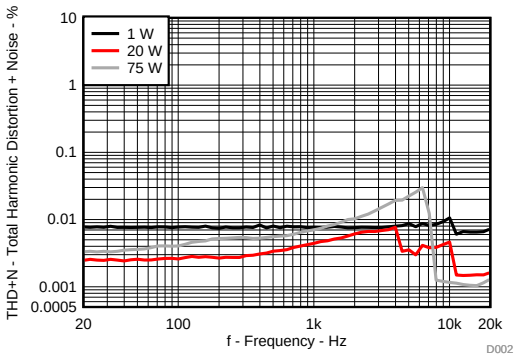
7.15.1 BTL Configuration

All Measurements taken at audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 600 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, MODE = 0, AES17 + AUX-0025 measurement filters, unless otherwise noted.



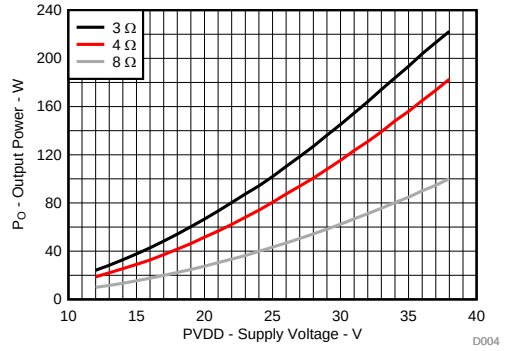
T_C = 75°C

Figure 5. Total Harmonic Distortion+Noise vs Output Power



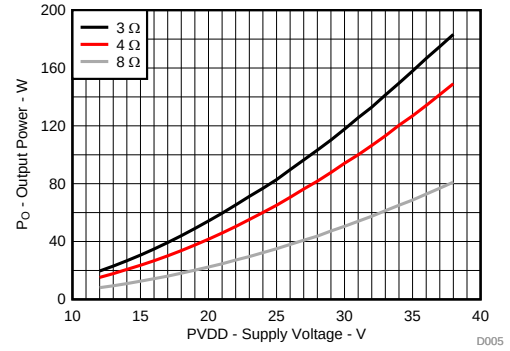
R_L = 4 Ω T_C = 75°C

Figure 6. Total Harmonic Distortion+Noise vs Frequency



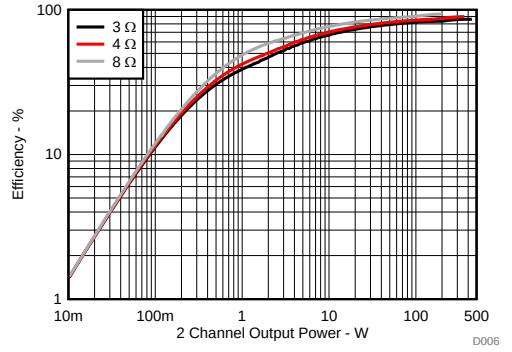
THD+N = 10% T_C = 75°C

Figure 7. Output Power vs Supply Voltage



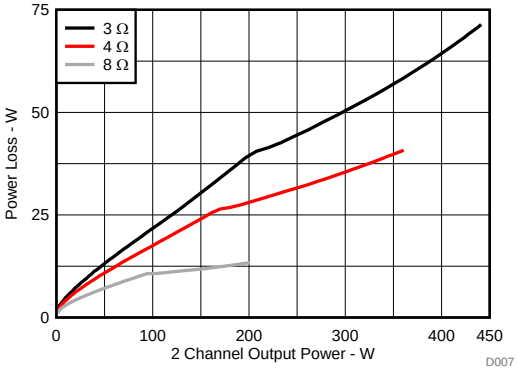
THD+N = 1% T_C = 75°C

Figure 8. Output Power vs Supply Voltage



T_C = 75°C

Figure 9. Efficiency vs Output Power

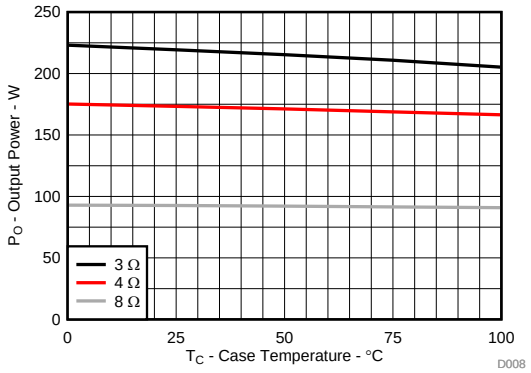


T_C = 75°C

Figure 10. Power Loss vs Output Power

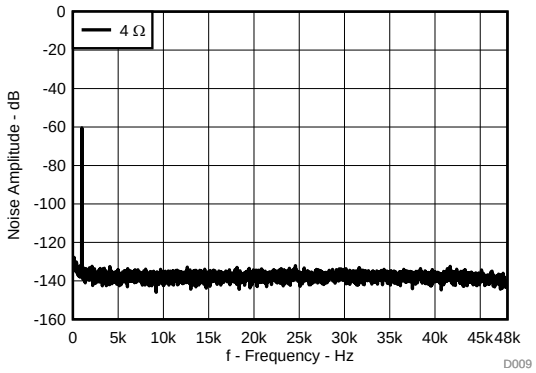
ADVANCE INFORMATION

BTL Configuration (continued)



THD+N = 10%

Figure 11. Output Power vs Temperature



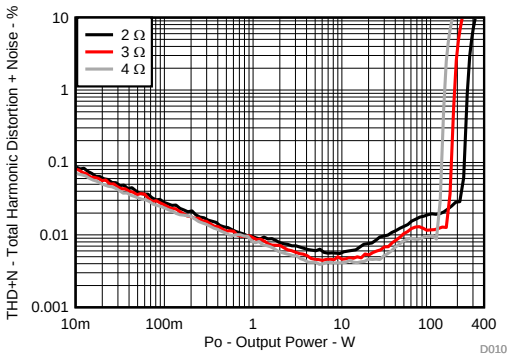
T_C = 75°C
AUX-0025 filter
V_{REF} = 25.46 V
FFT = 16384
80 kHz analyzer BW

Figure 12. Noise vs Frequency

ADVANCE INFORMATION

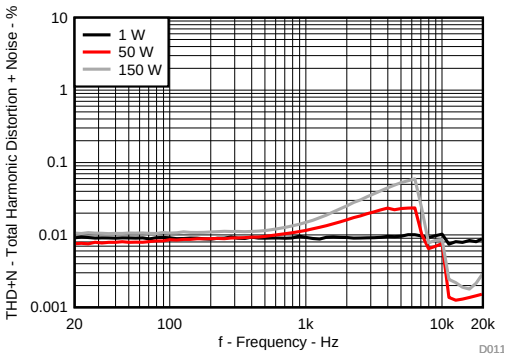
7.15.2 PBTL Configuration

All Measurements taken at audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 2 Ω, f_S = 600 kHz, R_{OC} = 22 kΩ, T_C = 75 °C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, MODE = 1, outputs paralleled after LC filter, AES17 + AUX-0025 measurement filters, unless otherwise noted.



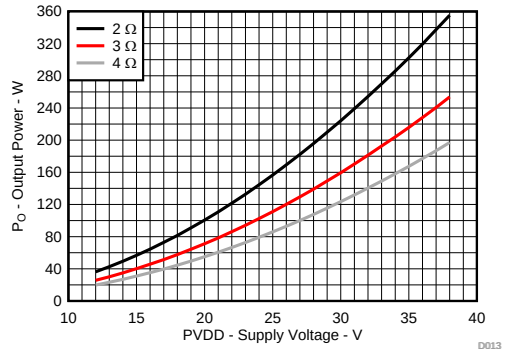
T_C = 75°C

Figure 13. Total Harmonic Distortion+Noise vs Output Power



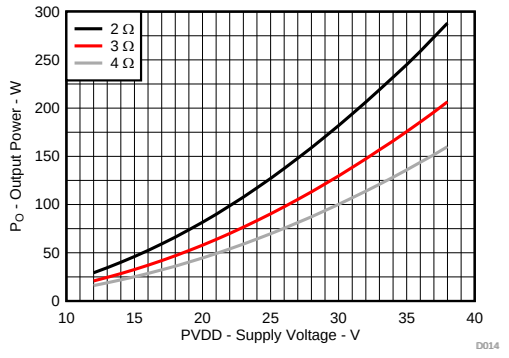
R_L = 3 Ω T_C = 75°C

Figure 14. Total Harmonic Distortion+Noise vs Frequency



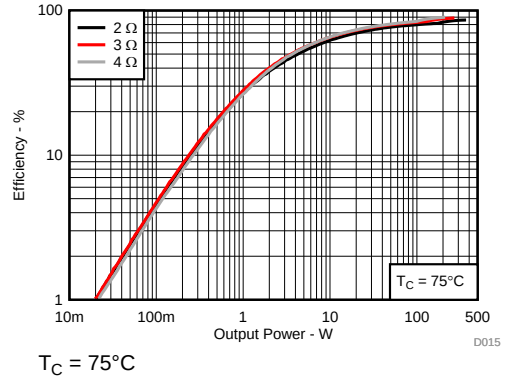
THD+N = 10% T_C = 75°C

Figure 15. Output Power vs Supply Voltage



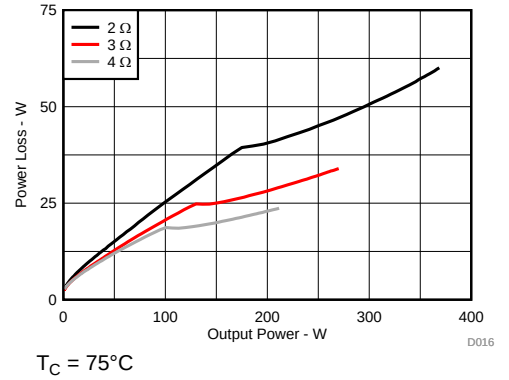
THD+N = 1% T_C = 75°C

Figure 16. Output Power vs Supply Voltage



T_C = 75°C

Figure 17. Efficiency vs Output Power

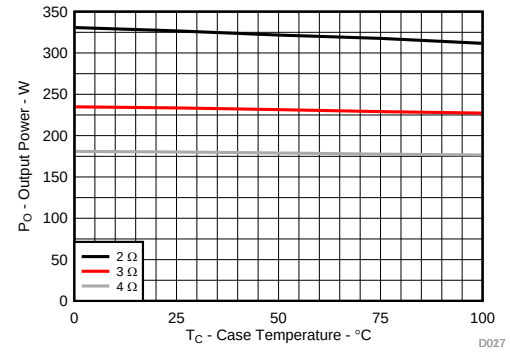


T_C = 75°C

Figure 18. Power Loss vs Output Power

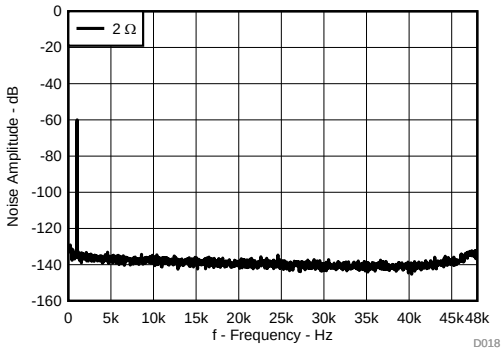
ADVANCE INFORMATION

PBTL Configuration (continued)



THD+N = 10%

Figure 19. Output Power vs Temperature



T_C = 75°C V_{REF} = 25.46 V FFT = 16384
AUX-0025 filter 80 kHz analyzer BW

Figure 20. Noise vs Frequency

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The TAS3251 device integrates four main building blocks into a single cohesive device that maximizes sound quality, flexibility, and ease of use. These include:

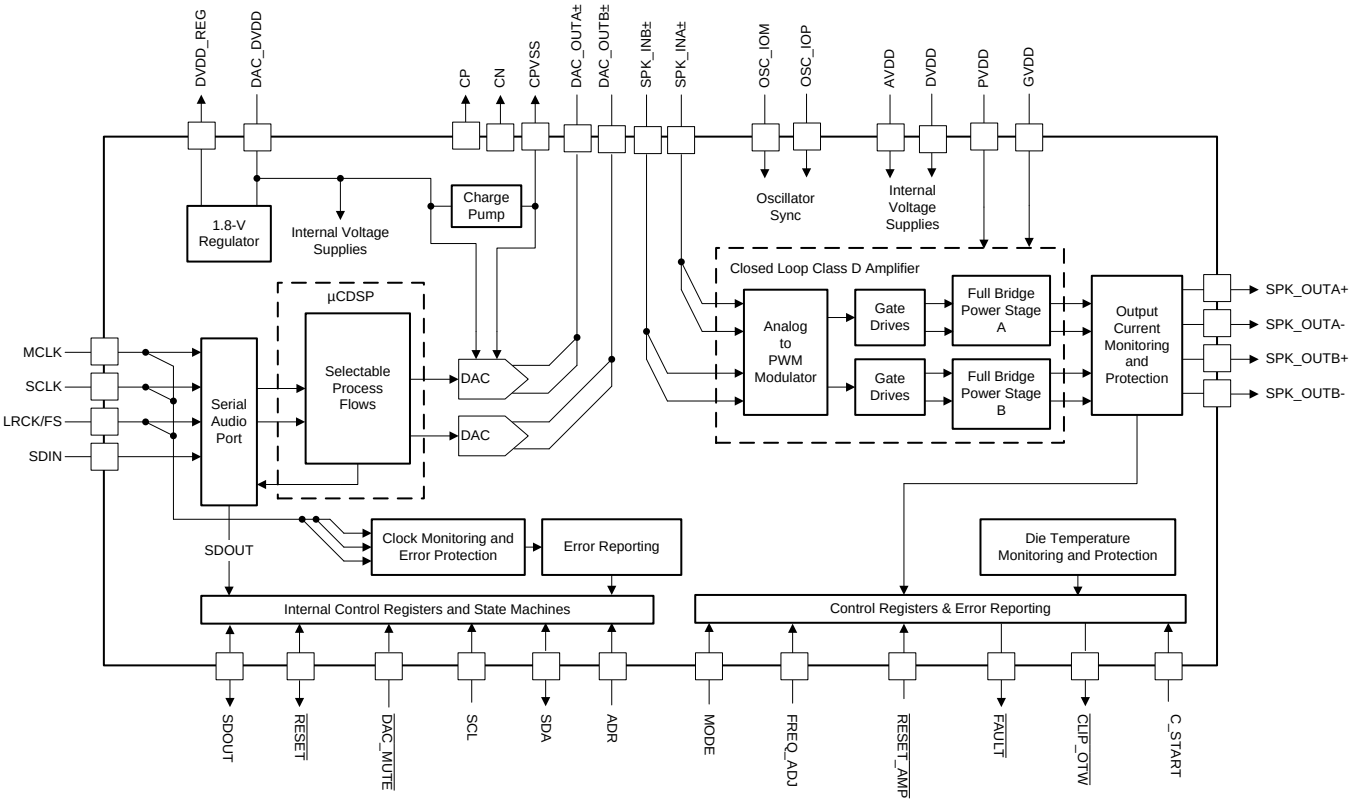
- Burr-Brown™ stereo audio DAC with a highly flexible serial audio port
- µCDSP, TI's latest audio processing core with a pre-programmed DSP audio process flows
- High-Performance, Ultra-HD Closed-loop Class-D amplifier capable of operating in stereo or mono
- An I^2C control port for communication and control of the device

The device requires three power supplies for proper operation. A 3.3 V rail for the low voltage circuitry and DAC, a 12 V rail for the amplifier gate-drive, and PVDD which is required to provide power to the output stage of the audio amplifier. The operating range for these supplies is shown in the *Recommended Operating Conditions*.

The communication and control interface for the device uses I^2C. A speaker amplifier fault output is also provided to notify a system controller of the occurrence of an overtemperature, overcurrent or undervoltage event.

The µCDSP audio processing core is pre-programmed with configurable DSP programs. The PurePath™ Console 3 software with the TAS3251 App available on TI.com provides the tools to control and tune the pre-programmed audio process flows.

8.2 Functional Block Diagram



ADVANCE INFORMATION

8.3 Feature Description

8.3.1 Power-on-Reset (POR) Function

The TAS3251 device has a power-on reset function. The power-on reset feature resets all of the registers to their default configuration as the device is powering up. When the low-voltage power supply used to power DVDD, AVDD, and CPVDD exceeds the POR threshold, the device sets all of the internal registers to their default values and holds them there until the device receives valid MCLK, SCLK, and LRCK/FS toggling for a period of approximately 4 ms. After the toggling period has passed, the internal reset of the registers is removed and the registers can be programmed via the I^2C Control Port.

8.3.2 Enable Device

To enable the device and play audio after power is applied write the following to the device over I2C. book 0x00, page 0x00, register 0x02 to 0x00. The following is a sample script for enabling the device:

```
w 90 00 00 # Go to page 0
w 90 7f 00 # Go to book 0
w 90 02 00 # Enable device
```

8.3.3 DAC and DSP Clocking

The TAS3251 front-end (DAC and DSP) has flexible systems for clocking. Internally, the device requires a number of clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface in one form or another. See section Oscillator for Output Power Stagefor setting the output stage oscillator and switching frequency.

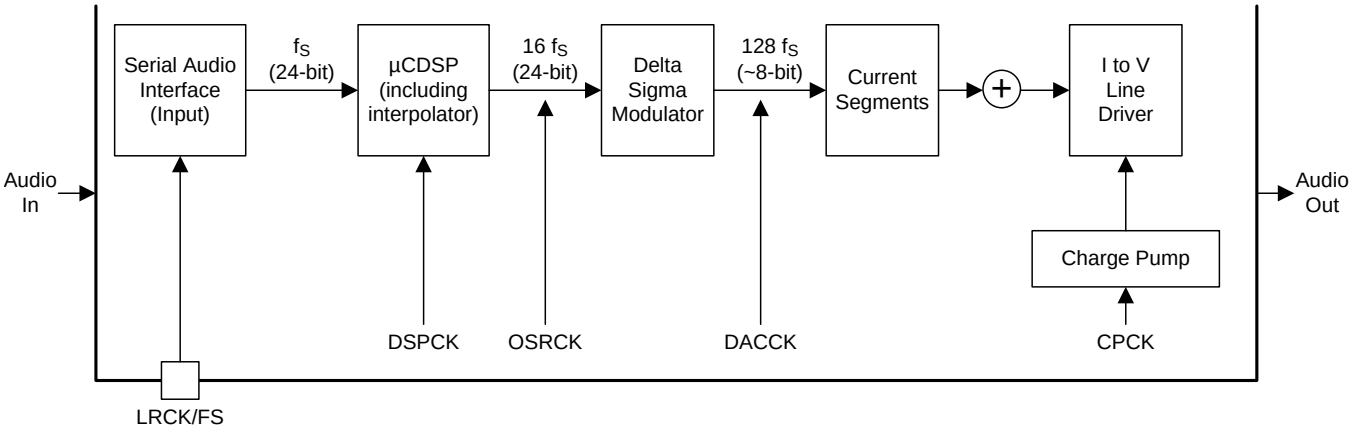


Figure 21. Audio Flow with Respective Clocks

Figure 21 shows the basic data flow at basic sample rate (f_S). When the data is brought into the serial audio interface, the data is processed, interpolated and modulated to 128 × f_S before arriving at the current segments for the final digital to analog conversion.

Figure 22 shows the clock tree.

ADVANCE INFORMATION

Feature Description (continued)

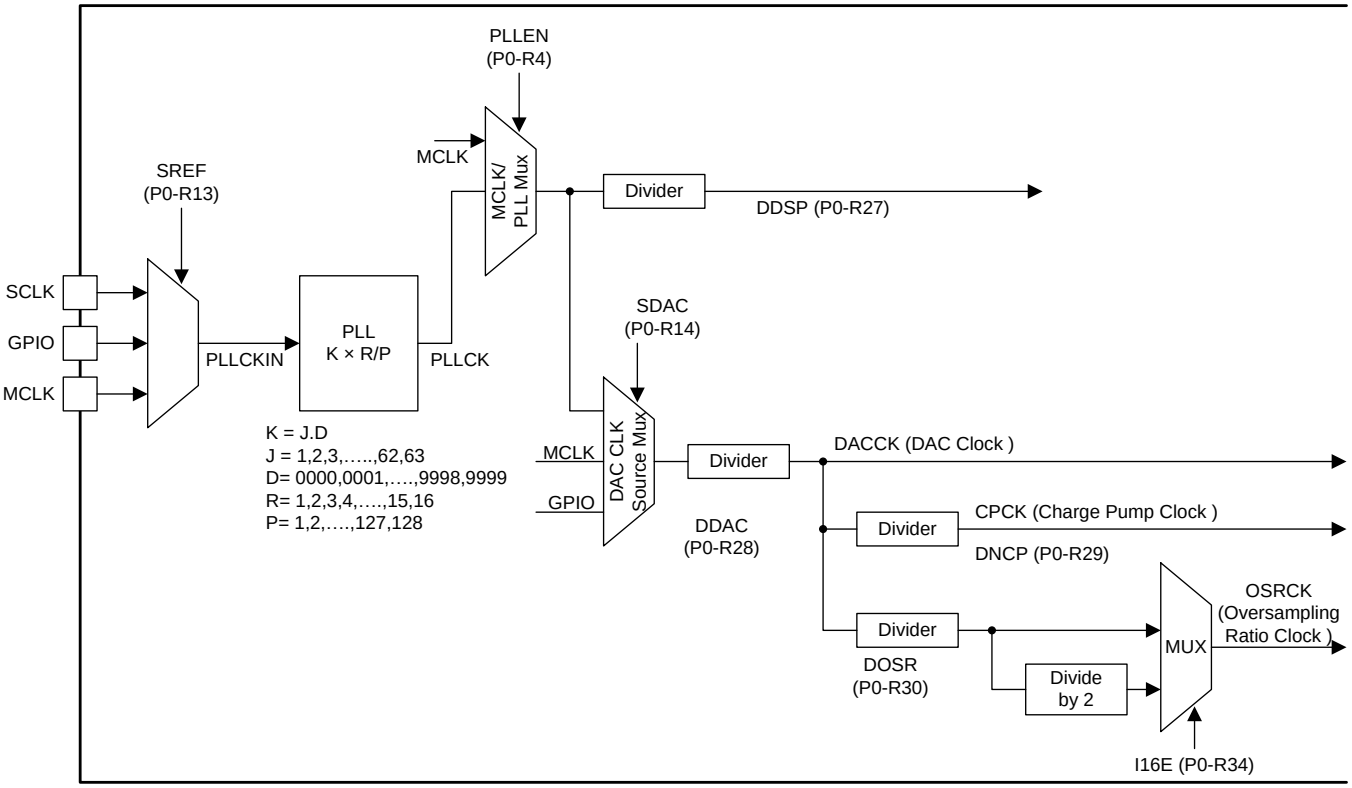


Figure 22. TAS3251 Clock Distribution Tree

The Serial Audio Interface typically has 4 connection pins which are listed as follows:

- MCLK (System Master Clock)
- SCLK (Serial or Bit Clock)
- LRCK/FS (Left-Right Word Clock and Frame Sync)
- SDIN (Input Data)
- SDOUT can be used to output pre- or post-processed DSP data for use externally (See the *SDOUT Port and Hardware Control Pins* section)

The device has an internal PLL that is used to take either MCLK or SCLK and create the higher rate clocks required by the DSP and the DAC clock.

In situations where the highest audio performance is required, bringing MCLK to the device along with SCLK and LRCK/FS is recommended. The device should be configured so that the PLL is only providing a clock source to the DSP. All other clocks are then a division of the incoming MCLK. To enable the MCLK as the main source clock, with all others being created as divisions of the incoming MCLK, set the DAC CLK source mux (SDAC in Figure 22) to use MCLK as a source, rather than the output of the MCLK/PLL mux.

8.3.3.1 Internal Clock Error Notification (CLKE)

When a clock error is detected on the incoming data clock, the TAS3251 device switches to an internal oscillator and continues to the drive the DAC, while attenuating the data from the last known value. Once this process is complete, the DAC outputs will be hard muted to the ground and the Class-D PWM output will stop switching. The clock error can be monitored at B0-P0-R94 and R95. The clock error status bits are non-latching, except for MCLK halted B0-P0-R95-D[4] which is cleared when read.

ADVANCE INFORMATION

Feature Description (continued)

8.3.4 Serial Audio Port

8.3.4.1 Clock Master Mode from Audio Rate Master Clock

In Master Mode, the device generates bit clock and left-right and frame sync clock and outputs them on the appropriate pins. To configure the device in master mode, first put the device into reset, then use registers SCLKO and LRKO (P0-R9). Then reset the LRCK/FS and SCLK divider counters using bits RSCLK and RLRK (P0-R12). Finally, exit reset.

Figure 23 shows a simplified serial port clock tree for the device in master mode.

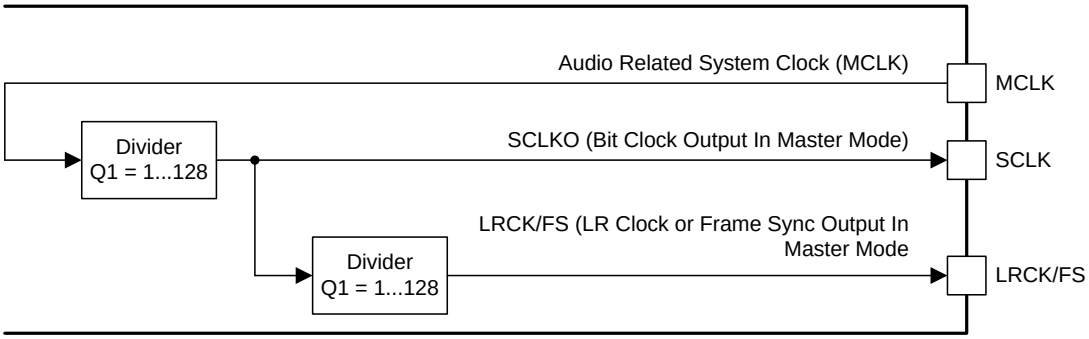


Figure 23. Simplified Clock Tree for MCLK Sourced Master Mode

In master mode, MCLK is an input and SCLK and LRCK/FS are outputs. SCLK and LRCK/FS are integer divisions of MCLK. Master mode with a non-audio rate master clock source requires external GPIO's to use the PLL in standalone mode. The PLL should be configured to ensure that the on-chip processor can be driven at the maximum clock rate. The master mode of operation is described in the section.

When used with audio rate master clocks, the register changes that should be done include switching the device into master mode, and setting the divider ratio. An example of the master mode of operations is using 24.576 MHz MCLK as a master clock source and driving the SCLK and LRCK/FS with integer dividers to create 48 kHz sample rate clock output. In master mode, the DAC section of the device is also running from the PLL output. The TAS3251 device is able to meet the specified audio performance while using the internal PLL. However, using the MCLK CMOS oscillator source will have less jitter than the PLL.

To switch the DAC clocks (SDAC in the Figure 22) the following registers should be modified

- Clock Tree Flex Mode (P253-R63 and P253-R64)
- DAC and OSR Source Clock Register (P0-R14). Set to 0x30 (MCLK input, and OSR is set to whatever the DAC source is)
- The DAC clock divider should be 16 f_S.
  - 16 × 48 kHz = 768 kHz
  - 24.576 MHz (MCLK in) / 768 kHz = 32
  - Therefore, the divide ratio for register DDAC (P0-R28) should be set to 32. The register mapping gives 0x00 = 1, therefore 32 must be converter to 0x1F (31dec).

8.3.4.2 Clock Slave Mode with 4-Wire Operation (SCLK, MCLK, LRCK/FS, SDIN)

The TAS3251 device requires a system clock to operate the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the MCLK input and supports up to 50 MHz. The TAS3251 device system-clock detection circuit automatically senses the system-clock frequency. Common audio sampling frequencies in the bands of 32 kHz, (44.1 – 48 kHz), (88.2 – 96 kHz) are supported.

NOTE

Values in the parentheses are grouped when detected, for example, 88.2 kHz and 96 kHz are detected as *double rate*, 32 kHz, 44.1 kHz and 48 kHz are detected as *single rate* and so on.

ADVANCE INFORMATION

Feature Description (continued)

In the presence of a valid bit MCLK, SCLK and LRCK/FS, the device automatically configures the clock tree and PLL to drive the miniDSP as required.

The sampling frequency detector sets the clock for the digital filter, Delta Sigma Modulator (DSM) and the Negative Charge Pump (NCP) automatically. Table 3 shows examples of system clock frequencies for common audio sampling rates.

MCLK rates that are not common to standard audio clocks, between 1 MHz and 50 MHz, are supported by configuring various PLL and clock-divider registers directly. In slave mode, auto clock mode should be disabled using P0-R37. Additionally, the user can be required to ignore clock error detection if external clocks are not available for some time during configuration, or if the clocks presented on the pins of the device are invalid. The extended programmability allows the device to operate in an advanced mode in which the device becomes a clock master and drive the host serial port with LRCK/FS and SCLK, from a non-audio related clock (for example, using a setting of 12 MHz to generate 44.1 kHz [LRCK/FS] and 2.8224 MHz [SCLK]).

Table 3 shows the timing requirements for the system clock input. For optimal performance, use a clock source with low phase jitter and noise. For MCLK timing requirements, refer to the *Serial Audio Port Timing – Master Mode* section.

Table 3. System Master Clock Inputs for Audio Related Clocks

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{MCLK}) (MHz)					
	64 f_S	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S
8 kHz	See	1.024	1.536	2.048	3.072	4.096
16 kHz		2.048	3.072	4.096	6.144	8.192
32 kHz		4.096	6.144	8.192	12.288	16.384
44.1 kHz		5.6488	8.4672	11.2896	16.9344	22.5792
48 kHz		6.144	9.216	12.288	18.432	24.576
88.2 kHz		11.2896	16.9344	22.5792	33.8688	45.1584
96 kHz		12.288	18.432	24.576	36.864	49.152

8.3.4.3 Clock Slave Mode with SCLK PLL to Generate Internal Clocks (3-Wire PCM)

8.3.4.3.1 Clock Generation Using the PLL

The TAS3251 device supports a wide range of options to generate the required clocks as shown in Figure 22.

The clocks for the PLL require a source reference clock. This clock is sourced as the incoming SCLK or MCLK, a GPIO can also be used.

The source reference clock for the PLL reference clock is selected by programming the SRCREF value on P0-R13, D[6:4]. The TAS3251 device provides several programmable clock dividers to achieve a variety of sampling rates. See Figure 22.

If PLL functionality is not required, set the PLLEN value on P0-R4, D[0] to 0. In this situation, an external master clock is required.

Table 4. PLL Configuration Registers

CLOCK MULTIPLEXER		
REGISTER	FUNCTION	BITS
SREF	PLL Reference	B0-P0-R13-D[6:4]
DDSP	clock divider	B0-P0-R27-D[6:0]
DSCLK	External SCLK Div	B0-P0-R32-D[6:0]
DLRK	External LRCK/FS Div	B0-P0-R33-D[7:0]

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8.3.4.3.2 PLL Calculation

The TAS3251 device has an on-chip PLL with fractional multiplication to generate the clock frequency required by the Digital Signal Processing blocks. The programmability of the PLL allows operation from a wide variety of clocks that may be available in the system. The PLL input (PLLCKIN) supports clock frequencies from 1 MHz to 50 MHz and is register programmable to enable generation of required sampling rates with fine precision.

The PLL is enabled by default. The PLL can be enabled by writing to P0-R4, D[0]. When the PLL is enabled, the PLL output clock PLLCK is given by Equation 1:

$$PLLCK = \frac{PLLCKIN \times R \times J.D}{P} \quad \text{or} \quad PLLCK = \frac{PLLCKIN \times R \times K}{P} \tag{1}$$

where

- R = 1, 2, 3,4, ... , 15, 16
- J = 4,5,6, . . . 63, and D = 0000, 0001, 0002, . . . 9999
- K = [J value].[D value]
- P = 1, 2, 3, ... 15

R, J, D, and P are programmable. J is the integer portion of K (the numbers to the left of the decimal point), while D is the fractional portion of K (the numbers to the right of the decimal point, assuming four digits of precision).

8.3.4.3.2.1 Examples:

- If K = 8.5, then J = 8, D = 5000
- If K = 7.12, then J = 7, D = 1200
- If K = 14.03, then J = 14, D = 0300
- If K = 6.0004, then J = 6, D = 0004

When the PLL is enabled and D = 0000, **the following conditions must be satisfied:**

- 1 MHz ≤ (PLLCKIN / P) ≤ 20 MHz
- 64 MHz ≤ (PLLCKIN x K x R / P) ≤ 100 MHz
- 1 ≤ J ≤ 63

When the PLL is enabled and D ≠ 0000, **the following conditions must be satisfied:**

- 6.667 MHz ≤ PLLCLKIN / P ≤ 20 MHz
- 64 MHz ≤ (PLLCKIN x K x R / P) ≤ 100 MHz
- 4 ≤ J ≤ 11
- R = 1

When the PLL is enabled,

- f_S = (PLLCLKIN × K × R) / (2048 × P)
- The value of N is selected so that f_S × N = PLLCLKIN x K x R / P is in the allowable range.

Example: MCLK = 12 MHz and f_S = 44.1 kHz, (N=2048)
Select P = 1, R = 1, K = 7.5264, which results in J = 7, D = 5264

Example: MCLK = 12 MHz and f_S = 48.0 kHz, (N=2048)
Select P = 1, R = 1, K = 8.192, which results in J = 8, D = 1920

Values are written to the registers in Table 5.

Table 5. PLL Registers

DIVIDER	FUNCTION	BITS
PLLE	PLL enable	P0-R4, [0]
PPDV	PLL P	P0-R20, [3:0]
PJDV	PLL J	P0-R21, [5:0]
PDDV	PLL D	P0-R22, [5:0]
		P0-R23, [7:0]
PRDV	PLL R	P0-R24, [3:0]

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Table 6. PLL Configuration Recommendations

EQUATIONS	DESCRIPTION
f_S (kHz)	Sampling frequency
R_{MCLK}	Ratio between sampling frequency and MCLK frequency (MCLK frequency = RMCLK x sampling frequency)
MCLK (MHz)	System master clock frequency at MCLK input (pin 20)
PLL VCO (MHz)	PLL VCO frequency as PLLCK in Figure 22
P	One of the PLL coefficients in Equation 1
PLL REF (MHz)	Internal reference clock frequency which is produced by MCLK / P
M = K × R	The final PLL multiplication factor computed from K and R as described in Equation 1
K = J.D	One of the PLL coefficients in Equation 1
R	One of the PLL coefficients in Equation 1
PLL f_S	Ratio between f_S and PLL VCO frequency (PLL VCO / f_S)
DSP f_S	Ratio between operating clock rate and f_S (PLL f_S / NMAC)
NMAC	The clock divider value in Table 4
DSP CLK (MHz)	The operating frequency as DSPCK in Figure 22
MOD f_S	Ratio between DAC operating clock frequency and f_S (PLL f_S / NDAC)
MOD f (kHz)	DAC operating frequency as DACCK in
NDAC	DAC clock divider value in Table 4
DOSR	OSR clock divider value in Table 4 for generating OSRCK in Figure 22. DOSR must be chosen so that MOD f_S / DOSR = 16 for correct operation.
NCP	NCP (negative charge pump) clock divider value in Table 4
CP f	Negative charge pump clock frequency (f_S × MOD f_S / NCP)
% Error	Percentage of error between PLL VCO / PLL f_S and f_S (mismatch error). • This value is typically zero but can be non-zero especially when K is not an integer (D is not zero). • This value can be non-zero only when the TAS3251 device acts as a master.

The previous equations explain how to calculate all necessary coefficients and controls to configure the PLL. Table 7 provides for easy reference to the recommended clock divider settings for the PLL as a Master Clock.

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Table 7. Recommended Clock Divider Settings for PLL as Master Clock

f_S (kHz)	R_{MCLK}	MCLK (MHz)	PLL VCO (MHz)	P	PLL REF (MHz)	M = K×R	K = J×D	R	PLL f_S	DSP f_S	NMAC	DSP CLK (MHz)	MOD f_S	MOD f (kHz)	NDAC	DOSR	% ERROR	NCP	CP f (kHz)
8	128	1.024	98.304	1	1.024	96	48	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	192	1.536	98.304	1	1.536	64	32	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	256	2.048	98.304	1	2.048	48	48	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	384	3.072	98.304	3	1.024	96	48	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	512	4.096	98.304	3	1.365	72	36	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	768	6.144	98.304	3	2.048	48	48	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	1024	8.192	98.304	3	2.731	36	36	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	1152	9.216	98.304	9	1.024	96	48	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	1536	12.288	98.304	9	1.365	72	36	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	2048	16.384	98.304	9	1.82	54	54	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
	3072	24.576	98.304	9	2.731	36	36	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
11.025	128	1.4112	90.3168	1	1.411	64	32	2	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	192	2.1168	90.3168	3	0.706	128	32	4	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	256	2.8224	90.3168	1	2.822	32	32	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	384	4.2336	90.3168	3	1.411	64	32	2	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	512	5.6448	90.3168	3	1.882	48	48	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	768	8.4672	90.3168	3	2.822	32	32	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	1024	11.2896	90.3168	3	3.763	24	24	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	1152	12.7008	90.3168	9	1.411	64	32	2	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	1536	16.9344	90.3168	9	1.882	48	48	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	2048	22.5792	90.3168	9	2.509	36	36	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
	3072	33.8688	90.3168	9	3.763	24	24	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
16	64	1.024	98.304	1	1.024	96	48	2	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	128	2.048	98.304	1	2.048	48	48	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	192	3.072	98.304	1	3.072	32	32	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	256	4.096	98.304	1	4.096	24	24	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	384	6.144	98.304	3	2.048	48	48	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	512	8.192	98.304	3	2.731	36	36	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	768	12.288	98.304	3	4.096	24	24	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	1024	16.384	98.304	3	5.461	18	18	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	1152	18.432	98.304	3	6.144	16	16	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	1536	24.576	98.304	9	2.731	36	36	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	2048	32.768	98.304	9	3.641	27	27	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
	3072	49.152	98.304	9	5.461	18	18	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536

Table 7. Recommended Clock Divider Settings for PLL as Master Clock (continued)

f_S (kHz)	R_{MCLK}	MCLK (MHz)	PLL VCO (MHz)	P	PLL REF (MHz)	M = K×R	K = J×D	R	PLL f_S	DSP f_S	NMAC	DSP CLK (MHz)	MOD f_S	MOD f (kHz)	NDAC	DOSR	% ERROR	NCP	CP f (kHz)
22.05	64	1.4112	90.3168	1	1.411	64	32	2	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	128	2.8224	90.3168	1	2.822	32	32	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	192	4.2336	90.3168	3	1.411	64	32	2	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	256	5.6448	90.3168	1	5.645	16	16	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	384	8.4672	90.3168	3	2.822	32	32	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	512	11.2896	90.3168	3	3.763	24	24	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	768	16.9344	90.3168	3	5.645	16	16	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	1024	22.5792	90.3168	3	7.526	12	12	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	1152	25.4016	90.3168	9	2.822	32	32	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	1536	33.8688	90.3168	9	3.763	24	24	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
	2048	45.1584	90.3168	9	5.018	18	18	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
32	32	1.024	98.304	1	1.024	96	48	2	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	48	1.536	98.304	1	1.536	64	16	4	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	64	2.048	98.304	1	2.048	48	24	2	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	128	4.096	98.304	1	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	192	6.144	98.304	3	2.048	48	48	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	256	8.192	98.304	2	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	384	12.288	98.304	3	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	512	16.384	98.304	3	5.461	18	18	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	768	24.576	98.304	3	8.192	12	12	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	1024	32.768	98.304	3	10.923	9	9	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	1152	36.864	98.304	9	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
	1536	49.152	98.304	6	8.192	12	12	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
44.1	32	1.4112	90.3168	1	1.411	64	32	2	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	64	2.8224	90.3168	1	2.822	32	16	2	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	128	5.6448	90.3168	1	5.645	16	16	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	192	8.4672	90.3168	3	2.822	32	32	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	256	11.2896	90.3168	2	5.645	16	16	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	384	16.9344	90.3168	3	5.645	16	16	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	512	22.5792	90.3168	3	7.526	12	12	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	768	33.8688	90.3168	3	11.29	8	8	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
	1024	45.1584	90.3168	3	15.053	6	6	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2

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Table 7. Recommended Clock Divider Settings for PLL as Master Clock (continued)

f_S (kHz)	R_{MCLK}	MCLK (MHz)	PLL VCO (MHz)	P	PLL REF (MHz)	M = K×R	K = J×D	R	PLL f_S	DSP f_S	NMAC	DSP CLK (MHz)	MOD f_S	MOD f (kHz)	NDAC	DOSR	% ERROR	NCP	CP f (kHz)
48	32	1.536	98.304	1	1.536	64	32	2	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	64	3.072	98.304	1	3.072	32	16	2	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	128	6.144	98.304	1	6.144	16	16	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	192	9.216	98.304	3	3.072	32	32	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	256	12.288	98.304	2	6.144	16	16	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	384	18.432	98.304	3	6.144	16	16	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	512	24.576	98.304	3	8.192	12	12	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	768	36.864	98.304	3	12.288	8	8	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
	1024	49.152	98.304	3	16.384	6	6	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
96	32	3.072	98.304	1	3.072	32	16	2	1024	512	2	49.152	64	6144	16	4	0	4	1536
	48	4.608	98.304	3	1.536	64	32	2	1024	512	2	49.152	64	6144	16	4	0	4	1536
	64	6.144	98.304	1	6.144	16	8	2	1024	512	2	49.152	64	6144	16	4	0	4	1536
	128	12.288	98.304	2	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
	192	18.432	98.304	3	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
	256	24.576	98.304	4	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
	384	36.864	98.304	6	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
	512	49.152	98.304	8	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536

8.3.4.4 Serial Audio Port – Data Formats and Bit Depths

The serial audio interface port is a 3-wire serial port with the signals LRCK/FS (pin 25), SCLK (pin 23), and SDIN (pin 24). SCLK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio interface. Serial data is clocked into the TAS3251 device on the rising edge of SCLK.The LRCK/FS pin is the serial audio left/right word clock or frame sync when the device is operated in TDM Mode.

Table 8. TAS3251 device Audio Data Formats, Bit Depths and Clock Rates

FORMAT	DATA BITS	MAXIMUM LRCK/FS FREQUENCY (kHz)	MCLK RATE (f_S)	SCLK RATE (f_S)
I^2S/LJ/RJ	32, 24, 20, 16	Up to 96	128 to 3072 (≤ 50 MHz)	64, 48, 32
TDM/DSP	32, 24, 20, 16	Up to 48	128 to 3072	125, 256
		96	128 to 512	125, 256

The TAS3251 device requires the synchronization of LRCK/FS and system clock, but does not require a specific phase relation between LRCK/FS and system clock.

If the relationship between LRCK/FS and system clock changes more than ±5 MCLK, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until re-synchronization between LRCK/FS and system clock is completed.

If the relationship between LRCK/FS and SCLK are invalid more than 4 LRCK/FS periods, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until re-synchronization between LRCK/FS and SCLK is completed.

8.3.4.4.1 Data Formats and Master/Slave Modes of Operation

The TAS3251 device supports industry-standard audio data formats, including standard I^2S and left-justified. Data formats are selected via Register (P0-R40). All formats require binary two's complement, MSB-first audio data; up to 32-bit audio data is accepted. The data formats are detailed in Figure 24 through Figure 29.

The TAS3251 device also supports right-justified and TDM/DSP data. I^2S, LJ, RJ, and TDM/DSP are selected using Register (P0-R40). All formats require binary 2s complement, MSB-first audio data. Up to 32 bits are accepted. Default setting is I^2S and 24 bit word length. The I^2S slave timing is shown in Figure 3.

shows a detailed timing diagram for the serial audio interface.

In addition to acting as a I^2S slave, the TAS3251 device can act as an I^2S master, by generating SCLK and LRCK/FS as outputs from the MCLK input. Table 9 lists the registers used to place the device into Master or Slave mode. Please refer to the *Serial Audio Port Timing – Master Mode* section for serial audio Interface timing requirements in Master Mode. For Slave Mode timing, please refer to to the *Serial Audio Port Timing – Slave Mode* section.

Table 9. I^2S Master Mode Registers

REGISTER	FUNCTION
P0-R9-B0, B4, and B5	I^2S Master mode select
P0-R32-D[6:0]	SCLK divider and LRCK/FS divider
P0-R33-D[7:0]	

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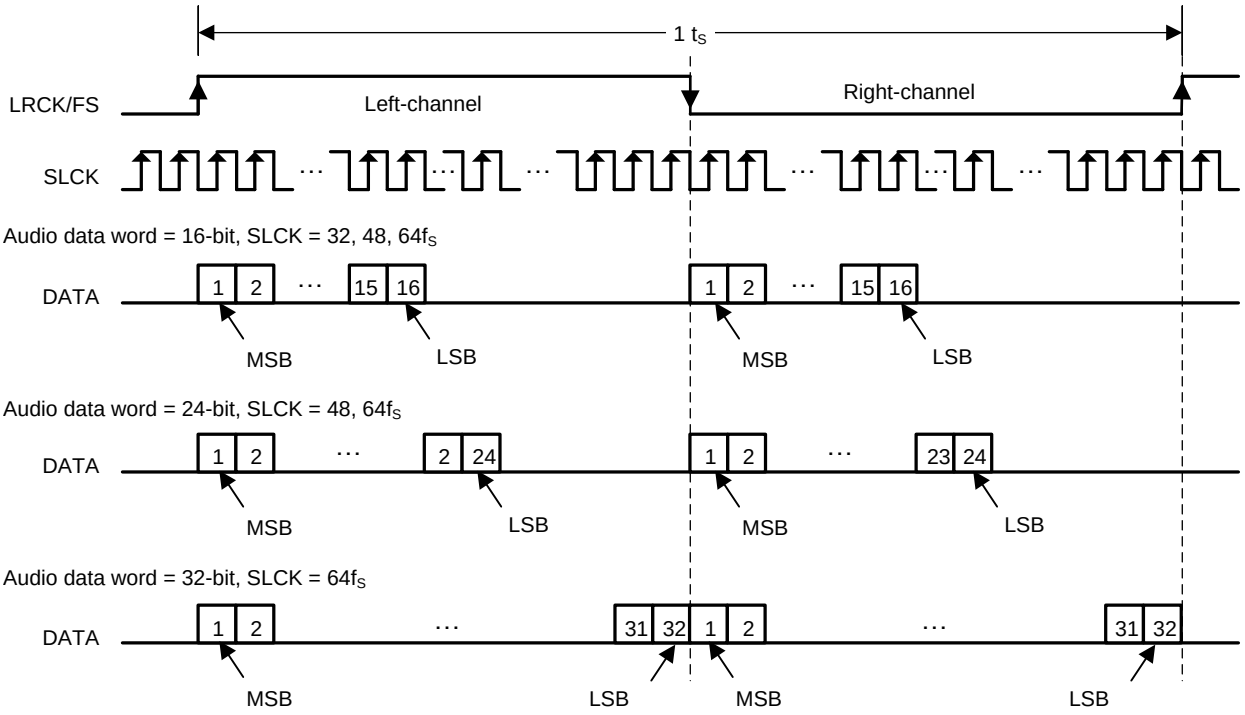
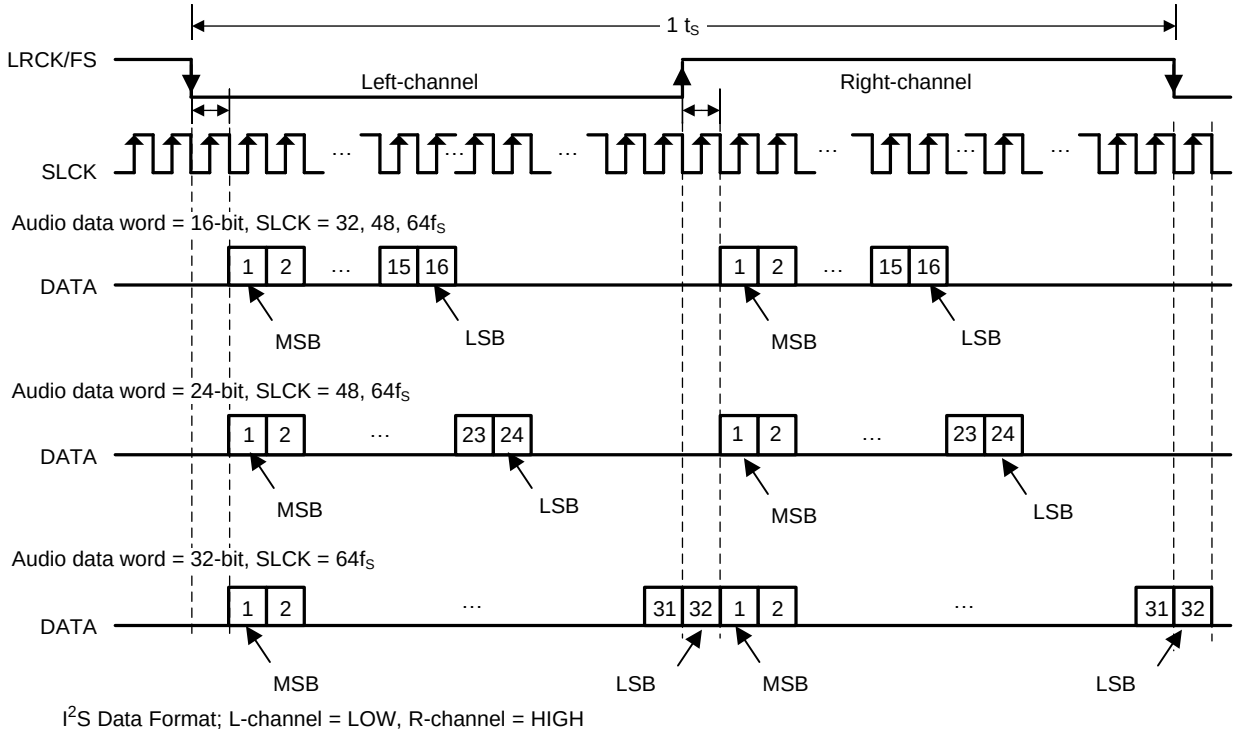
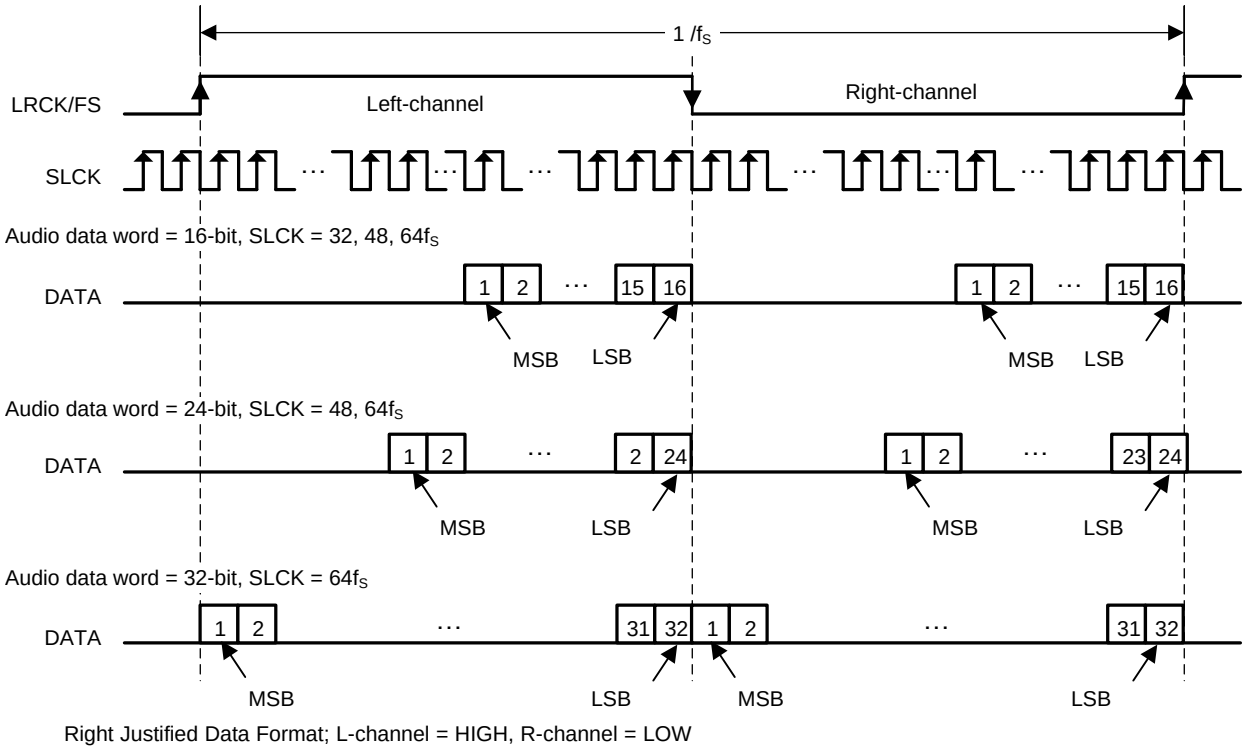


Figure 24. Left Justified Audio Data Format



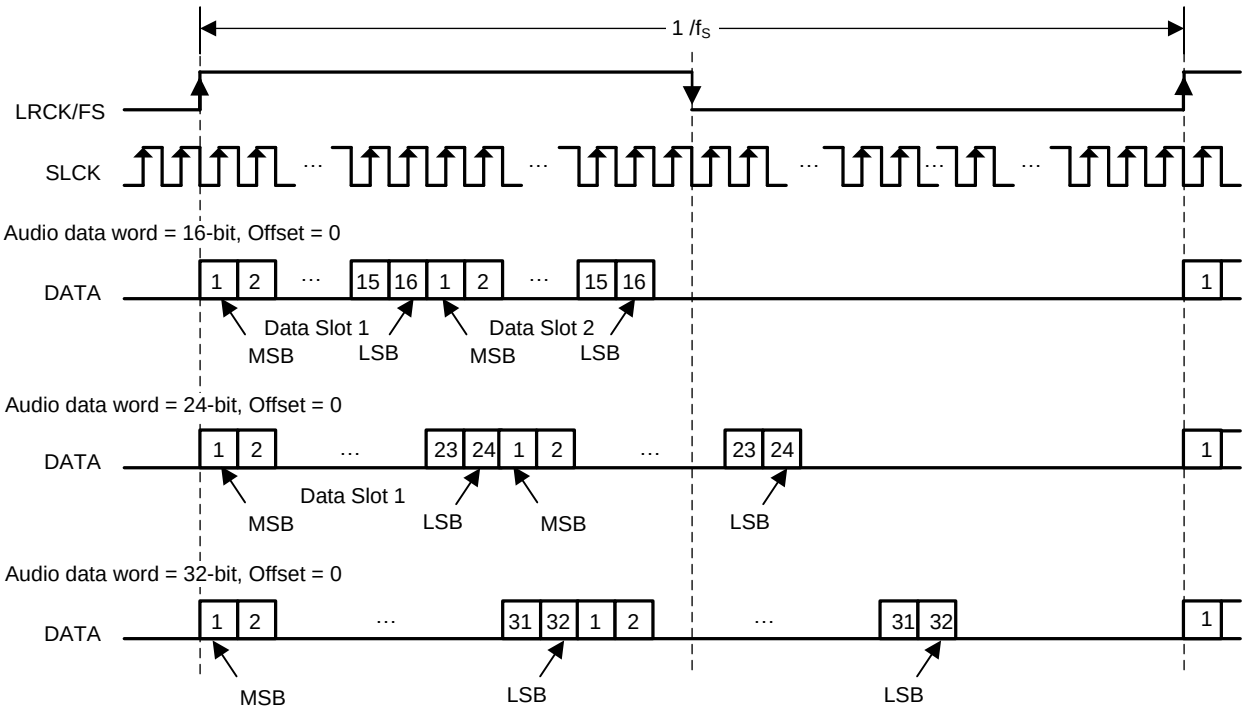
I^2S Data Format; L-channel = LOW, R-channel = HIGH

Figure 25. I^2S Audio Data Format



Right Justified Data Format; L-channel = HIGH, R-channel = LOW

Figure 26. Right Justified Audio Data Format



TDM/DSP Data Format with OFFSET = 0

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

Figure 27. TDM/DSP 1 Audio Data Format

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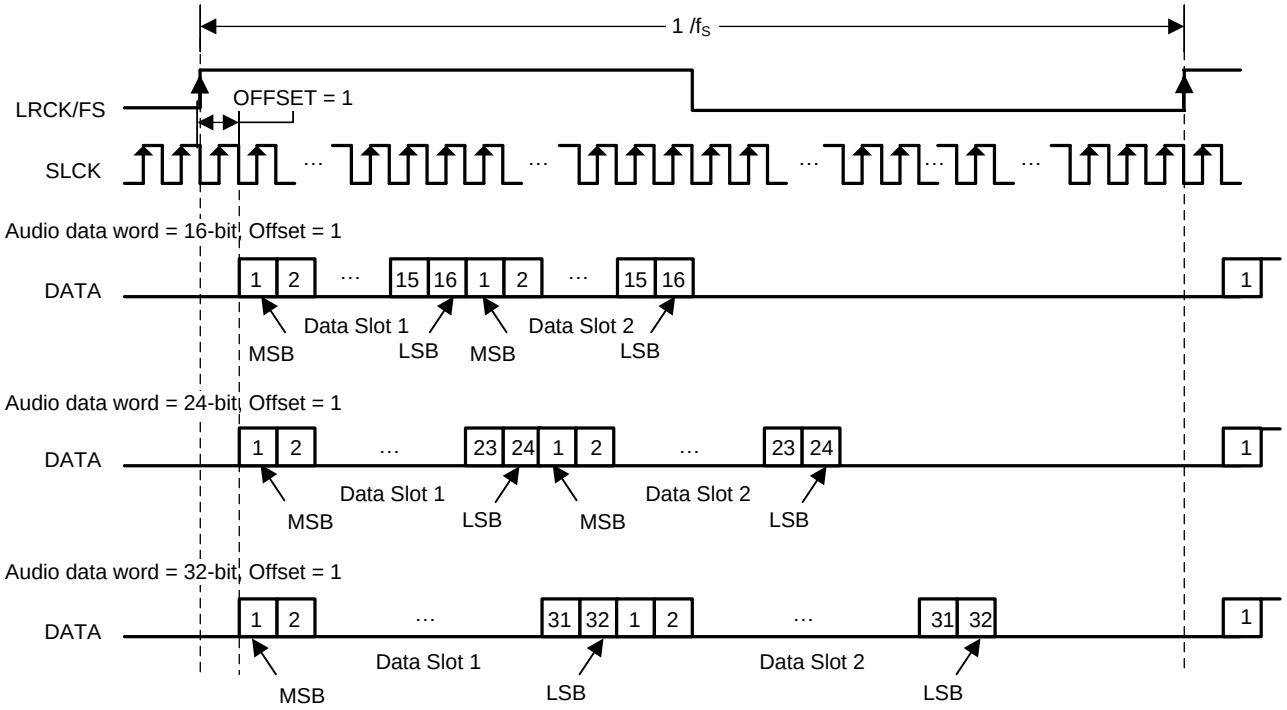
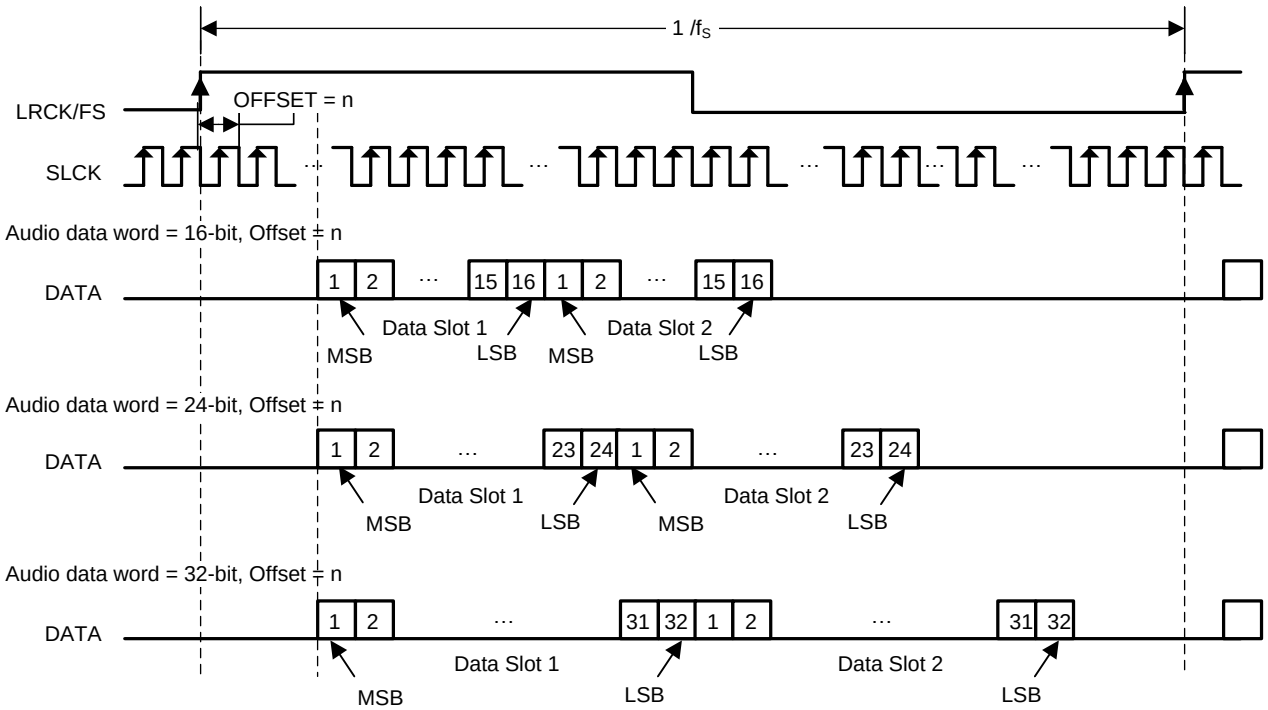


TDM/DSP Data Format with OFFSET = 1

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

Figure 28. TDM/DSP 2 Audio Data Format



TDM/DSP Data Format with OFFSET = N

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

Figure 29. TDM/DSP 3 Audio Data Format

8.3.4.5 Input Signal Sensing (Power-Save Mode)

The TAS3251 device has a zero-detect function. The zero-detect function can be applied to both channels of data as an AND function or an OR function, via controls provided in the control port in P0-R65-D[2:1].Continuous Zero data cycles are counted by LRCK/FS, and the threshold of decision for analog mute can be set by P0-R59, D[6:4] for the data which is clocked in on the left frame of an I^2S signal or Slot 1 of a TDM signal and P0-R59, D[2:0] for the data which is clocked in on the right frame of an I^2S signal or Slot 2 of a TDM signal as shown in Table 11. Default values are 0 for both channels.

Table 10. Zero Detection Mode

ATMUTECTL	VALUE	FUNCTION
Bit : 2	0	Zero data triggers for the two channels for zero detection are ORed together.
	1 (Default)	Zero data triggers for the two channels for zero detection are ANDed together.
Bit : 1	0	Zero detection and analog mute are disabled for the data clocked in on the right frame of an I^2S signal or Slot 2 of a TDM signal.
	1 (Default)	Zero detection analog mute are enabled for the data clocked in on the right frame of an I^2S signal or Slot 2 of a TDM signal.
Bit : 0	0	Zero detection analog mute are disabled for the data clocked in on the left frame of an I^2S signal or Slot 1 of a TDM signal.
	1 (Default)	Zero detection analog mute are enabled for the data clocked in on the left frame of an I^2S signal or Slot 1 of a TDM signal.

Table 11. Zero Data Detection Time

ATMUTETIML OR ATMA	NUMBER OF LRCK/FS CYCLES	TIME at 48 kHz
0 0 0	1024	21 ms
0 0 1	5120	106 ms
0 1 0	10240	213 ms
0 1 1	25600	533 ms
1 0 0	51200	1.066 secs
1 0 1	102400	2.133 secs
1 1 0	256000	5.333 secs
1 1 1	512000	10.66 secs

8.3.5 Volume Control

8.3.5.1 DAC Digital Gain Control

A basic DAC digital gain control with range between 24 dB and –103 dB and mute is available on each channels by P0-R61-D[7:0] for SPK_OUTB± and P0-R62-D[7:0] for SPK_OUTA±. These volume controls all have 0.5 dB step programmability over most gain and attenuation ranges. Table 12 lists the detailed gain versus programmed setting for the basic volume control. Volume can be changed for both SPK_OUTB± and SPK_OUTA± at the same time or independently by P0-R61-D[1:0] . When D[1:0] set 00 (default), independent control is selected. When D[1:0] set 01, SPK_OUTA± accords with SPK_OUTB± volume. When D[1:0] set 10, SPK_OUTA± volume controls the volume for both channels. To set D[1:0] to 11 is prohibited.

Table 12. DAC Digital Gain Control Settings

GAIN SETTING	BINARY DATA	GAIN (dB)	COMMENTS
0	0000-0000	24.0	Positive maximum
1	0000-0001	23.5	
. . .	. . .	. . .	
46	0010-1110	1.0	

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Table 12. DAC Digital Gain Control Settings (continued)

GAIN SETTING	BINARY DATA	GAIN (dB)	COMMENTS
47	0010-1111	0.5	
48	0011-0000	0.0	No attenuation (default)
49	0011-0001	–0.5	
50	0011-0010	–1.0	
51	0011-0011	–1.5	
. . .	. . .	. . .	
253	1111-1101	–102.5	
254	1111-1110	–103	Negative maximum
255	1111-1111	– ∞	Negative infinite (Mute)

Ramp-up frequency and ramp-down frequency can be controlled by P0-R63, D[7:6] and D[3:2] as shown in Table 13. Also ramp-up step and ramp-down step can be controlled by P0-R63, D[5:4] and D[1:0] as shown in Table 14.

Table 13. Ramp Up or Down Frequency

RAMP UP SPEED	EVERY N f_S	COMMENTS	RAMP DOWN FREQUENCY	EVERY N f_S	COMMENTS
00	1	Default	00	1	Default
01	2		01	2	
10	4		10	4	
11	Direct change		11	Direct change	

Table 14. Ramp Up or Down Step

RAMP UP STEP	STEP dB	COMMENTS	RAMP DOWN STEP	STEP dB	COMMENTS
00	4.0		00	–4.0	
01	2.0		01	–2.0	
10	1.0	Default	10	–1.0	Default
11	0.5		11	–0.5	

8.3.5.1.1 Emergency Volume Ramp Down

Emergency ramp down of the volume is provided for situations such as I^2S clock error and power supply failure. Ramp-down speed is controlled by P0-R64-D[7:6]. Ramp-down step can be controlled by P0-R64-D[5:4]. Default is ramp-down by every f_S cycle with –4dB step.

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8.3.6 SDOUT Port and Hardware Control Pin

The TAS3251 device contains a versatile GPIO port (SDOUT pin), allowing signals to be passed from the system to the device or sent from the device to the system. This pin can be used for advanced clocking features, to pass internal signals to the system or accept signals from the system for use inside the device by a given process flow. The SDOUT pin supports serial data out and the features described in Figure 30. The register map can be used to configure the function of the SDOUT pin.

Here are a few key registers to enable the SDOUT pin:

- Page 0, Register 7, Bit 0 (SDSL) - select if SDOUT data is pre-DSP or post-DSP processing.
- Page 0, Register 9, Bit 5 (SDDIR) - select the SDOUT pin as input or output.
- See register map for more details to configure the SDOUT pin function.

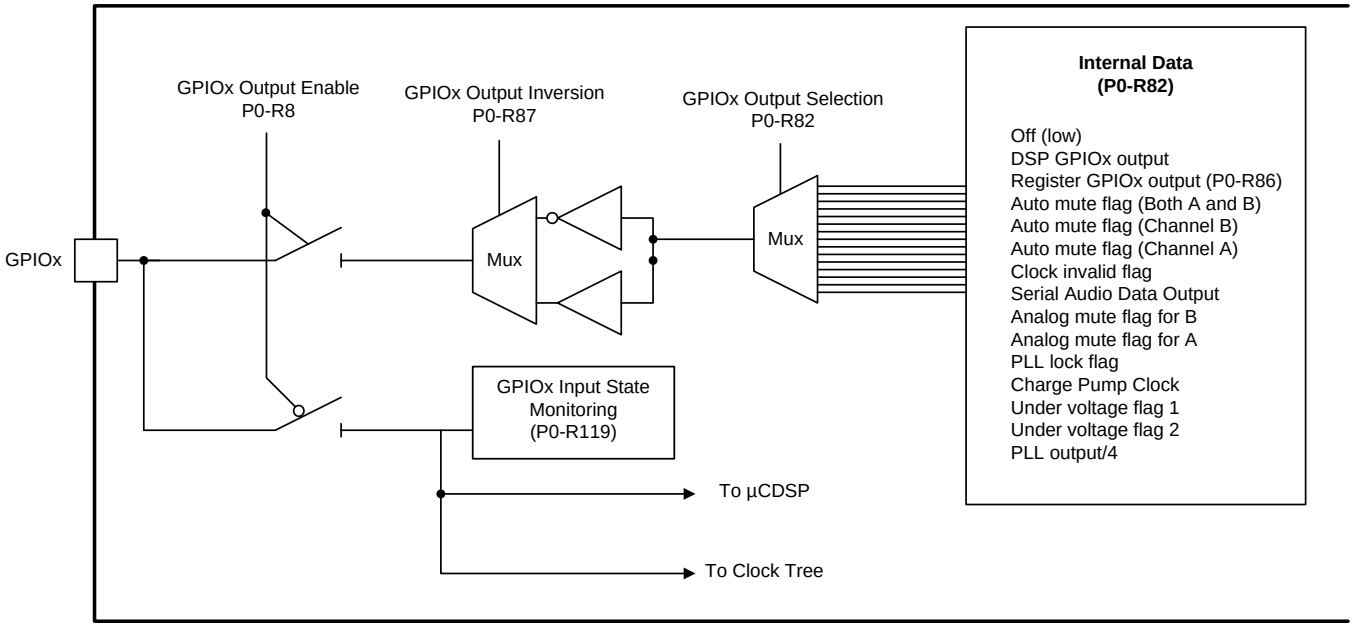

Figure 30. SDOUT GPIO Port

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8.3.7 I²C Communication Port

The TAS3251 device supports the I²C serial bus and the data transmission protocol for standard and fast mode as a slave device. Because the TAS3251 register map spans several books and pages, the user must select the correct book and page before writing individual register bits or bytes. Changing from book to book is accomplished by first changing to page 0x00 by writing 0x00 to register 0x00 and then writing the book number to register 0x7f of page 0. Changing from page to page is accomplished via register 0x00 on each page. The register value selects the register page, from 0 to 255.

8.3.7.1 Slave Address

Table 15. I²C Slave Address

MSB							LSB
1	0	0	1	0	1	ADR	R/ $\overline{W}$

The TAS3251 device has 7 bits for the slave address. The last bit of the address byte is the device select bit which can be selected by setting the ADR pin either high or low. A maximum of two devices can be connected on the same bus at one time, which gives two options: 0x94 and 0x96. See table Table 16 for more details. Each TAS3251 device responds when it receives the slave address.

Table 16. I²C Address Configuration using ADR Pin

ADR Pin / Bit	I²C SLAVE ADDRESS + [R/$\overline{W}$]
0	0x94
1	0x96

8.3.7.2 Register Address Auto-Increment Mode

Auto-increment mode allows multiple sequential register locations to be written to or read back in a single operation, and is especially useful for block write and read operations. The TAS3251 device supports auto-increment mode automatically. Auto-increment stops at page boundries.

8.3.7.3 Packet Protocol

A master device must control packet protocol, which consists of start condition, slave address, read/write bit, data if write or acknowledge if read, and stop condition. The TAS3251 device supports only slave receivers and slave transmitters.

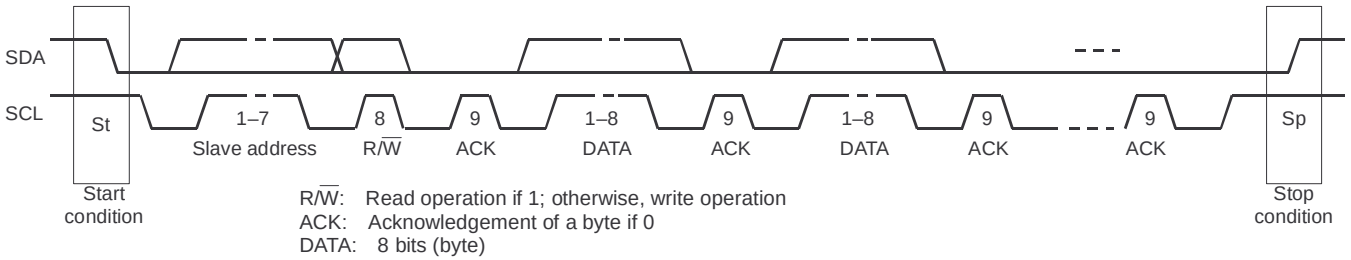

Figure 31. Packet Protocol

Table 17. Write Operation - Basic I²C Framework

Transmitter	*M*	*M*	*M*	*S*	*M*	*S*	*M*	*S*		*S*	*M*
Data Type	St	slave address	R/	ACK	DATA	ACK	DATA	ACK		ACK	Sp

Table 18. Read Operation - Basic I²C Framework

Transmitter	*M*	*M*	*M*	*S*	*S*	*M*	*S*	*M*		*M*	*M*
Data Type	St	slave address	R/	ACK	DATA	ACK	DATA	ACK		NACK	Sp

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M = Master Device; S = Slave Device; St = Start Condition Sp = Stop Condition

8.3.7.4 Write Register

A master can write to any TAS3251 device registers using single or multiple accesses. The master sends a TAS3251 device slave address with a write bit, a register address with auto-increment bit, and the data. If auto-increment is enabled, the address is that of the starting register, followed by the data to be transferred. When the data is received properly, the index register is incremented by 1 automatically. When the index register reaches 0x7F, the next value is 0x0. Table 19 shows the write operation.

Table 19. Write Operation

Transmitter	*M*	*M*	*M*	*S*	*M*		*S*	*M*	*S*	*M*	*S*		*S*	*M*
Data Type	St	slave addr	W	ACK	inc	reg addr	ACK	write data 1	ACK	write data 2	ACK		ACK	Sp

M = Master Device; S = Slave Device; St = Start Condition Sp = Stop Condition; W = Write; ACK = Acknowledge

8.3.7.5 Read Register

A master can read the TAS3251 device register. The value of the register address is stored in an indirect index register in advance. The master sends a TAS3251 device slave address with a read bit after storing the register address. Then the TAS3251 device transfers the data which the index register points to. When auto-increment is enabled, the index register is incremented by 1 automatically. When the index register reaches 0x7F, the next value is 0x0. Table 20 lists the read operation.

Table 20. Read Operation

Transmitter	*M*	*M*	*M*	*S*	*M*		*S*	*M*	*M*	*M*	*S*	*S*	*M*		*M*	*M*
Data Type	St	slave addr	W	ACK	inc	reg addr	ACK	Sr	slave addr	R	ACK	data	ACK		NACK	Sp

M = Master Device; S = Slave Device; St = Start Condition; Sr = Repeated start condition; Sp = Stop Condition; W = Write; R = Read; NACK = Not acknowledge

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8.3.7.6 DSP Book, Page, and Register Update

The DSP memory is arranged in books, pages, and registers. Each book has several pages and each page has several registers.

8.3.7.6.1 Book and Page Change

To change the book, the user must be on page 0x00. In register 0x7f on page 0x00 you can change the book. On page 0x00 of each book, register 0x7f is used to change the book. Register 0x00 of each page is used to change the page. To change a book first write 0x00 to register 0x00 to switch to page 0 then write the book number to register 0x7f on page 0. To change between pages in a book, simply write the page number to register 0x00.

8.3.7.6.2 Swap Flag

The swap flag is used to copy the audio coefficient from the host memory to the DSP memory. The swap flag feature is important to maintain the stability of the BQs. A BQ is a closed-loop system with 5 coefficients. To avoid instability in the BQ in an update transition between two different filters, update all five parameters within one audio sample. The interal swap flag insures all 5 coefficients for each filter are transferred from host memory to DSP memory occurs within an audio sample. The swap flag stays high until the full host buffer is transferred to DSP memory. Updates to the Host buffer should not be made while the swap flag is high.

All writes to book 0x8C at pages above page 0x1B and register 0x58 require the swap flag. The swap flag is located in book 0x8C, page 0x05page 0x01, and register 0x7C and must be set to 0x00 00 00 01 for a swap.

8.3.7.6.3 Example Use

The following is a sample script for using the DSP host memory to change the fine volume on the device on I^2C slave address 0x90 to the default value of 0 dB:

```
w 90 00 00 #Go to page 0
w 90 7f 8C #Change the book to 0x8C
w 90 00 21 #Go to page 0x21
w 90 34 40 00 00 00 #Fine volume Left
w 90 38 40 00 00 00 #Fine volume Rights
#Run the swap flag for the DSP to work on the new coefficients
w 90 00 00 #Go to page 0
w 90 7f 8C #Change the book to 0x8C
w 90 00 05 #Go to page 0x05
w 90 7C 00 00 00 01 #Swap flag
```

8.3.8 Pop and Click Free Startup and Shutdown

The output power stage PWM generator minimizes pop and click with a unique turn on and turn off behavior. The sequence ramps up the PWM switching to the full PVDD voltage using the timing capacitor on the C_START pin. It is recommended to use a 10 nF capacitor from the C_START pin to GND for best pop and click performance. The startup time can be lengthened by increasing the capacitance up to 470 nF.

8.3.9 Integrated Oscillator for Output Power Stage

The amplifier power stage of the uses a built in oscillator that can be trimmed by an external resistor from the FREQ_ADJ pin to GND. Changes in the oscillator frequency should be made with resistor values specified in *Recommended Operating Conditions* while $\overline{\text{RESET}}$ is low. See section DAC and DSP Clocking for configuring the clocks for the digital front-end (DAC and DSP).

To reduce interference problems while using a radio receiver tuned within the AM band, the switching frequency can be changed from nominal to lower or higher values. These values should be chosen such that the nominal and the alternate switching frequencies together result in the fewest cases of interference throughout the AM band. The oscillator frequency can be selected by the value of the FREQ_ADJ resistor connected to GND in master mode.

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8.3.9.1 Oscillator Synchronization and Slave Mode

The TAS3251 supports synchronizing the internal oscillator and output switching frequency of multiple TAS3251 devices for managing the power supply, electro-magnetic interference and preventing audio beating. For slave mode operation, turn off the oscillator of the slave by pulling the FREQ_ADJ pin to DVDD. This configures the OSC_IOM and OSC_IOP pins as inputs to be slaved from an external differential clock. In a master/slave system inter-channel delay is automatically added to the PWM between audio channels, which can be seen with all channels switching at different times. This will not influence the audio output, but only the switch timing to minimize noise coupling between audio channels through the power supply. Inter-channel delay is needed to optimize audio performance and to get better operating conditions for the power supply. The inter-channel delay will be set up for a slave device depending on the polarity of the OSC_IOM and OSC_IOP connection as follows:

- **Slave 1 Mode** has positive polarity with the master device. Master OSC_IOP and the slave OSC_IOP are connected. Master OSC_IOM and the slave OSC_IOM are connected.
- **Slave 2 Mode** has reverse polarity with the master device. Master OSC_IOP and the slave OSC_IOM are connected. Master OSC_IOM and the slave OSC_IOP are connected.

Multiple slaves can be connected to one master TAS3251. If more than 2 slaves are used it is best to alternate the slave modes so that adjacent devices are configured in different slave modes. The inter-channel delay for interleaved channel idle switching is given in the table below for the master/slave and output configuration modes in degrees relative to the PWM frame.

Table 21. Master/Slave Inter Channel Delay Settings

Master	MODE = 0, 2 x BTL mode	MODE = 1, 1 x PBTL mode
SPK_OUTA+	0°	0°
SPK_OUTA-	180°	180°
SPK_OUTB+	60°	0°
SPK_OUTB-	240°	180°
Slave 1		
SPK_OUTA+	60°	60°
SPK_OUTA-	240°	240°
SPK_OUTB+	120°	60°
SPK_OUTB-	300°	240°
Slave 2		
SPK_OUTA+	30°	30°
SPK_OUTA-	210°	210°
SPK_OUTB+	90°	30°
SPK_OUTB-	270°	210°

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8.3.10 Device Output Stage Protection System

The TAS3251 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, and undervoltage. The TAS3251 responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the $\overline{\text{FAULT}}$ pin low. In situations other than overload and overtemperature error (OTE), the device automatically recovers when the fault condition has been removed, that is, the supply voltage has increased.

The device will handle errors, as shown in Table 22.

Table 22. Device Protection

BTL MODE		PBTL MODE	
LOCAL ERROR IN	TURNS OFF	LOCAL ERROR IN	TURNS OFF
SPK_OUTA+	A+ and A-	SPK_OUTA+	A+, A-, B+, and B-
SPK_OUTA-		SPK_OUTA-	
SPK_OUTB+	B+ and B-	SPK_OUTB+	
SPK_OUTB-		SPK_OUTB-	

Bootstrap UVP does not shutdown according to the table, it shuts down the respective halfbridge (non-latching, does not assert $\overline{\text{FAULT}}$).

8.3.10.1 Error Reporting

The $\overline{\text{FAULT}}$, and $\overline{\text{CLIP\_OTW}}$, pins are active-low, open-drain outputs. Each pin has a 26 kΩ pull-up resistor reference to DVDD and does not need an external pull-up resistor. The function is for protection-mode signaling to a system-control device.

Any fault resulting in device shutdown is signaled by the $\overline{\text{FAULT}}$ pin going low. Also, $\overline{\text{CLIP\_OTW}}$ goes low when the device junction temperature exceeds 125°C (see Table 23).

Table 23. Error Reporting

$\overline{\text{FAULT}}$	$\overline{\text{CLIP\_OTW}}$	DESCRIPTION
0	0	Overtemperature (OTE), overload (OLP) or undervoltage (UVP) Junction temperature higher than 125°C (overtemperature warning)
0	1	Overload (OLP) or undervoltage (UVP). Junction temperature lower than 125°C
1	0	Junction temperature higher than 125°C (overtemperature warning)
1	1	Junction temperature lower than 125°C and no OLP or UVP faults (normal operation)

Note that asserting $\overline{\text{RESET}}$ low forces the $\overline{\text{FAULT}}$ signal high, independent of faults being present. TI recommends monitoring the $\overline{\text{CLIP\_OTW}}$ signal using the system microcontroller and responding to an overtemperature warning signal by turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on both $\overline{\text{FAULT}}$ and $\overline{\text{CLIP\_OTW}}$ outputs.

8.3.10.2 Overload and Short Circuit Current Protection

TAS3251 has fast reacting current sensors with a programmable trip threshold (OC threshold) on all high-side and low-side FETs. To prevent output current from increasing beyond the programmed threshold, TAS3251 has the option of either limiting the output current for each switching cycle (Cycle By Cycle Current Control, CB3C) or to perform an immediate shutdown of the output in case of excess output current (Latching Shutdown). CB3C prevents premature shutdown due to high output current transients caused by high level music transients and a drop of real speaker's load impedance, and allows the output current to be limited to a maximum programmed level. If the maximum output current persists, i.e. the power stage being overloaded with too low load impedance, the device will shut down the affected output channel and the affected output is put in a high-impedance (Hi- Z) state until a $\overline{\text{RESET}}$ cycle is initiated. CB3C works individually for each half bridge output. If an over current event is triggered, CB3C performs a state flip of the half bridge output that is cleared upon beginning of next PWM frame.

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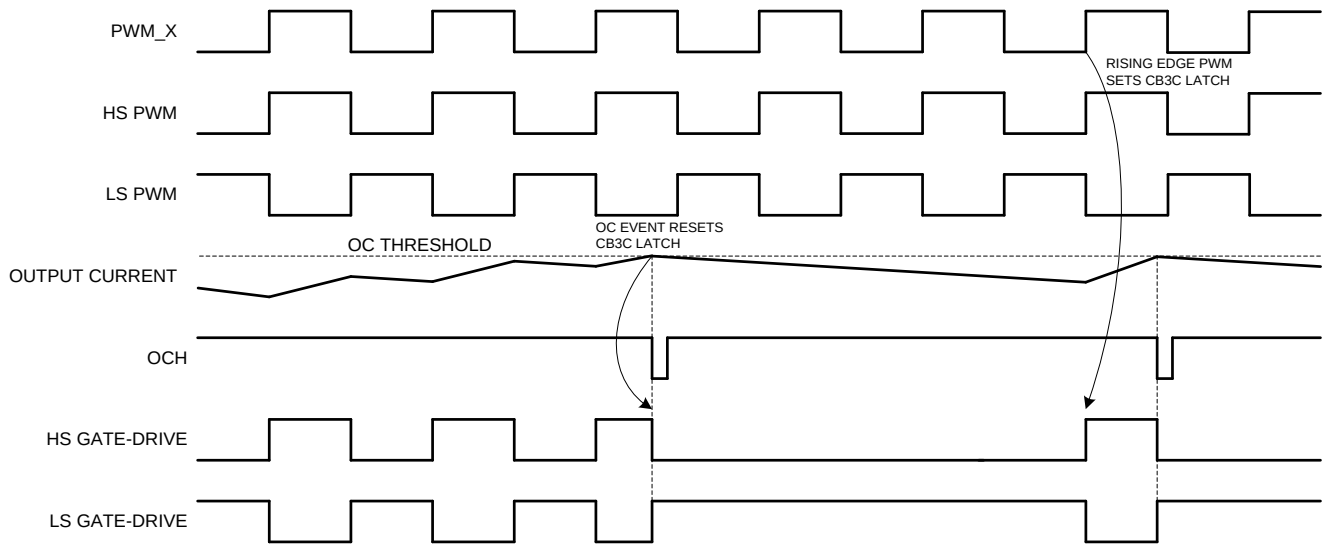

Figure 32. CB3C Timing Example

During CB3C an over load counter increments for each over current event and decrease for each non-over current PWM cycle. This allows full amplitude transients into a low speaker impedance without a shutdown protection action. In the event of a short circuit condition, the over current protection limits the output current by the CB3C operation and eventually shut down the affected output if the overload counter reaches its maximum value. If a latched OC operation is required such that the device shuts down the affected output immediately upon first detected over current event, this protection mode should be selected. The over current threshold and mode (CB3C or Latched OC) is programmed by the OC_ADJ resistor value. The OC_ADJ resistor needs to be within its intentional value range for either CB3C operation or Latched OC operation.

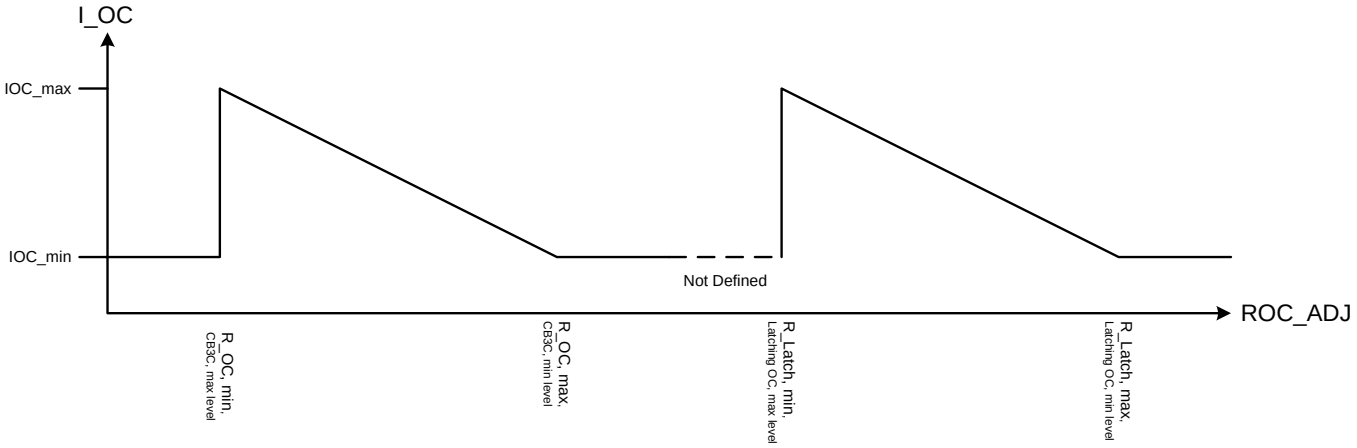

Figure 33. OC Threshold versus OC ADJ Resistor Value Example

OC_ADJ values outside specified value range for either CB3C or latched OC operation will result in minimum OC threshold.

Table 24. Device Protection

OC_ADJ Resistor Value	Protection Mode	OC Threshold
22 kΩ	CB3C	16.3 A
24 kΩ	CB3C	15.1 A
27 kΩ	CB3C	13.5 A
30 kΩ	CB3C	12.3 A

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Table 24. Device Protection (continued)

OC_ADJ Resistor Value	Protection Mode	OC Threshold
47 kΩ	Latched OC	16.3 A
51 kΩ	Latched OC	15.1 A
56 kΩ	Latched OC	13.5 A
64 kΩ	Latched OC	12.3 A

8.3.10.3 Signal Clipping and Pulse Injector

A built in activity detector monitors the PWM activity of the SPK_OUTx pins. TAS3251 is designed to drive unclipped output signals all the way to PVDD and GND rails. In case of audio signal clipping when applying excessive input signal voltage, or in case of CB3C current protection being active, the amplifier feedback loop of the audio channel will respond to this condition with a saturated state, and the output PWM signals will stop unless special circuitry is implemented to handle this situation. To prevent the output PWM signals from stopping in a clipping or CB3C situation, narrow pulses are injejcted to the gate drive to maintain output activity. The injected narrow pulses are injected at every 4th PWM frame, and thus the effective switching frequency during this state is reduced to 1/4 of the normal switching frequency.

Signal clipping is signalled on the $\overline{\text{CLIP\_OTW}}$ pin and is self clearing when signal level reduces and the device reverts to normal operation. The $\overline{\text{CLIP\_OTW}}$ pulses starts at the onset to output clipping, typically at a THD level around 0.01%, resulting in narrow $\overline{\text{CLIP\_OTW}}$ pulses starting with a pulse width of ~500ns.

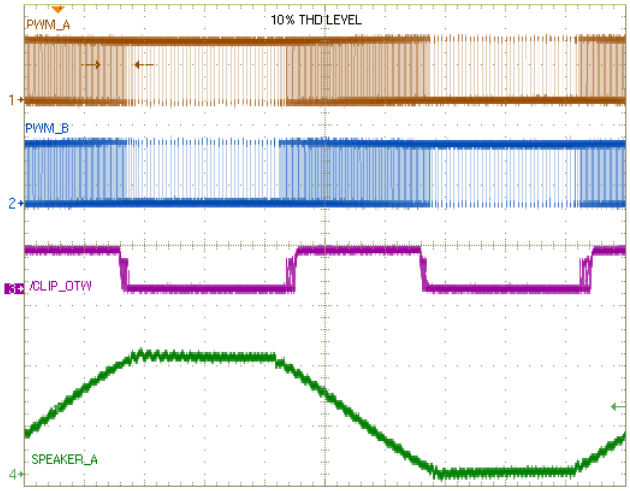

Figure 34. Signal Clipping PWM and Speaker Output Signals

8.3.10.4 DC Speaker Protection

The output DC protection scheme protects a speaker from excess DC current in case one terminal of the speaker is connected to the amplifier while the other is accidentally shorted to the chassis ground. Such a short circuit results in a DC voltage of PVDD/2 across the speaker, which potentially can result in destructive current levels. The output DC protection detects any unbalance of the output and input current of a BTL output, and in the event of the unbalance exceeding a programmed threshold, the overload counter increments until its maximum value and the affected output channel is shut down. DC Speaker Protection is disabled in PBTL and SE mode operation.

8.3.10.5 Pin-to-Pin Short Circuit Protection (PPSC)

The PPSC detection system protects the device from permanent damage in the case that a power output pin (SPK_OUTx) is shorted to GND_X or PVDD_X. For comparison, the OC protection system detects an overcurrent after the demodulation filter where PPSC detects shorts directly at the pin before the filter. PPSC detection is performed at startup i.e. when VDD is supplied, consequently a short to either GND_X or PVDD_X after system startup does not activate the PPSC detection system. When PPSC detection is activated by a short on the output, all half bridges are kept in a Hi-Z state until the short is removed; the device then continues the startup sequence and starts switching. The detection is controlled globally by a two step sequence. The first step

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ensures that there are no shorts from SPK_OUTx to GND_X, the second step tests that there are no shorts from SPK_OUTx to PVDD_X. The total duration of this process is roughly proportional to the capacitance of the output LC filter. The typical duration is < 15 ms/μF. While the PPSC detection is in progress, FAULT is kept low, and the device will not react to changes applied to the RESET pin. If no shorts are present the PPSC detection passes, and FAULT is released. A device reset will not start a new PPSC detection. PPSC detection is enabled in BTL and PBTL output configurations, the detection is not performed in SE mode. To make sure not to trip the PPSC detection system it is recommended not to insert a resistive load to GND_X or PVDD_X.

8.3.10.6 Overtemperature Protection OTW and OTE

TAS3251 has a two-level temperature-protection system that asserts an active-low warning signal (CLIP_OTW) when the device junction temperature exceeds 125°C (typical) and, if the device junction temperature exceeds 155°C (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and FAULT being asserted low. OTE is latched in this case. To clear the OTE latch, RESET must be asserted. Thereafter, the device resumes normal operation.

8.3.10.7 Undervoltage Protection (UVP) and Power-on Reset (POR)

The UVP and POR circuits of the TAS3251 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach values stated in the *Electrical Characteristics* table. Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and FAULT being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

ADVANCE INFORMATION

8.3.10.8 Fault Handling

If a fault situation occurs while in operation, the device acts accordingly to the fault being a global or a channel fault. A global fault is a chip-wide fault situation and causes all PWM activity of the device to be shut down, and will assert $\overline{\text{FAULT}}$ low. A global fault is a latching fault and clearing $\overline{\text{FAULT}}$ and restarting operation requires resetting the device by toggling $\overline{\text{RESET}}$. Deasserting $\overline{\text{RESET}}$ should never be allowed with excessive system temperature, so it is advised to monitor $\overline{\text{RESET}}$ by a system microcontroller and only allow releasing $\overline{\text{RESET}}$ ($\overline{\text{RESET}}$ high) if the CLIP_$\overline{\text{OTW}}$ signal is cleared (high). A channel fault results in shutdown of the PWM activity of the affected channel(s). Note that asserting $\overline{\text{RESET}}$ low forces the $\overline{\text{FAULT}}$ signal high, independent of faults being present.

Table 25. Error Reporting

Fault/Event	Fault/Event Description	Global or Channel	Reporting Method	Latched/Self Clearing	Action needed to Clear	Output FETs
PVDD_X UVP	Voltage Fault	Global	$\overline{\text{FAULT}}$ pin	Self Clearing	Increase affected supply voltage	HI-Z
VDD UVP						
AVDD UVP						
POR (DVDD UVP)	Power On Reset	Global	$\overline{\text{FAULT}}$ pin	Self Clearing	Allow DVDD to rise	HI-Z
BST_X UVP	Voltage Fault	Channel (Half Bridge)	None	Self Clearing	Allow BST cap to recharge (lowside ON, VDD 12V)	HighSide off
OTW	Thermal Warning	Global	$\overline{\text{OTW}}$ pin	Self Clearing	Cool below OTW threshold	Normal operation
OTE	Thermal Shutdown	Global	$\overline{\text{FAULT}}$ pin	Latched	Toggle $\overline{\text{RESET}}$	HI-Z
OLP (CB3C>1.7ms)	OC Shutdown	Channel	$\overline{\text{FAULT}}$ pin	Latched	Toggle $\overline{\text{RESET}}$	HI-Z
Latched OC (47kΩ<ROC_ADJ<68kΩ)	OC Shutdown	Channel	$\overline{\text{FAULT}}$ pin	Latched	Toggle $\overline{\text{RESET}}$	HI-Z
CB3C (22kΩ<ROC_ADJ<30kΩ)	OC Limiting	Channel	None	Self Clearing	Reduce signal level or remove short	Flip state, cycle by cycle at fs/3
Stuck at Fault(1)	No OSC_IO activity in Slave Mode	Global	None	Self Clearing	Resume OSC_IO activity	HI-Z

(1) Stuck at Fault occurs when input OSC_IO input signal frequency drops below minimum frequency given in the *Electrical Characteristics* table of this data sheet.

8.3.10.9 Output Power Stage Reset

Asserting $\overline{\text{RESET}}$ low initiates the device ramp down. The output FETs go into a Hi-Z state after the ramp down is complete. Output pull downs are active both in SE mode and BTL mode with $\overline{\text{RESET}}$ low.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset input low enables weak pulldown of the half-bridge outputs.

Asserting reset input low removes any fault information to be signaled on the $\overline{\text{FAULT}}$ output, that is, $\overline{\text{FAULT}}$ is forced high. A rising-edge transition on reset input allows the device to resume operation after a fault. To ensure thermal reliability, the rising edge of reset must occur no sooner than 4 ms after the falling edge of $\overline{\text{FAULT}}$.

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8.3.11 Initialization, Startup and Shutdown

This section provides common procedures for power up, operation and power down sequencing.

8.3.11.1 Power Up and Startup Sequence

The device analog front-end, including the DAC and DSP, are controlled independently of the output power stage. Follow the sequence below to power up the digital front-end and power stage to begin playing audio.

1. Apply power to DAC_DVDD, DAC_AVDD, GVDD_x, and PVDD_x. The power supplies do not have a power on sequence and can be powered on in any order.
2. Apply I2S or TDM clocks to the device to enable the internal system clocks.
3. Mute the left and right DAC channels, by setting Register 0x03, Bits 0 (right) and 4 (left) to '1'.
4. Set DSP coefficients and configuration settings through I^2C (optional). The DSP will pass-through audio if no registers are changed.
5. Bring the DSP out of standby by setting Register 0x02, Bit 7 (DSPR) to '1'.
6. Unmute the left and right DAC channels, by setting Register 0x03, Bits 0 (right) and 4 (left) to '0'.
7. Enable the amplifier output stage by setting the $\overline{\text{RESET\_AMP}}$ pin high.
8. Play audio through I2S or TDM.

8.3.11.2 Power Down and Shutdown Sequence

Follow the sequence below to initiate standby and power down the digital front-end and power stage.

1. Stop audio playback.
2. Disable the amplifier output stage by setting the $\overline{\text{RESET\_AMP}}$ pin low.
3. Mute the left and right DAC channels by setting Register 0x03, Bits 0 (right) and 4 (left) to '1'.
4. Optional: Put the DAC into a low-power mode register 0x02.
5. Optional: Remove voltage from all power supply rails.

8.3.11.3 Device Mute

1. Optional: Disable the amplifier output stage by setting the $\overline{\text{RESET\_AMP}}$ pin low.
2. Mute the left and right DAC channels by setting Register 0x03, Bits 0 (right) and 4 (left) to '1'.

8.3.11.4 Device Unmute

1. Unmute the left and right DAC channels, by setting Register 0x03, Bits 0 (right) and 4 (left) to '0'.
2. Optional: If the amplifier output stage is powered down, enable the amplifier output stage by setting the $\overline{\text{RESET\_AMP}}$ pin high.

8.3.11.5 Device Reset

8.3.11.6 Mute with $\overline{\text{DAC\_MUTE}}$ or Clock Error

Under certain conditions, the TAS3251 can exhibit some pop on power down if the device does not have enough time to detect power loss and initiate the muting process. The TAS3251has two auto-mute functions to mute the device upon power loss (intentional or unintentional).

- **$\overline{\text{DAC\_MUTE}}$** - when the $\overline{\text{DAC\_MUTE}}$ pin is pulled low, the incoming serial port data is attenuated to 0, closely followed by a hard analog mute. This process takes 150 samples + 0.2 ms.
- **Clock Error Detect** - when a clock error is detected on the incoming serial port data, the TAS3251 switches to an internal oscillator and continues to drive the DAC outputs while attenuating the data from the last known good value. Once this process completes, the TAS3251 DAC outputs are hard muted to ground.

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8.3.11.6.1 Mute using DAC_MUTE

Deassert $\overline{\text{DAC\_MUTE}}$ low 150 samples + 0.2 ms before power is removed.

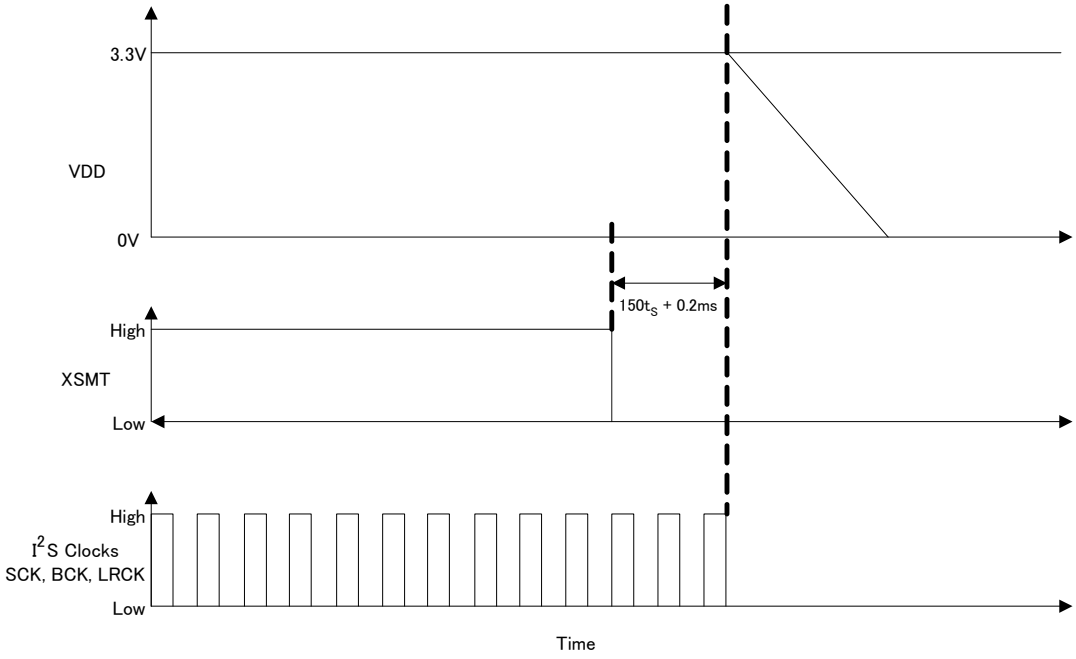

Figure 35. $\overline{\text{DAC\_MUTE}}$ Timing Diagram

8.3.11.7 Mute using Serial Audio Port Clock

Stop I^{2}S clocks (SCLK, MCLK, LRCK) 3 ms before power-down as shown in the figure below.

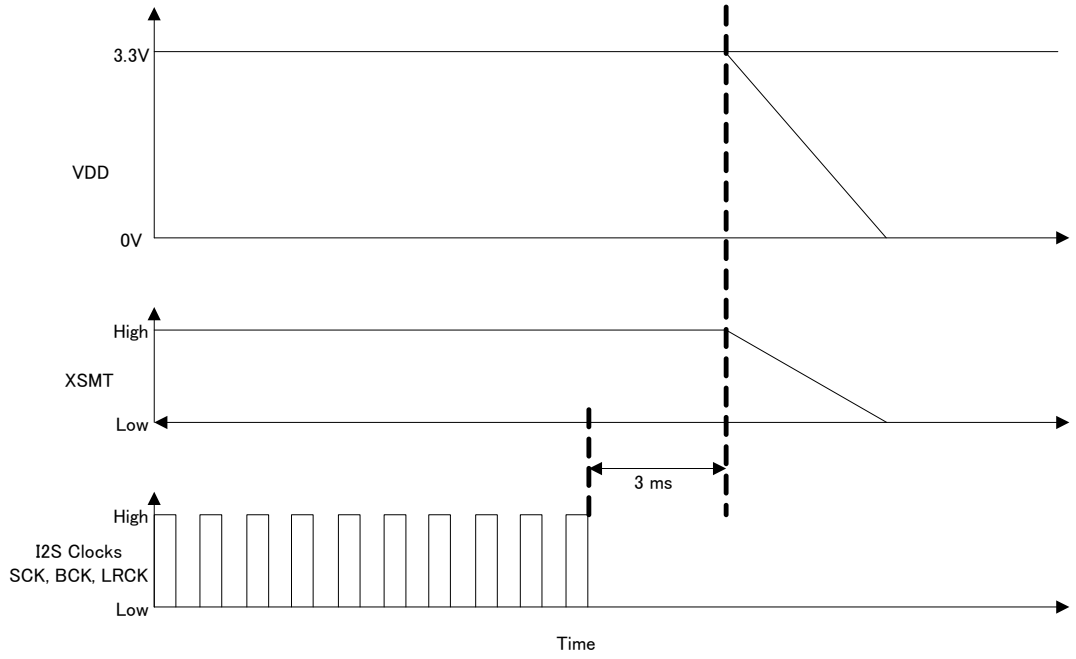

Figure 36. Serial Port Muting Timing Diagram

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8.3.11.8 Muting before an Unplanned Shutdown with $\overline{\text{DAC\_MUTE}}$

Many systems use a low-noise regulator to provide 3.3 V to the DAC_AVDD and DAC_DVDD. The $\overline{\text{DAC\_MUTE}}$ pin can take advantage of such a feature to measure the pre-regulated output (3.3 V) from the system power supply to mute the output before the PVDD power supply discharges. Figure 37 shows how to configure the system to use the $\overline{\text{DAC\_MUTE}}$ pin. The $\overline{\text{DAC\_MUTE}}$ pin can also be used in parallel with a GPIO pin from the system microcontroller, DSP or power supply.

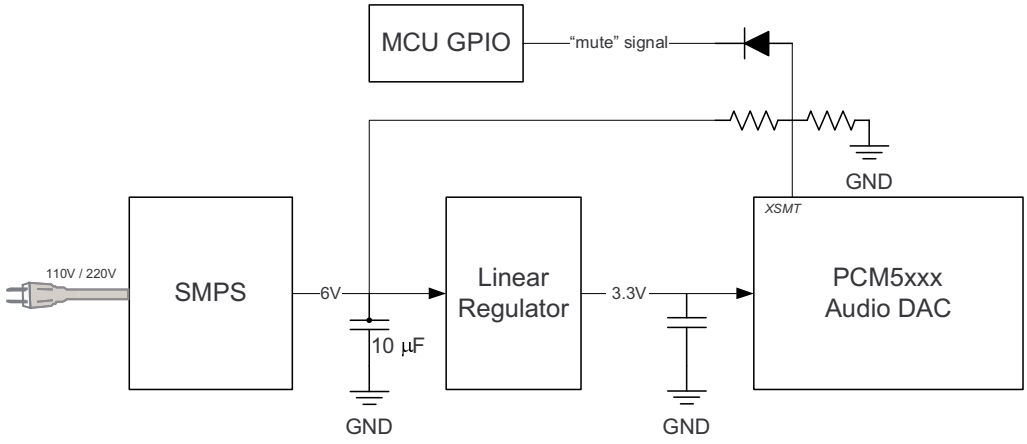

Figure 37. Application Diagram for $\overline{\text{DAC\_MUTE}}$

8.3.11.9 Output Power Stage Startup Timing

The TAS3251 output power stage does not require a specific power-up sequence, but it is recommended to hold $\overline{\text{RESET}}$ low for a minimum of 400 ms after PVDD supply voltage is powered on. The outputs of the half-bridges remain in a high-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the Electrical Characteristics table of this data sheet). This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pull-down of the half-bridge output as well as initiating a controlled ramp up sequence of the output voltage.

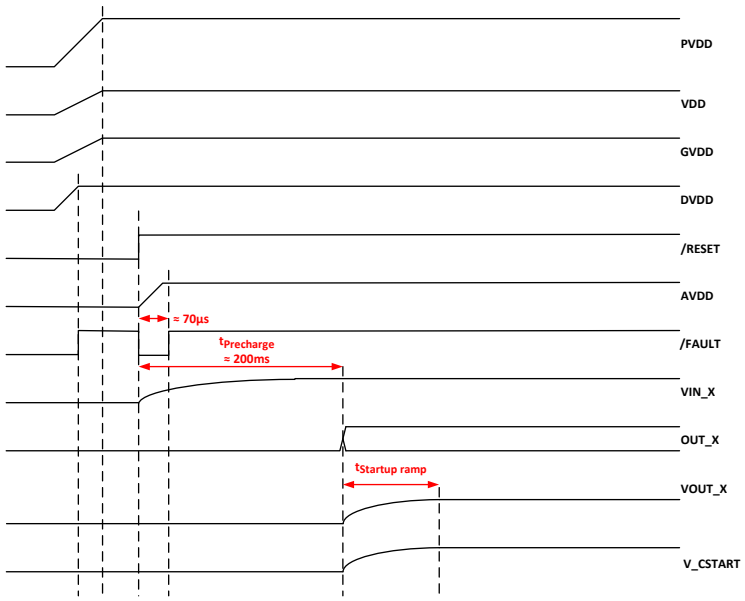

Figure 38. Power Stage Startup Timing

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When $\overline{\text{RESET}}$ is released to turn on TAS3251, $\overline{\text{FAULT}}$ signal will output low and AVDD voltage regulator will be enabled. $\overline{\text{FAULT}}$ will stay low until AVDD reaches the undervoltage protection (UVP) voltage threshold (see the Electrical Characteristics table of this data sheet). Next a pre-charge time begins to stabilize the DC voltage across the input AC coupling capacitors, followed by the ramp up output power stage sequence .

8.4 Device Functional Modes

Because the TAS3251 device is a highly configurable device, numerous modes of operation can exist for the device. For the sake of succinct documentation, these modes are divided into two modes:

- Fundamental operating modes
- Secondary usage modes

Fundamental operating modes are the primary modes of operation that affect the major operational characteristics of the device, which are the most basic configurations that are chosen to ensure compatibility with the intended application or the other components that interact with the device in the final system. Some examples of the operating modes are the communication protocol used by the control port, the output configuration of the amplifier, or the Master/Slave clocking configuration.

The fundamental operating modes are described starting in the *Serial Audio Port Operating Modes* section.

Secondary usage modes are best described as modes of operation that are used after the fundamental operating modes are chosen to fine tune how the device operates within a given system. These secondary usage modes can include selecting between left justified and right justified Serial Audio Port data formats, or enabling some slight gain/attenuation within the DAC path. Secondary usage modes are accomplished through manipulation of the registers and controls in the I^2C control port. Those modes of operation are described in their respective register/bit descriptions and, to avoid redundancy, are not included in this section.

8.4.1 Serial Audio Port Operating Modes

The serial audio port in the TAS3251 device supports industry-standard audio data formats, including I^2S, Time Division Multiplexing (TDM), Left-Justified (LJ), and Right-Justified (RJ) formats. To select the data format that will be used with the device, controls are provided on P0-R40. The timing diagrams for the serial audio port are shown in the *Serial Audio Port Timing – Slave Mode* section, and the data formats are shown in the *Serial Audio Port – Data Formats and Bit Depths* section.

8.4.1.1 Master and Slave Mode Clocking for Digital Serial Audio Port

The digital audio serial port in the TAS3251 device can be configured to receive clocks from another device as a serial audio slave device. The slave mode of operation is described in the *Clock Slave Mode with SCLK PLL to Generate Internal Clocks (3-Wire PCM)* section. If no system processor is available to provide the audio clocks, the TAS3251 device can be placed into Master Mode. In master mode, the TAS3251 device provides the clocks to the other audio devices in the system. For more details regarding the Master and Slave mode operation within the TAS3251 device, see the *Serial Audio Port Operating Modes* section.

8.4.2 Communication Port Operating Modes

The TAS3251 device is configured via an I^2C communication port. The device does not support a hardware only mode of operation, nor Serial Peripheral Interface (SPI) communication. The I^2C Communication Protocol is detailed in the *I^2C Communication Port* section. The I^2C timing requirements are described in the *I^2C Bus Timing –Standard* and *I^2C Bus Timing –Fast* sections.

8.4.3 Speaker Amplifier Operating Modes

The TAS3251 device can be used in two different amplifier configurations:

- Stereo Mode
- Mono Mode

8.4.3.1 Stereo Mode

The familiar stereo mode of operation uses the TAS3251 device to amplify two independent signals, which represent the left and right portions of a stereo signal. These amplified left and right audio signals are presented on differential output pairs shown as SPK_OUTA± and SPK_OUTB±. The routing of the audio data which is presented on the SPK_OUTx outputs can be changed according to the Audio Process Flow which is used and the configuration of registers P0-R42-D[5:4] and P0-R42-D[1:0]. The familiar stereo mode of operation is shown in .

By default, the TAS3251 device is configured to output the Right frame of a I^2S input on the Channel A output and the left frame on the Channel B output.

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Device Functional Modes (continued)

8.4.3.2 Mono Mode

The mono mode of operation is used to describe operation in which the two outputs of the device are placed in parallel with one another to increase the power sourcing capabilities of the audio output channel. This is also known as Parallel Bridge Tied Load (PBTL).

On the output side of the TAS3251 device, the summation of the devices can be done before the filter in a configuration called Pre-Filter PBTL. However, the two outputs may be required to merge together after the inductor portion of the output filter. Doing so does require two additional inductors, but allows smaller, less expensive inductors to be used because the current is divided between the two inductors. This process is called *Post-Filter PBTL*. Both variants of mono operation are shown in Figure 39 and Figure 40.

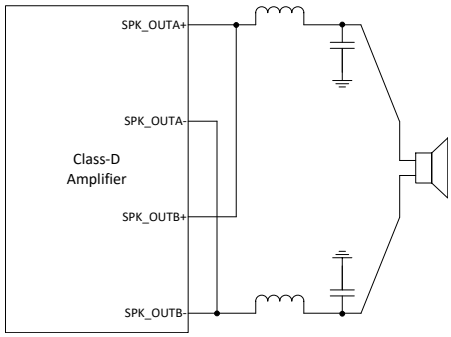

Figure 39. Pre-Filter PBTL

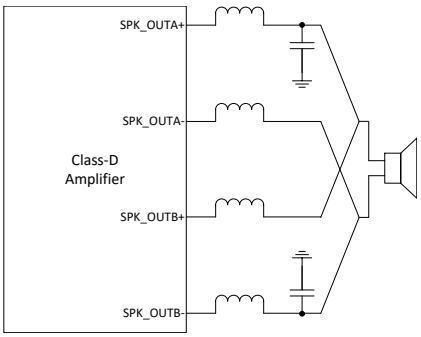

Figure 40. Post-Filter PBTL

On the input side of the TAS3251 device, the input signal to the mono amplifier can be selected from the any slot in a TDM stream or the left or right frame from an I^2S, LJ, or RJ signal. The TAS3251 device can also be configured to amplify some mixture of two signals, as in the case of a subwoofer channel which mixes the left and right channel together and sends the mixture through a low-pass filter to create a mono, low-frequency signal.

ADVANCE INFORMATION

8.5 Programming

8.5.1 Audio Processing Features

The TAS3251 device includes audio processing to optimize the audio performance of the audio system into which they are integrated. The TAS3251 device has 12 Biquad Filters for speaker response tuning, One dual band DPEQ to dynamically adjust the equalization curve that is applied to low-level signal and the curve that is applied to high level signals. A 2-band advanced DRC + AGL structure limits the output power of the amplifier for two regions while controlling the peaking that can occur in the crossover region during compression. A fine volume control is provided to finely adjust the output level of the amplifier based upon the system level considerations faced by the product development engineer.

The TAS3251 device has two signal monitoring options available, the level meter and the serial data out signal. The level meter monitors the signal level through an alpha filter and presents the signal in an I²C register. The level meter signal is taken before the 4x interpolation which occurs before the digital-to-analog conversion.

The details of the audio processing flow, including the I²C control port registers associated with each block, are shown in .

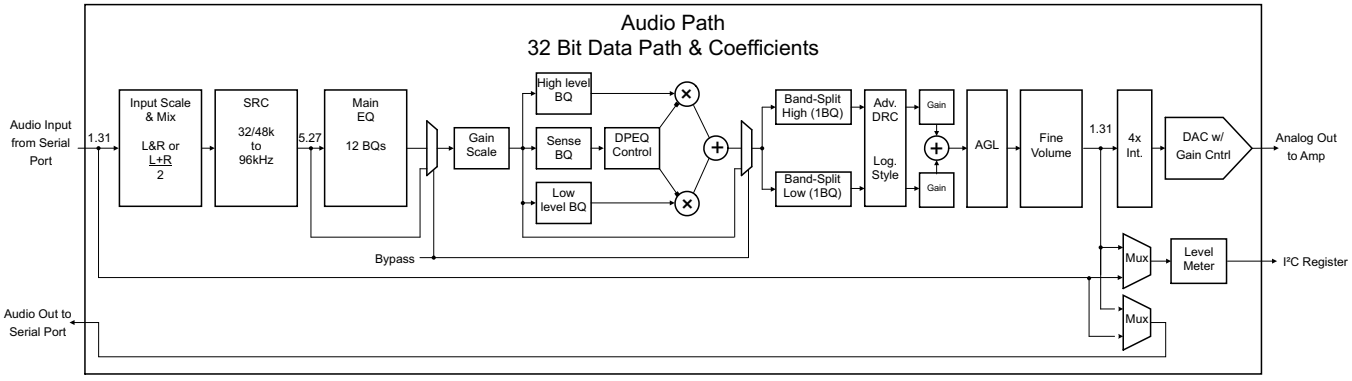

Figure 41. Fixed-Function Process Flow found in the TAS3251

8.5.2 Processing Block Description

The processing block shown in the above is comprised of the following major blocks:

- Input scale and mixer
- Sample Rate Converter (SRC)
- Parametric Equalizers (PEQs)
- BQs Gain Scale
- Dynamic Parametric Equalizer (DPEQ)
- Two-Band Dynamic Ranger Control (DRC)
- Automatic Gain Limiter (AGL)
- Fine Volume
- Level Meter

8.5.2.1 Input Scale and Mixer

The input mixer can be used to mix the left and right channel input signals as shown in Figure 42. The input mixer has four coefficients, which control the mixing and gains of the input signals. When mixing and scaling the input signals, ensure that at maximum input level the input mixer outputs don't exceed 0 dBFs, which will overdrive the SRC inputs.

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Programming (continued)

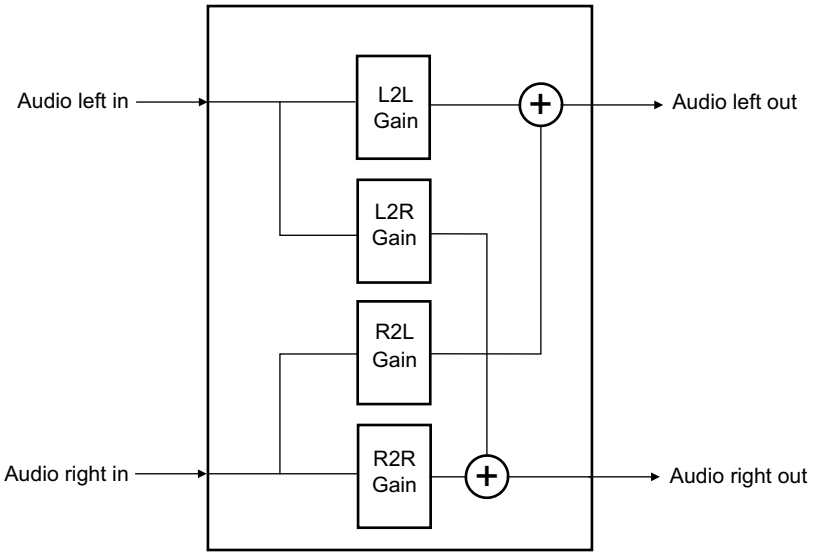

Figure 42. Input Scale and Mixer

8.5.2.1.1 Example

The following is a sample script for setting up the both left and right channels for (½L + ½R) or (L + R) / 2:

```
w 90 00 00 # Go to page 0
w 90 7f 8C #Change the book to 0x8C
w 90 00 21 #Go to page 0x21
w 90 3C 00 40 26 E7 #Input mixer left in to left out gain
w 90 40 00 40 26 E7 #Input mixer right in to left out gain
w 90 44 00 40 26 E7 #Input mixer left in to right out gain
w 90 48 00 40 26 E7 #Input mixer right in to right out gain
#Run the swap flag for the DSP to work on the new coefficients
w 90 00 00 #Go to page 0
w 90 7f 8C #Change the book to 0x8C
w 90 00 05 #Go to page 0x05
w 90 7C 00 00 00 01 #Swap flag
```

8.5.2.2 Sample Rate Converter

The sample rate converter supports 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz and 96 kHz input sample rates. These input sample rates are converted to 88.2 or 96 kHz sample rate. The sample rate detection doesn't distinguish between sample rates from 32 to 48 kHz. These sample rates are treated as 48 kHz by the sample rate converter. The detected sample rate can be read at book 0x78 page 0x0C register 0x5C. The input sample rate is 88.2 or 96 kHz at register 0x5C which reads 0x00 00 00 01. The input sample rate is 32 to 48 kHz at register 0x5C which reads 0x00 00 00 02. Input sample rate 32 kHz requires changing the interpolation setting from 2x to 3x by writing B0-P0-R37-D7 to 1. The device must be placed in standby mode for this change to take effect.

Table 26. Sample Rate Detection

SAMPLING RATE (KHZ)	B0-P0-R91-D[6:4]
8	001
16	010
32 – 48	011
88.2 – 96	100
176.4 – 192	101
384	110

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Even though the sample rate converter supports 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz and 96 kHz input sample rates, the TAS3251 device supports all input sample rates shown in Table 26 in 1x interpolation mode, base rate processing.

The SRC input should not be overdriven. Making the maximum signal level into the SRC –0.5dBFs is recommended to prevent overdriving the SRC and causing audio artifacts. The input scale and mixer can be used to attenuate or boost the maximum input signal to –0.5dBFs. The processing block has several blocks after the SRC where the signal can be compensate for any gain attenuation done in the input mixer and scale block to prevent over driving the SRC.

8.5.2.3 Parametric Equalizers (PEQ)

The device supports 12 individual tuned PEQs for left channel and 12 individual tuned PEQs for the right channel. The PEQs are implemented using cascaded “direct form 1” BQs structures as shown in Figure 43.

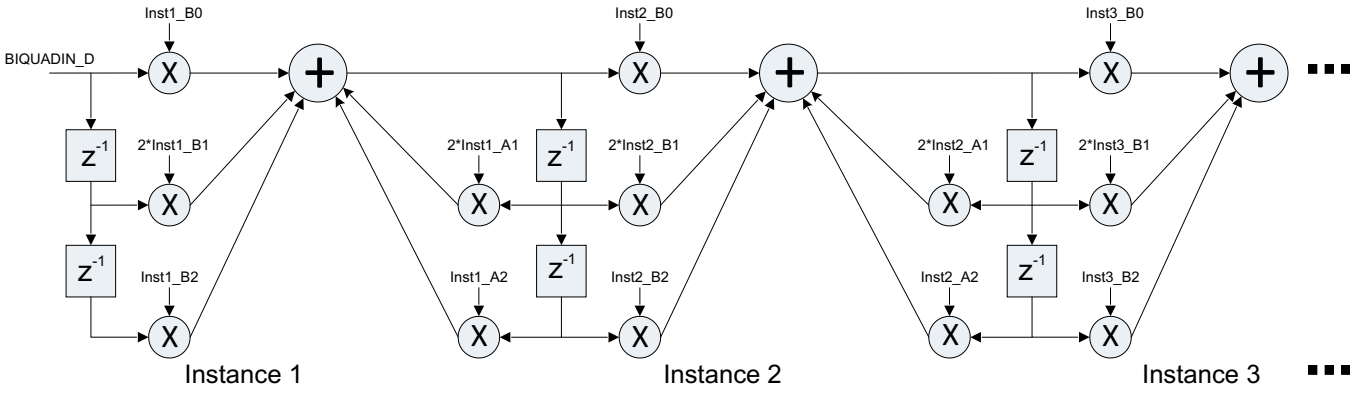

Figure 43. Cascaded BQ Structure

$$H(z) = \frac{b_0 + b_1 Z^{-1} + b_2 Z^{-2}}{a_0 + a_1 Z^{-1} + a_2 Z^{-2}} \quad (2)$$

All BQ coefficients are normalized with a0 to insure that a0 is equal to 1. The structure requires 5 BQ coefficients as shown in Table x. Any BQ with coefficients greater than 1 undergoes gain scaling as described in *BQ Gain Scale*.

Table 27. BQ Coefficients Normalization

BQ COEFFICIENT FOR TAS3251	COEFFICIENT CALCULATION
B0_DSP	b0 / a0
B1_DSP	b1 / (a0 × 2)
B2_DSP	b2 / a0
A1_DSP	–a1 / (a0 × 2)
A2_DSP	–a2 / a0

8.5.2.4 BQ Gain Scale

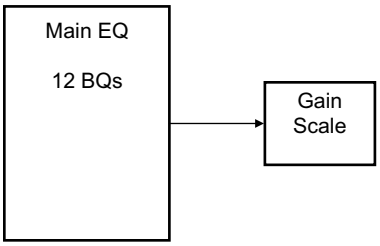

Figure 44. PEQs and BQs Gain Scale Block

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The BQ coefficients format is as follows: The first BQ has B0 = 5.x, B1 = 6.x, B2 = 5.x, A1 = 2.x, and A2 = 1.x. The rest of the BQ have this format: B0 = 1.x, B1 = 2.x, B2 = 1.x, A1 = 2.x, and A2 = 1.x. This formatting maintains the highest possible resolution and noise performance. The 1.31 format restricts the ability to do high gains within the BQs and as a result requires gain compensation for the restriction. When generating BQ coefficients, ensure none of the BQ coefficients is greater than 1 by implementing gain compensation. The Gain compensation reduces the BQ coefficients gain to ensure all BQ coefficients are less than 1. The reduced gain is then reapplied in the subsequent gain scale block.

Gain compensation takes the maximum value of B0_DSP, B1_DSP, and B2_DSP after the BQ normalization shown in Table 27 is implemented. All the B coefficients are divided by maximum B coefficient value then multiplied by 0.999999999534339 (the nearest two's complement 32-bit number to 1). The following calculations are done for each BQ in the PEQ block:

$$Max\_k = \max(B0\_DSP, B1\_DSP, B2\_DSP) \quad (3)$$

$$k\_BQX = Max\_k \quad (4)$$

$$B0\_DSP = \frac{B0\_DSP}{k\_BQX} \quad (5)$$

$$B1\_DSP = \frac{B1\_DSP}{k\_BQX} \quad (6)$$

$$B2\_DSP = \frac{B2\_DSP}{k\_BQX} \quad (7)$$

The calculations above insure all DSP BQ coefficients are in a 1.31 format. The reduced gains in the BQ 1.31 format is compensation for in the gain scale block. The following calculation is done for each channel.

k_BQ = k_BQ1 × k_BQ2 × k_BQ3 × k_BQ4 × k_BQ5 × k_BQ6 × k_BQ7 × k_BQ8 × k_BQ9 × k_BQ10 × k_BQ11 × k_BQ12 (8)

The calculated k_BQ compensation value is then applied to the BQ gain scale in an 8.24 format. The BQ gain scale can also be used for volume control before the DRCs. The block can be considered as *BQ gain scale and volume gain block*. When the BQ gain scale block is used for volume control the coefficient value must be calculated as follows:

$$Gain\_BQ\_V = 10^{\frac{Volume}{20}} \times k\_BQ$$

where

- Volume is in dB (9)

The BQ gain scale coefficients are located in book 0x8C, page 0x21 register 0x4C for left and register 0x50 for right.

The Bypass EQ Mux allows the user to bypass all processing. The Bypass EQ mux is at Page 0x21, Register 0x64. The Gang Left / Right mux forces the left processing to be the same as the right processing. The Gang Left / Right Mux is located at Page 0x21, Register 0x68.

8.5.2.5 Dynamic Parametric Equalizer (DPEQ)

The dynamic parametric equalizer mixes the audio signals routed through two paths containing one BQ each based upon the signal level detected by the sense path, as shown in Figure 45. The sense path contains one BQ, which can be used to focus the DPEQ sensing on a specific frequency bandwidth. An alpha filter structure is used to sense the energy in the sense path and setting the dynamic mixing ratios.

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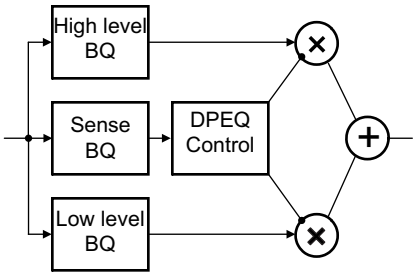

Figure 45. DPEQ Signal Path

The dynamic mixing is controlled by offset, gain, and alpha coefficients in a 1.31 format. The alpha coefficient controls the average time constant in ms of the signal data in the sense path. The offset and gain coefficients control the dynamic mixing thresholds shown in Figure 46.

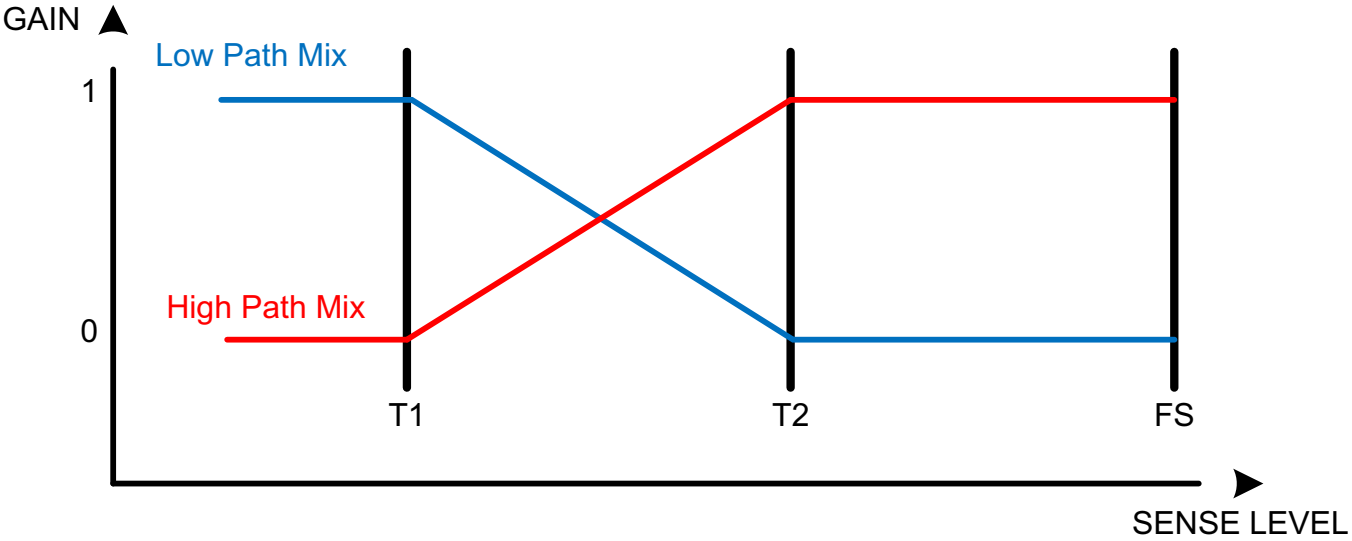

Figure 46. Dynamic Mixing

The offset, gain and alpha coefficients are calculated as follows:

$$T1\_Linear = 10^{\frac{T1}{20}} \quad (10)$$

$$T2\_Linear = 10^{\frac{T2-6}{20}}$$

where

- T2 ≥ –20 dB

(11)

$$T2\_Linear = 10^{\frac{T2}{20}}$$

where

- T2 < –20 dB

(12)

$$Offset = -T1\_Linear \quad (13)$$

$$Gain = \frac{1}{32(T2\_Linear - T1\_Linear)} \quad (14)$$

$$Alpha = 1 - e^{\frac{-1000}{time\ constant \times Fs}}$$

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where

- T1 and T2 are in dB
- The time constant is in ms (15)

The DPEQ control coefficients are located in book 0x8C, page0x20. Register 0x44 is alpha coefficient, register 0x48 is gain coefficient and register 0x4C is offset coefficient.

The high level path BQ, low level path BQ, and sense path BQ coefficients use a 1.31 format as shown in Table 29. The DPEQ BQs don't have a gain scale to compensate for any BQ gain reduction due to the requirements of the 1.31 format. During tuning, the reduced gain can be compensated by using the BQ gain scale or the DRC offset coefficient.

The DPEQ sense gain scale is located in the sensing path. The DPEQ sense gain scale can be used to shift the dynamic mixing thresholds by changing the signal level in the sensing path. A positive dB gain shifts the dynamic mixing thresholds down by the gain amount and a negative dB gain shifts the dynamic mixing thresholds up by the gain amount.

8.5.2.6 Two-Band Dynamic Range Control

The Dynamic Range Control (DRC) is a feed-forward mechanism that can be used to automatically control the audio signal amplitude or the dynamic range within specified limits. The dynamic range control is done by sensing the audio signal level using an estimate of the alpha filter energy then adjusting the gain based on the region and slope parameters that are defined. The Dynamic Range Control is shown in Figure 47.

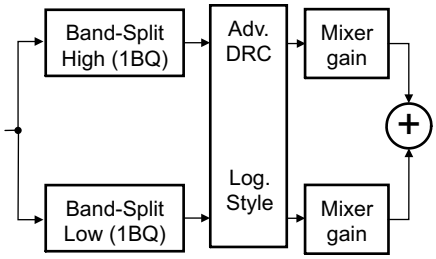

Figure 47. Dynamic Range Control

The DRCs have seven programmable transfer function parameters each: k0, k1, k2, T1, T2, OFF1, and OFF2. The T1 and T2 parameters specify thresholds or boundaries of the three compression or expansion regions in terms of input level. The Parameters k0, k1, and k2 define the gains or slopes of curves for each of the three regions. The parameters OFF1 and OFF2 specify the offset shift relative 1:1 transfer function curve at the thresholds T1 and T2 respectively shown in Figure 48.

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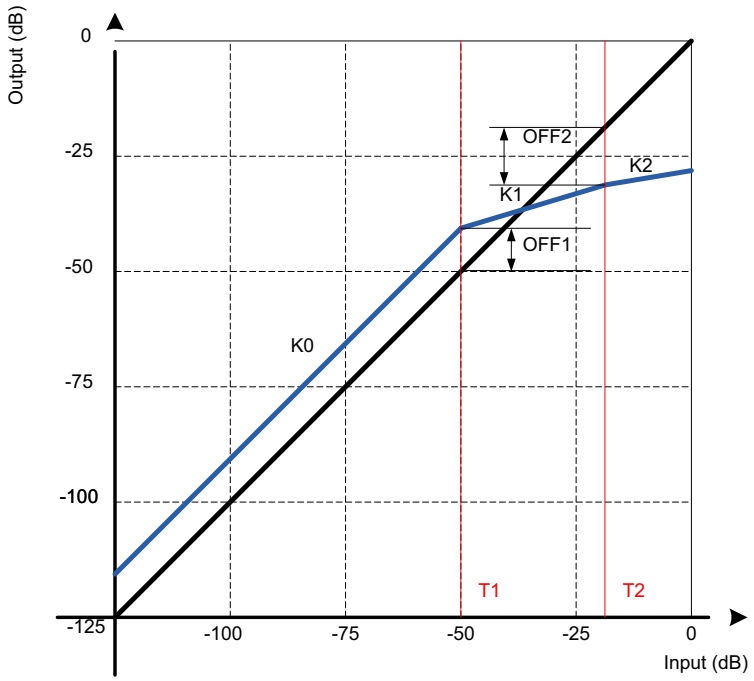

Figure 48. DRC Transfer Function Example Plot

The two-band dynamic range control is comprised of two DRCs that can be spilt into two bands using the BQ at the input of each band. The frequency where the two bands are spilt is referred to as the crossover frequency. The crossover frequency is the cut off frequency for the low pass filter used to create the low band and the cut off frequency for the high pass filter used to create the high band. It is inherent of parallel two-band DRC to have a hump at the crossover region due to the overlap of energy going through both bands of the DRC being summed in the two-band DRC output mixer.

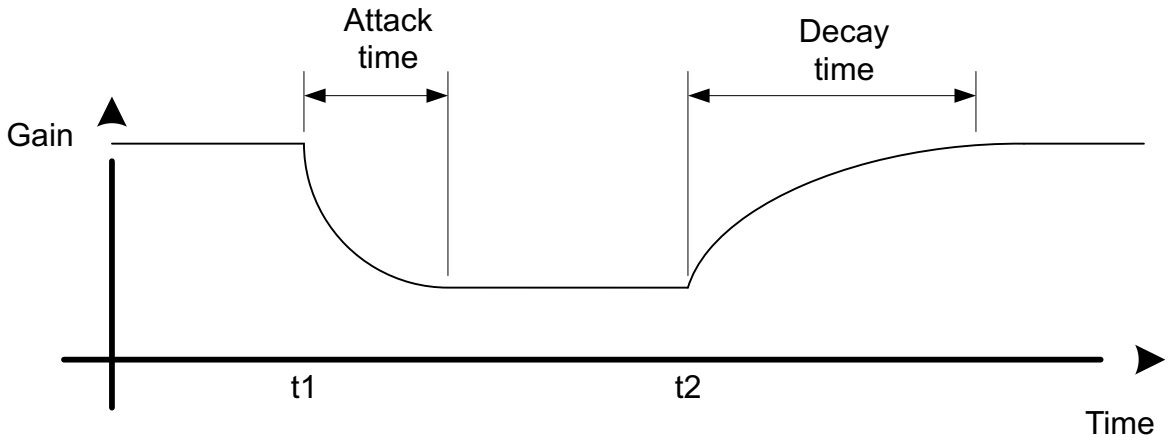

Figure 49. DRC Attack and Decay

The DRC in each band is equipped with individual energy, attack, and decay time constants. The DRC time constants control the transition time of changes and decisions in the DRC gain during compression or expansion. The energy, attack, and decay time constants affect the sensitivity level of the DRC. The shorter the time constant, the more aggressive the DRC response and vice versa.

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8.5.2.7 Automatic Gain Limiter

The Automatic Gain Limiter (AGL) is a feedback mechanism that can be used to automatically control the audio signal amplitude or dynamic range within specified limits. The automatic gain limiting is done by sensing the audio signal level using an alpha filter energy structure shown in Figure 51 at the output of the AGL then adjusting the gain based on the whether the signal level is above or below the defined threshold. Three decisions made by the AGL are engage, disengage, or do nothing. The rate at which the AGL engages or disengages depends on the attack and release settings, respectively.

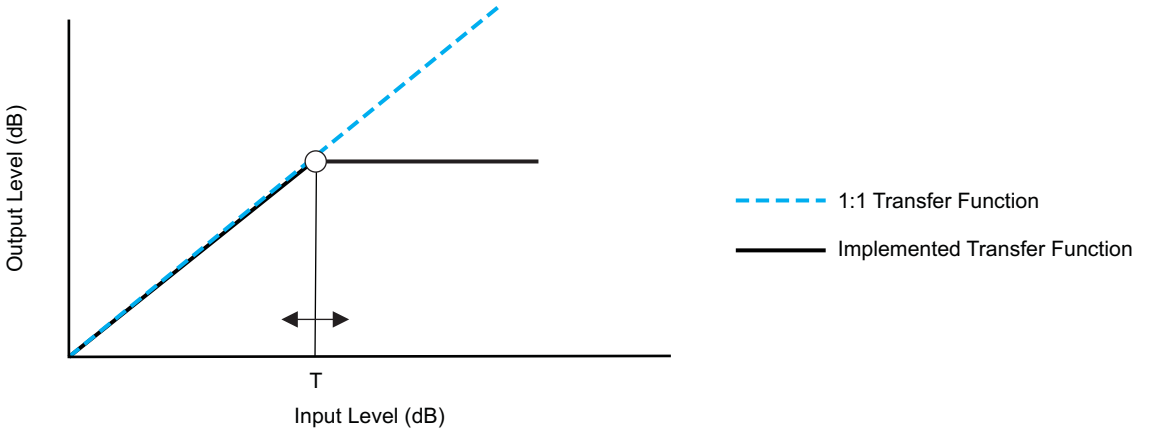

Figure 50. AGL Transfer Function Example Plot

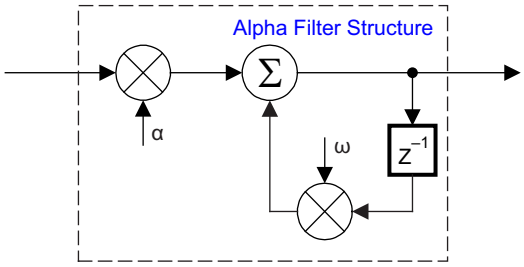

Figure 51. AGL Alpha Filter Structure

8.5.2.7.1 Softening Filter Alpha (AEA)

- AEA = $1 - e^{-1000 / (fs \times User\_AE)}$
- e ≈ 2.718281828
- Fs = sampling frequency
- User_AE = user input step size

8.5.2.7.2 Softening Filter Omega (AEO)

- AEO = 1 – AEA

8.5.2.7.3 Attack Rate

- Attack rate = 2 (AA + Release rate)
- AA = 1000 × User_Ad / Fs
- User_Ad = user input attack step size

8.5.2.7.4 Release Rate

- Release rate = 1000 × User_Rd / Fs
- User_Rd = user input release step size

NOTE

The release duration (User_Rd) should be longer than the attack duration (User_Ad).

8.5.2.7.5 Attack Threshold

- Attack Threshold = user input level in dB

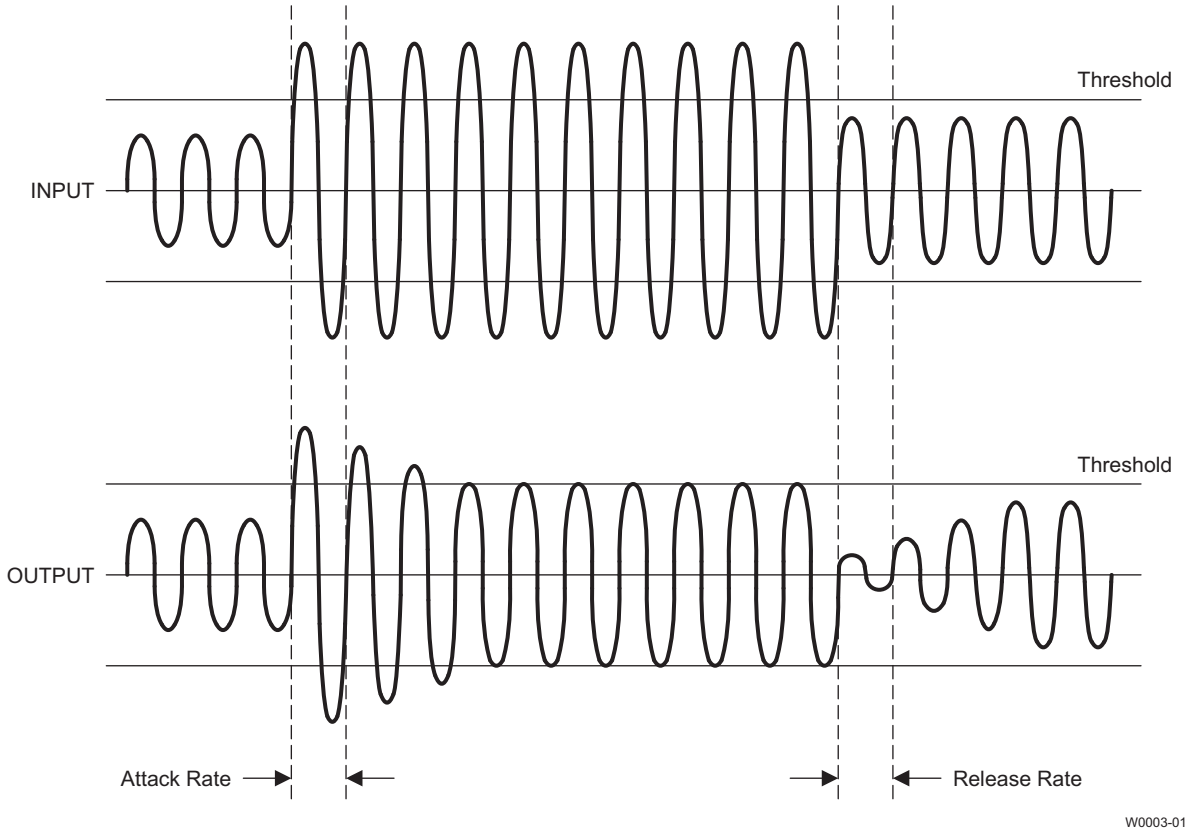

Figure 52. AGL Attack and Release

The Attack Threshold AGL coefficients are shown in .

8.5.2.8 Fine Volume

The fine volume block after the AGL can be used to provide additional fine volume steps from –192 dB to 6 dB in a 2.30 format. The Fine Coefficients are shown in .

8.5.2.9 THD Boost

A boost scaler and fine volume together can be used for clipping. The THD boost block allows the user to programmatically increase the THD by clipping at an operating point earlier than that defined by the supply rails.

8.5.2.10 Level Meter

The level meter uses an energy estimator with a programmable time constant to adjust the sensitivity level based on signal frequency and desired accuracy level. The level meter outputs of both left and right channels are written to a 32-bit sub address location in a 1.31 format as shown in . The BypassTo Level Meter Bit in Book 8C, Page 0x21, Register 0x70 can be used to switch the input to the Level Meter from the audio before processing to audio post-processing.

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8.5.3 Other Processing Block Features

8.5.3.1 Number Format

The data processing path is 32 bits with 32-bit coefficients. The coefficients use the two's complement digital number format.

Table 28. Two's Complement Format

BITS	TWO'S COMPLEMENT VALUE
0111 1111	127
0111 1110	126
0000 0010	2
0000 0001	1
0000 0000	0
1111 1111	–1
1111 1110	–2
1000 0010	–126
1000 0001	–127
1000 0000	–128

8.5.3.1.1 Coefficient Format Conversion

The device uses 32 bit two's complement number formats. The calculated 4 byte register values are shown below in an 8 digit hex value.

Table 29. Sample Calculations for 1.31 Format

dB	Linear	Decimal	Hex (1.31 Format)
0	1	2147483648	7FFFFFFF
–6	0.5	1073741824	40000000
–20	0.1	214748364	0CCCCCCC
x	$L = 10^{(x/20)}$	$D = 2^{31} \times L$, $D < 2^{31}$ $D = 2^{31}$, $D \geq 2^{31}$	Dec2Hex(D, 8) (1)

(1) Dec2Hex(D, 8), where 8 represents 8 nibbles or 38 bits.

Please note that for a 1.31 format the linear value cannot be greater than 1 or decimal value 232.

Table 30. Sample Calculations for B.A Format

dB	Linear	Decimal	Hex (1.31 Format)
x	$L = 10^{(x/20)}$	$D = 2^{A} \times L$, $D < 2^{(B + A - 1)}$ $D = 2^{(B + A - 1)}$, $D \geq 2^{(B + A - 1)}$	Dec2Hex(D, 8)

8.5.4 Checksum

The TAS3251 device supports two different check sum schemes, a cyclic redundancy check (CRC) checksum and an Exclusive (XOR) checksum. Both checksums work on every register write, except for *book switch register* and *page switching register*, 0x7F and 0x00, respectively. Register reads do not change checksum, but writes to even nonexistent registers will change the checksum. Both checksums are 8-bit checksums and both are available together simultaneously. The checksums can be reset by writing a starting value (eg. 0x 00 00 00 00) to their respective 4-byte register locations.

8.5.4.1 Cyclic Redundancy Check (CRC) Checksum

The 8-bit CRC checksum used is the 0x7 polynomial (CRC-8-CCITT I.432.1; ATM HEC, ISDN HEC and cell delineation, $(1 + x^1 + x^2 + x^8)$. A major advantage of the CRC checksum is that it is input order sensitive.

The CRC supports all I^2C transactions, excluding book and page switching. The CRC checksum is read from register 0x7E on any page of book 0x00 (B0_Page x_Reg 126). If the book isn't Book 0, the CRC checksum is only valid on page 0x00 register 0x7E (Page 0_Reg 126). The CRC checksum can be reset by writing 0x00 00 00 00 to the same register locations where the CRC checksum is valid.

8.5.4.2 Exclusive or (XOR) Checksum

The Xor checksum is a simpler checksum scheme. It performs sequential XOR of each register byte write with the previous 8-bit checksum register value. XOR supports only YMEM, which is located in Book 0x8C and excludes page switching and all registers in Page 0x00 of Book 0x8C. XOR checksum is read from location register 0x7D on page 0x00 of book 0x8C (B140_Page 0_Reg 125). The XOR Checksum can be reset by writing 0x00 00 00 00 to the same register location where it is read.

Table 31. XOR Truth Table

INPUT		OUTPUT
A	B	
0	0	0
0	1	1
1	0	1
1	1	0

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8.6 Register Maps

8.6.1 Registers - Page 0

8.6.1.1 Register 1 (0x01)

Figure 53. Register 1 (0x01)

7	6	5	4	3	2	1	0
Reserved			RSTM	Reserved			RSTR
R/W			R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. Register 1 (0x01) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved			Reserved
4	RSTM	R/W	0	Reset Modules – This bit resets the interpolation filter and the DAC modules. Since the DSP is also reset, the coeffient RAM content will also be cleared by the DSP. This bit is auto cleared and can be set only in standby mode. 0: Normal 1: Reset modules
3-1	Reserved			Reserved
0	RSTR	R/W	0	Reset Registers – This bit resets the mode registers back to their initial values. The RAM content is not cleared, but the execution source will be back to ROM. This bit is auto cleared and must be set only when the DAC is in standby mode (resetting registers when the DAC is running is prohibited and not supported). 0: Normal 1: Reset mode registers

8.6.1.2 Register 2 (0x02)

Figure 54. Register 2 (0x02)

7	6	5	4	3	2	1	0
DSPR	Reserved		RQST	Reserved			RQPD
R/W	R/W		R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. Register 2 (0x02) Field Descriptions

Bit	Field	Type	Reset	Description
7	DSPR	R/W	1	DSP reset – When the bit is made 0, DSP will start powering up and send out data. This needs to be made 0 only after all the input clocks are (ASI,MCLK,PLLCLK) are settled so that DMA channels do not go out of sync. 0: Normal operation 1: Reset the DSP
6-5	Reserved	R/W		Reserved
4	RQST	R/W	0	Standby Request – When this bit is set, the DAC will be forced into a system standby mode, which is also the mode the system enters in the case of clock errors. In this mode, most subsystems will be powered down but the charge pump and digital power supply. 0: Normal operation 1: Standby mode
3-1	Reserved	R/W		Reserved

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Table 33. Register 2 (0x02) Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RQPD	R/W	0	Powerdown Request – When this bit is set, the DAC will be forced into powerdown mode, in which the power consumption would be minimum as the charge pump is also powered down. However, it will take longer to restart from this mode. This mode has higher precedence than the standby mode, i.e. setting this bit along with bit 4 for standby mode will result in the DAC going into powerdown mode. 0: Normal operation 1: Powerdown mode

8.6.1.3 Register 3 (0x03)

Figure 55. Register 3 (0x03)

7	6	5	4	3	2	1	0
Reserved			RQML	Reserved			RQMR
RO			R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. Register 3 (0x03) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	RO		Reserved
4	RQML	R/W	0	Mute Left Channel – This bit issues soft mute request for the left channel. The volume will be smoothly ramped down/up to avoid pop/click noise. 0: Normal volume 1: Mute
3-1	Reserved	R/W		Reserved
0	RQMR	R/W	0	Mute Right Channel – This bit issues soft mute request for the right channel. The volume will be smoothly ramped down/up to avoid pop/click noise. 0: Normal volume 1: Mute

8.6.1.4 Register 4 (0x04)

Figure 56. Register 4 (0x04)

7	6	5	4	3	2	1	0
Reserved			PLCK	Reserved			PLLE
R/W			R	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. Register 4 (0x04) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W		Reserved
4	PLCK	R	0	PLL Lock Flag – This bit indicates whether the PLL is locked or not. When the PLL is disabled this bit always shows that the PLL is not locked. 0: The PLL is locked 1: The PLL is not locked
3-1	Reserved	R/W		Reserved
0	PLLE	R/W	1	PLL Enable – This bit enables or disables the internal PLL. When PLL is disabled, the master clock will be switched to the MCLK. 0: Disable PLL 1: Enable PLL

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8.6.1.5 Register 6 (0x06)

Figure 57. Register 6 (0x06)

7	6	5	4	3	2	1	0
Reserved				DBPG	Reserved		
R/W				R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 36. Register 6 (0x06) Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved		0	Reserved
3	DBPG	R/W	0	Page auto increment disable – Disable page auto increment mode. for non -zero books. When end of page is reached it goes back to 8th address location of next page when this bit is 0. When this bit is 1 it goes to 0 th location of current page itself like in older part. 0: Enable Page auto increment 1: Disable Page auto increment
2-0	Reserved	R/W	0	Reserved

8.6.1.6 Register 7 (0x07)

Figure 58. Register 7 (0x07)

7	6	5	4	3	2	1	0
Reserved			DEMP	Reserved			SDSL
R/W			R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 37. Register 7 (0x07) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	DEMP	R/W	0	De-Emphasis Enable – This bit enables or disables the de-emphasis filter. The default coefficients are for 44.1 kHz sampling rate, but can be changed by reprogramming the appropriate coeffients in RAM. 0: De-emphasis filter is disabled 1: De-emphasis filter is enabled
3-1	Reserved	R/W	0	Reserved
0	SDSL	R/W	1	SDOUT Select – This bit selects what is being output as SDOUT via the SDOUT pin. 0: SDOUT is the DSP output (post-processing) 1: SDOUT is the DSP input (pre-processing)

8.6.1.7 Register 8 (0x08)

Figure 59. Register 8 (0x08)

7	6	5	4	3	2	1	0
Reserved		G2OE	MUTEOE	Reserved			
R/W		R/W	R/W	R/W			

Table 38. Register 8 (0x08) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W		Reserved
5	G2OE	R/W	0	SDOUT Output Enable – This bit sets the direction of the SDOUT pin 0: SDOUT is input 1: SDOUT is output

Table 38. Register 8 (0x08) Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	MUTEOE	R/W	0	MUTE Control Enable – This bit sets an enable of MUTE control from PCM to TPA 0: MUTE control disable 1: MUTE control enable
3-0	Reserved	R/W	0	Reserved

8.6.1.8 Register 9 (0x09)

Figure 60. Register 9 (0x09)

7	6	5	4	3	2	1	0
Reserved		SCLKP	SCLKO	Reserved			LRCLKFSO
R/W		R/W	R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 39. Register 9 (0x09) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved			Reserved
5	SCLKP	R/W	0	SCLK Polarity – This bit sets the inverted SCLK mode. In inverted SCLK mode, the DAC assumes that the LRCLK and DIN edges are aligned to the rising edge of the SCLK. Normally they are assumed to be aligned to the falling edge of the SCLK. 0: Normal SCLK mode 1: Inverted SCLK mode
4	SCLKO	R/W	0	SCLK Output Enable – This bit sets the SCLK pin direction to output for I2S master mode operation. In I2S master mode the PCM51xx outputs the reference SCLK and LRCLK, and the external source device provides the DIN according to these clocks. Use P0-R32 to program the division factor of the MCLK to yield the desired SCLK rate (normally 64 FS) 0: SCLK is input (I2S slave mode) 1: SCLK is output (I2S master mode)
3-1	Reserved			Reserved
0	LRKO	R/W	0	LRCLK Output Enable – This bit sets the LRCLK pin direction to output for I2S master mode operation. In I2S master mode the PCM51xx outputs the reference SCLK and LRCLK, and the external source device provides the DIN according to these clocks. Use P0-R33 to program the division factor of the SCLK to yield 1 FS for LRCLK. 0: LRCLK is input (I2S slave mode) 1: LRCLK is output (I2S master mode)

8.6.1.9 Register 12 (0x0C)

Figure 61. Register 12 (0x0C)

7	6	5	4	3	2	1	0
Reserved						RSCLK	RLRK
R/W						R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 40. Register 12 (0x0C) Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R/W		Reserved
1	RSCLK	R/W	0	Master Mode SCLK Divider Reset – This bit, when set to 0, will reset the MCLK divider to generate SCLK clock for I2S master mode. To use I2S master mode, the divider must be enabled and programmed properly. 0: Master mode SCLK clock divider is reset 1: Master mode SCLK clock divider is functional

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Table 40. Register 12 (0x0C) Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RLRK	R/W	1	Master Mode LRCLK Divider Reset – This bit, when set to 0, will reset the SCLK divider to generate LRCLK clock for I2S master mode. To use I2S master mode, the divider must be enabled and programmed properly. 0: Master mode LRCLK clock divider is reset 1: Master mode LRCLK clock divider is functional

8.6.1.10 Register 13 (0x0D)

Figure 62. Register 13 (0x0D)

7	6	5	4	3	2	1	0
Reserved			SREF	Reserved	SDSP		
R/W			R/W	R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 41. Register 13 (0x0D) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W		Reserved
4	SREF	R/W	0	DSP clock source – This bit select the source clock for internal PLL. This bit is ignored and overriden in clock auto set mode. 0: The PLL reference clock is MCLK 1: The PLL reference clock is SCLK 010: The PLL reference clock is oscillator clock 011: The PLL reference clock is GPIO (selected using P0-R18) Others: Reserved (PLL reference is muted)
3	Reserved	R/W		Reserved
2-0	SDSP	R/W	0	DAC clock source – These bits select the source clock for DSP clock divider. 000: Master clock (PLL/MCLK and OSC auto-select) 001: PLL clock 010: OSC clock 011: MCLK clock 100: SCLK clock 101: GPIO (selected using P0-R16) Others: Reserved (muted)

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8.6.1.11 Register 14 (0x0E)

Figure 63. Register 14 (0x0E)

7	6	5	4	3	2	1	0
Reserved	SDAC			Reserved	SOSR		
R/W	R/W			R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 42. Register 14 (0x0E) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
6-4	SDAC	R/W	0	DAC clock source – These bits select the source clock for DAC clock divider. 000: Master clock (PLL/MCLK and OSC auto-select) 001: PLL clock 010: OSC clock 011: MCLK clock 100: SCLK clock 101: GPIO (selected using P0-R16) Others: Reserved (muted)
3	Reserved	R/W	0	Reserved
2-0	SOSR	R/W	0	OSR clock source – These bits select the source clock for OSR clock divider. 000: DAC clock 001: Master clock (PLL/MCLK and OSC auto-select) 010: PLL clock 011: OSC clock 100: MCLK clock 101: SCLK clock 110: GPIO (selected using P0-R17) Others: Reserved (muted)

8.6.1.12 Register 15 (0x0F)

Figure 64. Register 15 (0x0F)

7	6	5	4	3	2	1	0
Reserved					SNCP		
R/W					R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 43. Register 15 (0x0F) Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved	R/W		Reserved
2-0	SNCP	R/W	0	NCP clock source – These bits select the source clock for CP clock divider. 000: DAC clock 001: Master clock (PLL/MCLK and OSC auto-select) 010: PLL clock 011: OSC clock 100: MCLK clock 101: SCLK clock 110: GPIO (selected using P0-R17) Others: Reserved (muted)

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8.6.1.13 Register 16 (0x10)

Figure 65. Register 16 (0x10)

7	6	5	4	3	2	1	0
Reserved	GDSP			Reserved	GDAC		
R/W	R/W			R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 44. Register 16 (0x10) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
6-4	GDSP	R/W	0	GPIO Source for uCDSP clk – These bits select the SDOUT pin as clock input source when GPIO is selected as DSP clock divider source. 000: N/A 001: N/A 010: N/A 011: N/A 100: N/A 101: SDOUT Others: Reserved (muted)
3	Reserved	R/W	0	Reserved
2-0	GDAC	R/W	0	GPIO Source for DAC clk – These bits select the SDOUT pin as clock input source when GPIO is selected as DAC clock divider source. 000: N/A 001: N/A 010: N/A 011: N/A 100: N/A 101: SDOUT Others: Reserved (muted)

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8.6.1.14 Register 17 (0x11)

Figure 66. Register 17 (0x11)

7	6	5	4	3	2	1	0
Reserved	GNCP			Reserved	GOSR		
R/W	R/W			R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 45. Register 17 (0x11) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
6-4	GNCP	R/W	0	GPIO Source for NCP clk – These bits select the SDOUT pin as clock input source when GPIO is selected as CP clock divider source 000: N/A 001: N/A 010: N/A 011: N/A 100: N/A 101: SDOUT Others: Reserved (muted)
3	Reserved	R/W	0	Reserved
2-0	GOSR	R/W	0	GPIO Source for OSR clk – These bits select the SDOUT pin as clock input source when GPIO is selected as OSR clock divider source. 000: N/A 001: N/A 010: N/A 011: N/A 100: N/A 101: SDOUT Others: Reserved (muted)

8.6.1.15 Register 18 (0x12)

Figure 67. Register 18 (0x12)

7	6	5	4	3	2	1	0
Reserved						GREF	
R/W						R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 46. Register 18 (0x12) Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved	R/W	0	Reserved
2-0	GREF	R/W	0	GPIO Source for PLL reference clk – These bits select the SDOUT pin as clock input source when GPIO is selected as the PLL reference clock source. 000: N/A 001: N/A 010: N/A 011: N/A 100: N/A 101: SDOUT Others: Reserved (muted)

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8.6.1.16 Register 20 (0x14)

Figure 68. Register 20 (0x14)

7	6	5	4	3	2	1	0
Reserved				PPDV			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 47. Register 20 (0x14) Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R/W	0	Reserved
3-0	PPDV	R/W	0	PLL P – These bits set the PLL divider P factor. These bits are ignored in clock auto set mode. 0000: P=1 0001: P=2 ... 1110: P=15 1111: Prohibited (do not set this value)

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8.6.1.17 Register 21 (0x15)

Figure 69. Register 21 (0x15)

7	6	5	4	3	2	1	0
Reserved		PJDV					
R/W		R/W					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 48. Register 21 (0x15) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved		0	Reserved
5-0	PJDV	R/W	001000	PLL J – These bits set the J part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode. 000000: Prohibited (do not set this value) 000001: J=1 000010: J=2 ... 111111: J=63

8.6.1.18 Register 22 (0x16)

Figure 70. Register 22 (0x16)

7	6	5	4	3	2	1	0
Reserved		PDDV					
R/W		R/W					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 49. Register 22 (0x16) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W		Reserved
5-0	PDDV	R/W	0	PLL D (MSB) – These bits set the D part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode. 0 (in decimal): D=0000 1 (in decimal): D=0001 ... 9999 (in decimal): D=9999 Others: Prohibited (do not set)

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8.6.1.19 Register 23 (0x17)

Figure 71. Register 23 (0x17)

7	6	5	4	3	2	1	0
PDDV							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 50. Register 23 (0x17) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PDDV	R/W	0	PLL D (LSB) – These bits set the D part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode. 0 (in decimal): D=0000 1 (in decimal): D=0001 ... 9999 (in decimal): D=9999 Others: Prohibited (do not set)

8.6.1.20 Register 24 (0x18)

Figure 72. Register 24 (0x18)

7	6	5	4	3	2	1	0
Reserved				PRDV			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 51. Register 24 (0x18) Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R/W		Reserved
3-0	PRDV	R/W	0	PLL R – These bits set the R part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode. 0000: R=1 0001: R=2 ... 1111: R=16

8.6.1.21 Register 27 (0x1B)

Figure 73. Register 27 (0x1B)

7	6	5	4	3	2	1	0
Reserved	DDSP						
R/W	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 52. Register 27 (0x1B) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W		Reserved
6-0	DDSP	R/W	0	DSP Clock Divider – These bits set the source clock divider value for the DSP clock. These bits are ignored in clock auto set mode. 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128

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8.6.1.22 Register 28 (0x1C)

Figure 74. Register 28 (0x1C)

7	6	5	4	3	2	1	0
Reserved	DDAC						
R/W	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 53. Register 28 (0x1C) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved			Reserved
6-4	DDAC	R/W	0	DAC Clock Divider – These bits set the source clock divider value for the DAC clock. These bits are ignored in clock auto set mode. 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128
3-0		R/W	1	

8.6.1.23 Register 29 (0x1D)

Figure 75. Register 29 (0x1D)

7	6	5	4	3	2	1	0
Reserved	DNCP						
R/W	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 54. Register 29 (0x1D) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved			Reserved
6-2	DNCP	R/W	0	NCP Clock Divider – These bits set the source clock divider value for the CP clock. These bits are ignored in clock auto set mode. 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128
1-0		R/W	1	

8.6.1.24 Register 30 (0x1E)

Figure 76. Register 30 (0x1E)

7	6	5	4	3	2	1	0
Reserved	DOSR						
R/W	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 55. Register 30 (0x1E) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved			Reserved
6-4	DOSR	R/W	0	OSR Clock Divider – These bits set the source clock divider value for the OSR clock. These bits are ignored in clock auto set mode. 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128
3-0		R/W	1	

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8.6.1.25 Register 32 (0x20)

Figure 77. Register 32 (0x20)

7	6	5	4	3	2	1	0
Reserved	DSCLK						
R/W	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 56. Register 32 (0x20) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W		Reserved
6-0	DSCLK	R/W	0	Master Mode SCLK Divider – These bits set the MCLK divider value to generate I2S master SCLK clock. 0000000: Divide by 1 0000001: Divide by 2 ... 1111111: Divide by 128

8.6.1.26 Register 33 (0x21)

Figure 78. Register 33 (0x21)

7	6	5	4	3	2	1	0
DLRK							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 57. Register 33 (0x21) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DLRK	R/W	0	Master Mode LRCLK Divider – These bits set the I2S master SCLK clock divider value to generate I2S master LRCLK clock 00000000: Divide by 1 00000001: Divide by 2 ... 11111111: Divide by 256

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8.6.1.27 Register 34 (0x22)

Figure 79. Register 34 (0x22)

7	6	5	4	3	2	1	0
Reserved			I16E	Reserved	FSSP	FSSP	
R/W			R/W	R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 58. Register 34 (0x22) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W		Reserved
4	I16E	R/W	0	16x Interpolation – This bit enables or disables the 16x interpolation mode 0: 8x interpolation 1: 16x interpolation
3	Reserved	R/W		Reserved
2	FSSP	R/W	1	FS Speed Mode – These bits select the FS operation mode, which must be set according to the current audio sampling rate. These bits are ignored in clock auto set mode. 000: Reserved 001: Reserved 010: Reserved 011: 48 kHz 100: 88.2-96 kHz 101: Reserved 110: Reserved 111: 32kHz
1-0		R/W	0	

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8.6.1.28 Register 37 (0x25)

Figure 80. Register 37 (0x25)

7	6	5	4	3	2	1	0
Reserved	IDFS	IDBK	IDSK	IDCH	IDCM	DCAS	IPLK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 59. Register 37 (0x25) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W		Reserved
6	IDFS	R/W	0	Ignore FS Detection – This bit controls whether to ignore the FS detection. When ignored, FS error will not cause a clock error. 0: Regard FS detection 1: Ignore FS detection
5	IDBK	R/W	0	Ignore SCLK Detection – This bit controls whether to ignore the SCLK detection against LRCLK. The SCLK must be stable between 32 FS and 256 FS inclusive or an error will be reported. When ignored, a SCLK error will not cause a clock error. 0: Regard SCLK detection 1: Ignore SCLK detection
4	IDSK	R/W	0	Ignore MCLK Detection – This bit controls whether to ignore the MCLK detection against LRCLK. Only some certain MCLK ratios within some error margin are allowed. When ignored, an MCLK error will not cause a clock error. 0: Regard MCLK detection 1: Ignore MCLK detection
3	IDCH	R/W	0	Ignore Clock Halt Detection – This bit controls whether to ignore the MCLK halt (static or frequency is lower than acceptable) detection. When ignored an MCLK halt will not cause a clock error. 0: Regard MCLK halt detection 1: Ignore MCLK halt detection
2	IDCM	R/W	0	Ignore LRCLK/SCLK Missing Detection – This bit controls whether to ignore the LRCLK/SCLK missing detection. The LRCLK/SCLK need to be in low state (not only static) to be deemed missing. When ignored an LRCLK/SCLK missing will not cause the DAC go into powerdown mode. 0: Regard LRCLK/SCLK missing detection 1: Ignore LRCLK/SCLK missing detection
1	DCAS	R/W	0	Disable Clock Divider Autoset – This bit enables or disables the clock auto set mode. When dealing with uncommon audio clock configuration, the auto set mode must be disabled and all clock dividers must be set manually. Addtionally, some clock detectors might also need to be disabled. The clock autoset feature will not work with PLL enabled in VCOM mode. In this case this feature has to be disabled and the clock dividers must be set manually. 0: Enable clock auto set 1: Disable clock auto set
0	IPLK	R/W	0	Ignore PLL Lock Detection – This bit controls whether to ignore the PLL lock detection. When ignored, PLL unlocks will not cause a clock error. The PLL lock flag at P0-R4, bit 4 is always correct regardless of this bit. 0: PLL unlocks raise clock error 1: PLL unlocks are ignored

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8.6.1.29 Register 40 (0x28)

Figure 81. Register 40 (0x28)

7	6	5	4	3	2	1	0
Reserved		AFMT		Reserved		ALEN	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 60. Register 40 (0x28) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	–			
5-4	AFMT	R/W	0	I2S Data Format – These bits control both input and output audio interface formats for DAC operation. 00: I2S 01: DSP 10: RTJ 11: LTJ
3-2	Reserved	R/W		Reserved
1	ALEN	R/W	1	I2S Word Length – These bits control both input and output audio interface sample word lengths for DAC operation. 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits
0		R/W	0	

8.6.1.30 Register 41 (0x29)

Figure 82. Register 41 (0x29)

7	6	5	4	3	2	1	0
AOFS							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 61. Register 41 (0x29) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AOFS	R/W	0	I2S Shift – These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of SCLK from the starting (MSB) of audio frame to the starting of the desired audio sample. 00000000: offset = 0 SCLK (no offset) 00000001: ofsset = 1 SCLK 00000010: offset = 2 SCLKs … 11111111: offset = 256 SCLKs

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8.6.1.31 Register 42 (0x2A)

Figure 83. Register 42 (0x2A)

7	6	5	4	3	2	1	0
Reserved		AUPL		Reserved		AUPR	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 62. Register 42 (0x2A) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W		Reserved
5	AUPL	R/W	0	Left DAC Data Path – These bits control the left channel audio data path connection. 00: Zero data (mute) 01: Left channel data 10: Right channel data 11: Reserved (do not set)
4		R/W	1	
3-2	Reserved	R/W		Reserved
1	AUPR	R/W	0	Right DAC Data Path – These bits control the right channel audio data path connection. 00: Zero data (mute) 01: Right channel data 10: Left channel data 11: Reserved (do not set)
0		R/W	1	

8.6.1.32 Register 43 (0x2B)

Figure 84. Register 43 (0x2B)

7	6	5	4	3	2	1	0
Reserved				PSEL			
R/W				R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 63. Register 43 (0x2B) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W		Reserved
4-1	PSEL	R/W	0	DSP Program Selection – These bits select the DSP program to use for audio processing. 00000: Reserved 00001: Rom Mode 1 00010: Reserved 00011: Reserved
0		R/W	1	

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8.6.1.33 Register 44 (0x2C)

Figure 85. Register 44 (0x2C)

7	6	5	4	3	2	1	0
Reserved					CMDP		
R/W					R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 64. Register 44 (0x2C) Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved			Reserved
2-0	CMDP	R/W	0	Clock Missing Detection Period – These bits set how long both SCLK and LRCLK keep low before the audio clocks deemed missing and the DAC transitions to powerdown mode. 000: about 1 second 001: about 2 seconds 010: about 3 seconds ... 111: about 8 seconds

8.6.1.34 Register 59 (0x3B)

Figure 86. Register 59 (0x3B)

7	6	5	4	3	2	1	0
Reserved	AMTL			Reserved	AMTR		
R/W	R/W			R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 65. Register 59 (0x3B) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W		Reserved
6-4	AMTL	R/W	0	Auto Mute Time for Left Channel – These bits specify the length of consecutive zero samples at left channel before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec
3	Reserved	R/W		Reserved
2-0	AMTR	R/W	0	Auto Mute Time for Right Channel – These bits specify the length of consecutive zero samples at right channel before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec

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8.6.1.35 Register 60 (0x3C)

Figure 87. Register 60 (0x3C)

7	6	5	4	3	2	1	0
Reserved						PCTL	
R/W						R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 66. Register 60 (0x3C) Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R/W	0	Reserved
1-0	PCTL	R/W	0	Digital Volume Control – These bits control the behavior of the digital volume. 00: The volume for Left and right channels are independent 01: Right channel volume follows left channel setting

8.6.1.36 Register 61 (0x3D)

Figure 88. Register 61 (0x3D)

7	6	5	4	3	2	1	0
VOLL							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 67. Register 61 (0x3D) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VOLL	R/W	00110000	Left Digital Volume – These bits control the left channel digital volume. The digital volume is 24 dB to –103 dB in –0.5 dB step. 00000000: +24.0 dB 00000001: +23.5 dB … 00101111: +0.5 dB 00110000: 0.0 dB 00110001: –0.5 dB ... 11111110: –103 dB 11111111: Mute

8.6.1.37 Register 62 (0x3E)

Figure 89. Register 62 (0x3E)

7	6	5	4	3	2	1	0
VOLR							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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Table 68. Register 62 (0x3E) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VOLR	R/W	00110000	Right Digital Volume – These bits control the right channel digital volume. The digital volume is 24 dB to –103 dB in –0.5 dB step. 00000000: +24.0 dB 00000001: +23.5 dB … 00101111: +0.5 dB 00110000: 0.0 dB 00110001: –0.5 dB ... 11111110: –103 dB 11111111: Mute

8.6.1.38 Register 63 (0x3F)

Figure 90. Register 63 (0x3F)

7	6	5	4	3	2	1	0
VNDF		VNDS		VNUF		VNUS	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 69. Register 63 (0x3F) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VNDF	R/W	00	Digital Volume Normal Ramp Down Frequency – These bits control the frequency of the digital volume updates when the volume is ramping down. The setting here is applied to soft mute request, asserted by XSMUTE pin or P0-R3. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	VNDS	R/W	11	Digital Volume Normal Ramp Down Step – These bits control the step of the digital volume updates when the volume is ramping down. The setting here is applied to soft mute request, asserted by XSMUTE pin or P0-R3. 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update
3-2	VNUF	R/W	00	Digital Volume Normal Ramp Up Frequency – These bits control the frequency of the digital volume updates when the volume is ramping up. The setting here is applied to soft unmute request, asserted by XSMUTE pin or P0-R3. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly restore the volume (Instant unmute)
1-0	VNUS	R/W	11	Digital Volume Normal Ramp Up Step – These bits control the step of the digital volume updates when the volume is ramping up. The setting here is applied to soft unmute request, asserted by XSMUTE pin or P0-R3. 00: Increment by 4 dB for each update 01: Increment by 2 dB for each update 10: Increment by 1 dB for each update 11: Increment by 0.5 dB for each update

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8.6.1.39 Register 64 (0x40)

Figure 91. Register 64 (0x40)

7	6	5	4	3	2	1	0
VEDF		VEDS		Reserved			
R/W		R/W		R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 70. Register 64 (0x40) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VEDF	R/W	0	Digital Volume Emergency Ramp Down Frequency – These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	VEDS	R/W	1	Digital Volume Emergency Ramp Down Step – These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute. 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update
3-0	Reserved	R/W		Reserved

8.6.1.40 Register 65 (0x41)

Figure 92. Register 65 (0x41)

7	6	5	4	3	2	1	0
Reserved					ACTL	AMLE	AMRE
R/W					R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 71. Register 65 (0x41) Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved	R/W		Reserved
2	ACTL	R/W	1	Auto Mute Control**NOBUS** – This bit controls the behavior of the auto mute upon zero sample detection. The time length for zero detection is set with P0-R59. 0: Auto mute left channel and right channel independently. 1: Auto mute left and right channels only when both channels are about to be auto muted.
1	AMLE	R/W	1	Auto Mute Left Channel**NOBUS** – This bit enables or disables auto mute on right channel. Note that when right channel auto mute is disabled and the P0-R65, bit 2 is set to 1, the left channel will also never be auto muted. 0: Disable right channel auto mute 1: Enable right channel auto mute
0	AMRE	R/W	1	Auto Mute Right Channel**NOBUS** – This bit enables or disables auto mute on left channel. Note that when left channel auto mute is disabled and the P0-R65, bit 2 is set to 1, the right channel will also never be auto muted. 0: Disable left channel auto mute 1: Enable left channel auto mute

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8.6.1.41 Register 67 (0x43)

Figure 93. Register 67 (0x43)

7	6	5	4	3	2	1	0
DLPA		DRPA		DLPM		DRPM	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 72. Register 67 (0x43) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DLPA	R/W	0	Left DAC primary AC dither gain – These bits control the AC dither gain for left channel primary DAC modulator. 00: AC dither gain = 0.125 01: AC dither gain = 0.25
5-4	DRPA	R/W	0	Right DAC primary AC dither gain – These bits control the AC dither gain for right channel primary DAC modulator. 00: AC dither gain = 0.125 01: AC dither gain = 0.25
3-2	DLPM	R/W	0	Left DAC primary DEM dither gain – These bits control the dither gain for left channel primary Galton DEM. 00: DEM dither gain = 0.5 01: DEM dither gain = 1.0 Others: Reserved (do not set)
1-0	DRPM	R/W	0	Right DAC primary DEM dither gain – These bits control the dither gain for right channel primary Galton DEM. 00: DEM dither gain = 0.5 01: DEM dither gain = 1.0 Others: Reserved (do not set)

8.6.1.42 Register 68 (0x44)

Figure 94. Register 68 (0x44)

7	6	5	4	3	2	1	0
Reserved						DLPD	
R/W						R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 73. Register 68 (0x44) Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved	R/W		Reserved
2-0	DLPD	R/W	0	Left DAC primary DC dither – These bits control the DC dither amount to be added to the lower part of the left channel primary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : 2^{-11} × 1/32 FS 00000000010 : 2^{-10} × 1/32 FS

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8.6.1.43 Register 69 (0x45)

Figure 95. Register 69 (0x45)

7	6	5	4	3	2	1	0
DLPD							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 74. Register 69 (0x45) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DLPD	R/W	0	Left DAC primary DC dither – These bits control the DC dither amount to be added to the lower part of the left channel primary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : 2^{-11} × 1/32 FS 00000000010 : 2^{-10} × 1/32 FS

8.6.1.44 Register 70 (0x46)

Figure 96. Register 70 (0x46)

7	6	5	4	3	2	1	0
DRPD							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 75. Register 70 (0x46) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DRPD	R/W	0	Right DAC primary DC dither – These bits control the DC dither amount to be added to the lower part of the right channel primary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : 2^{-11} × 1/32 FS 00000000010 : 2^{-10} × 1/32 FS

8.6.1.45 Register 71 (0x47)

Figure 97. Register 71 (0x47)

7	6	5	4	3	2	1	0
DRPD							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 76. Register 71 (0x47) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DRPD	R/W	0	Right DAC primary DC dither – These bits control the DC dither amount to be added to the lower part of the right channel primary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : 2^{-11} × 1/32 FS 00000000010 : 2^{-10} × 1/32 FS

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8.6.1.46 Register 72 (0x48)

Figure 98. Register 72 (0x48)

7	6	5	4	3	2	1	0
DLSA		DRSA		DLSM		RSM	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 77. Register 72 (0x48) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DLSA	R/W	01	Left DAC secondary AC dither gain – These bits control the AC dither gain for left channel secondary DAC. 00: AC dither gain = 0.125 01: AC dither gain = 0.25
5-4	DRSA	R/W	01	Right DAC secondary AC dither gain – These bits control the AC dither gain for right channel secondary DAC modulator. 00: AC dither gain = 0.125 01: AC dither gain = 0.25 10: AC dither gain = 0.5 11: no AC dither
3-2	DLSM	R/W	01	Left DAC secondary DEM dither gain – These bits control the dither gain for left channel secondary Galton DEM. 00: DEM dither gain = 0.5 01: DEM dither gain = 1.0 Others: Reserved (do not set)
1-0	DRSM	R/W	01	Right DAC secondary DEM dither gain – These bits control the dither gain for right channel secondary Galton DEM. 00: DEM dither gain = 0.5 01: DEM dither gain = 1.0 Others: Reserved (do not set)

ADVANCE INFORMATION

8.6.1.47 Register 73 (0x49)

Figure 99. Register 73 (0x49)

7	6	5	4	3	2	1	0
DLSD							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 78. Register 73 (0x49) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DLSD	R/W	0	Left DAC secondary DC dither – These bits control the DC dither amount to be added to the lower part of the left channel secondary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : 2^{-11} × 1/32 FS 00000000010 : 2^{-10} × 1/32 FS

8.6.1.48 Register 74 (0x4A)

Figure 100. Register 74 (0x4A)

7	6	5	4	3	2	1	0
DLSD							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 79. Register 74 (0x4A) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DLSD	R/W	0	Left DAC secondary DC dither – These bits control the DC dither amount to be added to the lower part of the left channel secondary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : 2^{-11} × 1/32 FS 00000000010 : 2^{-10} × 1/32 FS

ADVANCE INFORMATION

8.6.1.49 Register 75 (0x4B)

Figure 101. Register 75 (0x4B)

7	6	5	4	3	2	1	0
DRSD							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 80. Register 75 (0x4B) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DRSD	R/W	00000000	Right DAC secondary DC dither – These bits control the DC dither amount to be added to the lower part of the right channel secondary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : 2^{-11} × 1/32 FS 00000000010 : 2^{-10} × 1/32 FS

8.6.1.50 Register 76 (0x4C)

Figure 102. Register 76 (0x4C)

7	6	5	4	3	2	1	0
DRSD							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 81. Register 76 (0x4C) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DRSD	R/W	00000000	Right DAC secondary DC dither – These bits control the DC dither amount to be added to the lower part of the right channel secondary DAC modulator. The DC dither is expressed is Q0.11 format, with 1.0 equals to 1/32 fullscale modulator input. 00000000000 : No DC dither 00000000001 : 2^{-11} × 1/32 FS 00000000010 : 2^{-10} × 1/32 FS

ADVANCE INFORMATION

8.6.1.51 Register 78 (0x4E)

Figure 103. Register 78 (0x4E)

7	6	5	4	3	2	1	0
OLOF							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 82. Register 78 (0x4E) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OLOF	R/W	00000000	Left OFSCAL offset – These bits controls the amount of manual DC offset to be added to the left channel DAC output. The additional offset would be approximately the negative of the decimal value of this register divided by 4 in mV. 01111111 : –31.75 mV 01111110 : –31.50 mV … 00000010 : –0.50 mV 00000001 : –0.25 mV 00000000 : 0.0 mV 11111111 : +0.25 mV 11111110 : +0.50 mV … 10000000 : +32.0 mV

8.6.1.52 Register 79 (0x4F)

Figure 104. Register 79 (0x4F)

7	6	5	4	3	2	1	0
OROF							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 83. Register 79 (0x4F) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OROF	R/W	0	Right OFSCAL offset – These bits controls the amount of manual DC offset to be added to the right channel DAC output. The additional offset would be approximately the negative of the decimal value of this register divided by 4 in mV. 01111111 : –31.75 mV 01111110 : –31.50 mV … 00000010 : –0.50 mV 00000001 : –0.25 mV 00000000 : 0.0 mV 11111111 : +0.25 mV 11111110 : +0.50 mV … 10000000 : +32.0 mV

ADVANCE INFORMATION

8.6.1.53 Register 85 (0x55)

Figure 105. Register 85 (0x55)

7	6	5	4	3	2	1	0
Reserved			G2SL				
R/W			R/W				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 84. Register 85 (0x55) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4-0	G2SL	R/W	0	SDOUT Output Selection – These bits select the signal to output to SDOUT. To actually output the selected signal, the SDOUT must be set to output mode at P0-R8. 0000: off (low) 0001: DSP SDOUT output 0010: Register SDOUT output (P0-R86, bit 5) 0011: Auto mute flag (asserted when both L and R channels are auto muted) 0100: Auto mute flag for left channel 0101: Auto mute flag for right channel 0110: Clock invalid flag (clock error or clock changing or clock missing) 0111: Serial audio interface data output (SDOUT) 1000: Analog mute flag for left channel (low active) 1001: Analog mute flag for right channel (low active) 1010: PLL lock flag 1011: Charge pump clock 1100: Reserved 1101: Reserved 1110: Under voltage flag, asserted when XSMUTE voltage is higher than 0.7 DVDD 1111: Under voltage flag, asserted when XSMUTE voltage is higher than 0.3 DVDD ** INTERNAL ** 1100: Short detection flag for left channel 1101: Short detection flag for right channel 10000: PLL clock/4 10001: Oscillator clock/4 10010: Impedance sense flag for left channel 10011: Impedance sense flag for right channel 10100: Internal UVP flag, becomes low when VDD falls below roughly 2.7V 10101: Offset calibration flag, asserted when the system is offset calibrating itself. 10110: Clock error flag 10111: Clock changing flag 11000: Clock missing flag 11001: Clock halt detection flag 11010: DSP boot done flag 11011: Charge pump voltage output valid flag (low active) Others: N/A (zero)

ADVANCE INFORMATION

8.6.1.54 Register 86 (0x56)

Figure 106. Register 86 (0x56)

7	6	5	4	3	2	1	0
R/W		R/W	R/W		R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 85. Register 86 (0x56) Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0	Reserved
5	GOUT2	R/W	0	GPIO Output Control – This bit controls the SDOUT pin output when the selection at P0-R85 is set to 0010 (register output) 0: Output low 1: Output high
4	MUTE	R/W	0	This bit controls the MUTE output when the selection at P0-R84 is set to 0010 (register output). 0: Output low 1: Output high
3-0	Reserved	R/W	0	Reserved

8.6.1.55 Register 87 (0x57)

Figure 107. Register 87 (0x57)

7	6	5	4	3	2	1	0
R/W		R/W	R/W		R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 86. Register 87 (0x57) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0	Reserved
5	GINV2	R/W	0	GPIO Output Inversion – This bit controls the polarity of the SDOUT pin output. When set to 1, the output will be inverted for any signal being selected. 0: Non-inverted 1: Inverted
4	MUTE	R/W	0	This bit controls the polarity of MUTE output. When set to 1, the output will be inverted for any signal being selected. 0: Non-inverted 1: Inverted
3-0	Reserved	R/W	0	Reserved

8.6.1.56 Register 88 (0x58)

Figure 108. Register 88 (0x58)

7	6	5	4	3	2	1	0
DIEI							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 87. Register 88 (0x58) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIEI	RO	0x84	Die ID, Device ID = 0x84

ADVANCE INFORMATION

8.6.1.57 Register 91 (0x5B)

Figure 109. Register 91 (0x5B)

7	6	5	4	3	2	1	0
Reserved	DTFS			DTSR			
R/W	R			R			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 88. Register 91 (0x5B) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
6-4	DTFS	R	0	Detected FS – These bits indicate the currently detected audio sampling rate. 000: Error (Out of valid range) 001: 8 kHz 010: 16 kHz 011: 32-48 kHz 100: 88.2-96 kHz 101: 176.4-192 kHz 110: 384 kHz
3-0	DTSR	R	0	Detected MCLK Ratio – These bits indicate the currently detected MCLK ratio. Note that even if the MCLK ratio is not indicated as error, clock error might still be flagged due to incompatible combination with the sampling rate. Specifically the MCLK ratio must be high enough to allow enough DSP cycles for minimal audio processing when PLL is disabled. The absolute MCLK frequency must also be lower than 50 MHz. 0000: Ratio error (The MCLK ratio is not allowed) 0001: MCLK = 32 FS 0010: MCLK = 48 FS 0011: MCLK = 64 FS 0100: MCLK = 128 FS 0101: MCLK = 192 FS 0110: MCLK = 256 FS 0111: MCLK = 384 FS 1000: MCLK = 512 FS 1001: MCLK = 768 FS 1010: MCLK = 1024 FS 1011: MCLK = 1152 FS 1100: MCLK = 1536 FS 1101: MCLK = 2048 FS 1110: MCLK = 3072 FS

ADVANCE INFORMATION

8.6.1.58 Register 92 (0x5C)

Figure 110. Register 92 (0x5C)

7	6	5	4	3	2	1	0
Reserved							DTBR
R/W							R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 89. Register 92 (0x5C) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R/W	0	Reserved
0	DTBR	R	0	Detected SCLK Ratio (MSB)

8.6.1.59 Register 93 (0x5D)

Figure 111. Register 93 (0x5D)

7	6	5	4	3	2	1	0
DTBR							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 90. Register 93 (0x5D) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DTBR	R/W		Detected SCLK Ratio (LSB) – These bits indicate the currently detected SCLK ratio, i.e. the number of SCLK clocks in one audio frame. Note that for extreme case of SCLK = 1 FS (which is not usable anyway), the detected ratio will be unreliable

ADVANCE INFORMATION

8.6.1.60 Register 94 (0x5E)

Figure 112. Register 94 (0x5E)

7	6	5	4	3	2	1	0
Reserved	CDST6	CDST5	CDST4	CDST3	CDST2	CDST1	CDST0
R/W	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 91. Register 94 (0x5E) Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	0	Reserved
6	CDST6	R		Clock Detector Status – This bit indicates whether the MCLK clock is present or not. 0: MCLK is present 1: MCLK is missing (halted)
5	CDST5	R		This bit indicates whether the PLL is locked or not. The PLL will be reported as unlocked when it is disabled. 0: PLL is locked 1: PLL is unlocked
4	CDST4	R		This bit indicates whether the both LRCLK and SCLK are missing (tied low) or not. 0: LRCLK and/or SCLK is present 1: LRCLK and SCLK are missing
3	CDST3	R		This bit indicates whether the combination of current sampling rate and MCLK ratio is valid for clock auto set. 0: The combination of FS/MCLK ratio is valid 1: Error (clock auto set is not possible)
2	CDST2	R		This bit indicates whether the MCLK is valid or not. The MCLK ratio must be detectable to be valid. There is a limitation with this flag, that is, when the low period of LRCLK is less than or equal to five SCLKs, this flag will be asserted (MCLK invalid reported). 0: MCLK is valid 1: MCLK is invalid
1	CDST1	R		This bit indicates whether the SCLK is valid or not. The SCLK ratio must be stable and in the range of 32-256FS to be valid. 0: SCLK is valid 1: SCLK is invalid
0	CDST0	R		This bit indicated whether the audio sampling rate is valid or not. The sampling rate must be detectable to be valid. There is a limitation with this flag, that is when this flag is asserted and P0-R37 is set to ignore all asserted error flags such that the DAC recovers, this flag will be de-asserted (sampling rate invalid not reported anymore). 0: Sampling rate is valid 1: Sampling rate is invalid

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8.6.1.61 Register 95 (0x5F)

Figure 113. Register 95 (0x5F)

7	6	5	4	3	2	1	0
Reserved			LTSH	Reserved	CKMF	CSRF	CERF
R/W			R	R/W	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 92. Register 95 (0x5F) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	LTSH	R		Latched Clock Halt – This bit indicates whether MCLK halt has occurred. The bit is cleared when read. 0: MCLK halt has not occurred 1: MCLK halt has occurred since last read
3	Reserved	R/W	0	Reserved
2	CKMF	R		Clock Missing – This bit indicates whether the LRCLK and SCLK are missing (tied low). 0: LRCLK and/or SCLK is present 1: LRCLK and SCLK are missing
1	CSRF	R		Clock Resync Request – This bit indicates whether the clock resynchronization is in progress. 0: Not resynchronizing 1: Clock resynchronization is in progress
0	CERF	R		Clock Error – This bit indicates whether a clock error has occurred. The bit is cleared when read 0: Clock error has not occurred 1: Clock error has occurred.

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8.6.1.62 Register 108 (0x6C)

Figure 114. Register 108 (0x6C)

7	6	5	4	3	2	1	0
Reserved						AMLM	AMRM
R/W						R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 93. Register 108 (0x6C) Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R/W	0	Reserved
1	AMLM	R		Left Analog Mute Monitor – This bit is a monitor for left channel analog mute status. 0: Mute 1: Unmute
0	AMRM	R		Right Analog Mute Monitor – This bit is a monitor for right channel analog mute status. 0: Mute 1: Unmute

8.6.1.63 Register 119 (0x77)

Figure 115. Register 119 (0x77)

7	6	5	4	3	2	1	0
Reserved		GPIN2	MUTE	Reserved			
R/W		R	R	R			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 94. Register 119 (0x77) Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0	Reserved
5	GPIN2	R	0	GPIO Input States – This bit indicates the logic level at SDOUT pin. 0: Low 1: High
4	MUTE	R	0	This bit indicates the logic level at MUTE pin. 0: Low 1: High
3-0	Reserved	R	0	Reserved bits. Data on these bits may vary. 0: Low 1: High

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8.6.1.64 Register 120 (0x78)

Figure 116. Register 120 (0x78)

7	6	5	4	3	2	1	0
Reserved			AMFL	Reserved			AMFR
R/W			R	R/W			R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 95. Register 120 (0x78) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	AMFL	R		Auto Mute Flag for Left Channel – This bit indicates the auto mute status for left channel. 0: Not auto muted 1: Auto muted
3-1	Reserved	R/W	0	Reserved
0	AMFR	R		Auto Mute Flag for Right Channel – This bit indicates the auto mute status for right channel. 0: Not auto muted 1: Auto muted

8.6.2 Registers - Page 1

8.6.2.1 Register 1 (0x01)

Figure 117. Register 1 (0x01)

7	6	5	4	3	2	1	0
Reserved							OSEL
R/W							R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 96. Register 1 (0x01) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R/W	0	Reserved
0	OSEL	R/W	0	Output Amplitude Type - This bit selects the output amplitude type. The clock autoset feature will not work with PLL enabled in VCOM mode. In this case this feature has to be disabled via P0-R37 and the clock dividers must be set manually. 0: VREF mode (Constant output amplitude against AVDD variation) 1: VCOM mode (Output amplitude is proportional to AVDD variation)

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8.6.2.2 Register 2 (0x02)

Figure 118. Register 2 (0x02)

7	6	5	4	3	2	1	0
Reserved			LAGN	Reserved			RAGN
R/W			R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 97. Register 2 (0x02) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	LAGN	R/W	0	Analog Gain Control for Left Channel - This bit controls the left channel analog gain. 0: 0 dB 1: -6 dB
3-1	Reserved	R/W	0	Reserved
0	RAGN	R/W	0	Analog Gain Control for Right Channel - This bit controls the right channel analog gain. 0: 0 dB 1: -6 dB

8.6.2.3 Register 6 (0x06)

Figure 119. Register 6 (0x06)

7	6	5	4	3	2	1	0
Reserved							AMCT
R/W							R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 98. Register 6 (0x06) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R/W	0	Reserved
0	AMCT	R/W	1	Analog Mute Control -This bit enables or disables analog mute following digital mute. 0: Disabled 1: Enabled

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8.6.2.4 Register 7 (0x07)

Figure 120. Register 7 (0x07)

7	6	5	4	3	2	1	0
Reserved			AGBL	Reserved			AGBR
R/W			R/W	R/W			R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 99. Register 7 (0x07) Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0	Reserved
4	AGBL	R/W	0	Analog +10% Gain for Left Channel - This bit enables or disables amplitude boost mode for left channel. 0: Normal amplitude 1: +10% (+0.8 dB) boosted amplitude
3-1	Reserved	R/W	0	Reserved
0	AGBR	R/W	0	Analog +10% Gain for Right Channel - This bit enables or disables amplitude boost mode for right channel. 0: Normal amplitude 1: +10% (+0.8 dB) boosted amplitude

8.6.2.5 Register 9 (0x09)

Figure 121. Register 9 (0x09)

7	6	5	4	3	2	1	0
Reserved						DEME	VCPD
R/W						R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 100. Register 9 (0x09) Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R/W	0	Reserved
1	DEME	R/W	0	VCOM Pin as De-emphasis Control - This bit controls whether to use the DEEMP/VCOM pin as De-emphasis control. 0: Disabled (DEEMP/VCOM is not used to control De-emphasis) 1: Enabled (DEEMP/VCOM is used to control De-emphasis)
0	VCPD	R/W	1	Power down control for VCOM - This bit controls VCOM powerdown switch. 0: VCOM is powered on 1: VCOM is powered down

ADVANCE INFORMATION

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical Applications

The TAS3251 device supports both 2-channel, bridge-tied load (BTL) and mono, parallel bridge-tied load output configurations. This allows flexibility to configure and program the device for a number of different applications:

- 2.0, Stereo Systems - this is a standard stereo configuration. Use either one TAS3251 device in stereo, BTL or two TTAS3251 devices in PBTL.
- 0.1, Mono Speaker - the TAS3251 can be used as a 1-channel amplifier when configured in PBTL.
- Two-Way (1.1) Powered Speaker - the TAS3251 processing and amplifier support two-way or active crossover systems with a tweeter and woofer driven by independent amplifiers. This allows for the removal of passive crossover components in the speaker. This can either be accomplished using one TAS3251 device in BTL or two TAS3251 devices in PBTL.
- Three-Way Powered Speaker - the TAS3251 processing and amplifier support a three-way active speaker with a tweeter, mid-range and woofer each driven by independent amplifiers. This allows the removal of passive crossover components in the speaker. This can be accomplished by using two TAS3251 devices (2x BTL + 1x PBTL) or three TAS3251 devices each configured in PBTL.
- 2.1 Systems - the TAS3251 can be configured to support a 2.1 to support stereo, 2-channels (2x BTL) and a subwoofer (1x PBTL).

Typical Applications (continued)

9.1.1 Stereo, Bridge Tied Load (BTL) Application

Bridge-tied load (BTL) is a 2-channel amplifier configuration that can be used for stereo systems or two-way powered speakers. See design details below.

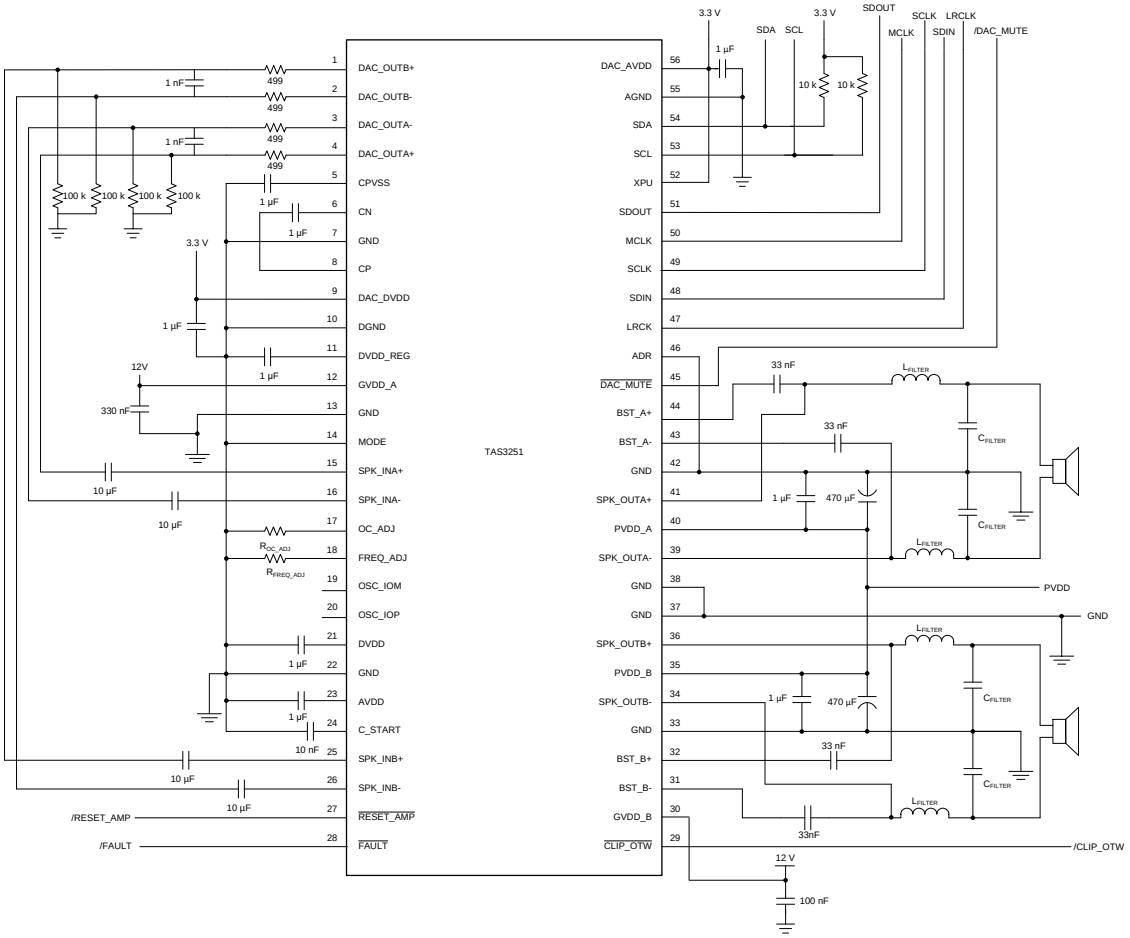


Figure 122. Bridge-Tied Load (BTL) Application Diagram

ADVANCE INFORMATION

Typical Applications (continued)

9.1.2 Mono, Parallel Bridge-Tied Load (PBTL) Application

Parallel bridge-tied load (PBTL) is a mono, one-channel amplifier configuration that provides twice the current of a single BTL channel. The TAS3251 supports both pre-filter PBTL and post-filter PBTL, which allows the Class-D output terminals to be paralleled before or after the LC filter. Paralleling the outputs after the LC filter requires four inductors and paralleling the outputs before the LC filter requires only two inductors.

9.1.2.1 Parallel Bridge-Tied Load (PBTL), Pre-Filter

The following diagram shows an application using pre-filter PBTL, which requires only two inductors. Note that the inductor should have a saturation current that is equal to the maximum current during an output short condition.

- SPK_OUTA+ and SPK_OUTB+ are connected before L_{FILTER} for the positive amplifier output.
- SPK_OUTA- and SPK_OUTB- are connected before L_{FILTER} for the negative amplifier output.

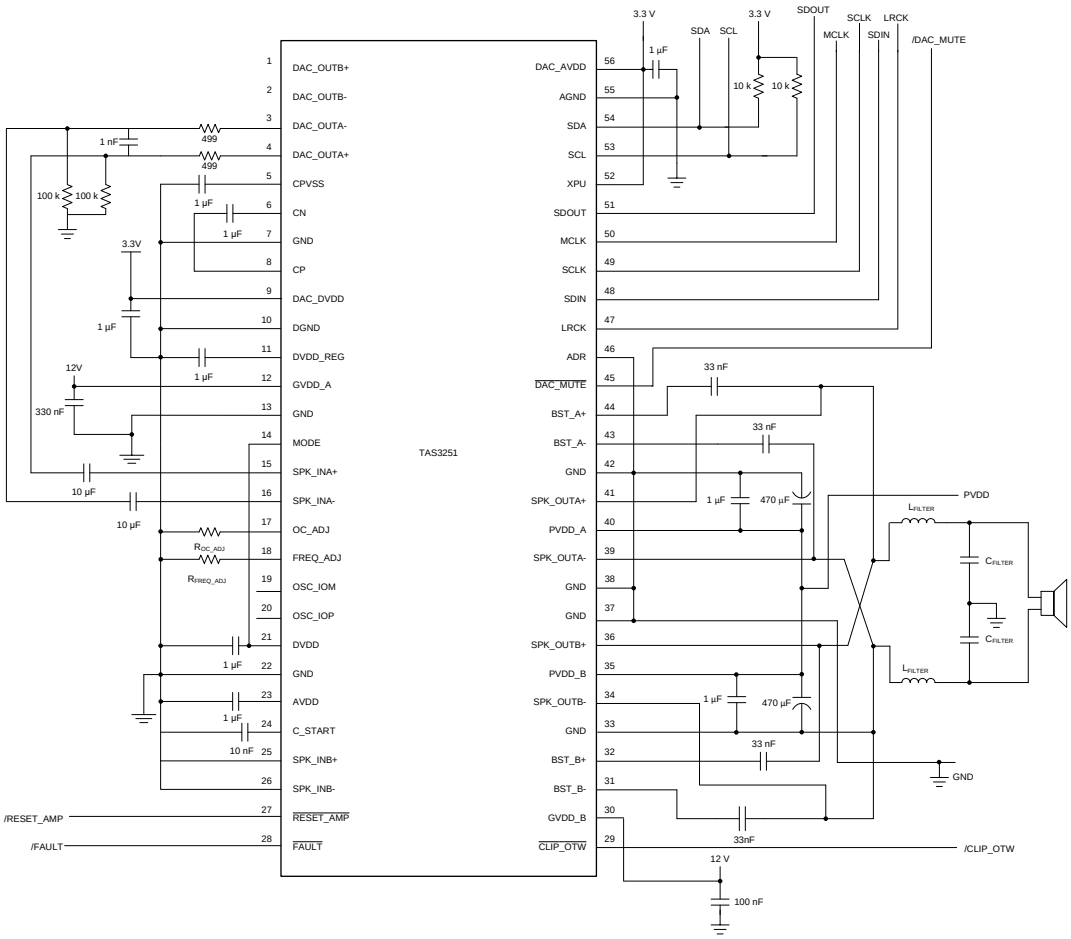


Figure 123. Pre-Filter Parallel Bridge-Tied Load (PBTL) Application Diagram

ADVANCE INFORMATION

Typical Applications (continued)

9.1.2.2 Parallel Bridge-Tied Load, Post-Filter

The following diagram shows an application using post-filter PBTL, which requires four inductors. The positive and negative output current are shared between two inductors.

- SPK_OUTA+, SPK_OUTA-, SPK_OUTB+ and SPK_OUTB- are each connected to L_{FILTER} first.
- The speaker side of the inductors are connected A+ and B+ and A- and B-. See diagram below.

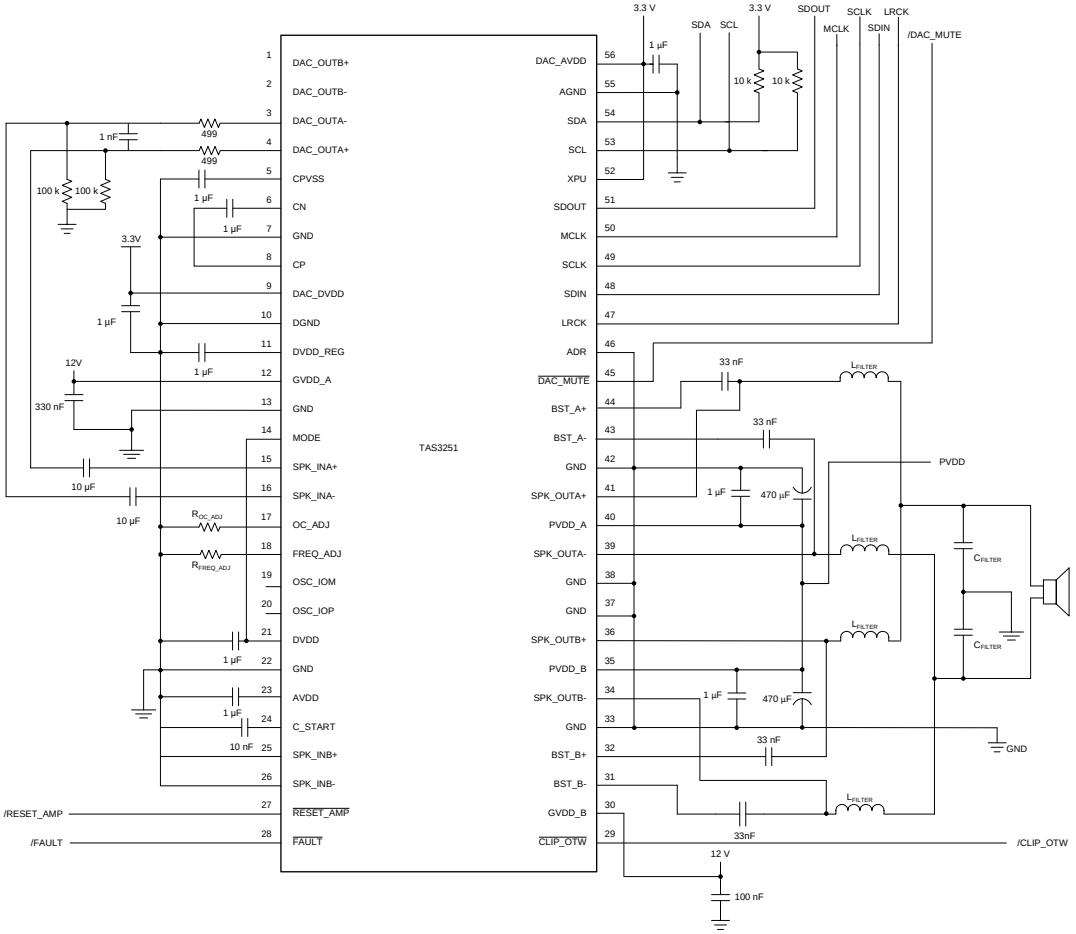


Figure 124. Post-Filter Parallel Bridge-Tied Load (PBTL) Application Diagram

9.1.3 Design Requirements

The following are required for operating and controlling the TAS3251.

- Power Supplies
  - Analog and Digital: 3.3-V supply
  - Gate Drive: 12-V supply
  - PVDD: 12-V to 36-V supply
- Communication: Host processor serving as I^2C compliant master
- Memory: The TAS3251 has a volatile register map that will reset when power is removed. The host processor should have adequate memory to initialize the device to the desired configuration.

9.1.4 Detailed Design Procedure

9.1.4.1 Step One: Schematic and Layout Design

Begin by designing the hardware for the TAS3251. Use the *Typical Application Schematic* and Pin Function Table as a guide for configuring the hardware pins. Follow the component placement and board layout from the TAS3251EVM. The most critical sections of the circuit are the power supply inputs, the amplifier output signals, and the high-frequency clock and data signals. Give precedence to these traces and connections when making design trade-offs.

1. First select the operating mode based on the application requirement: BTL, pre-filter PBTL (2-inductors) or post-filter PBTL (4-inductors).
2. Design the output stage including the LC filter based on the output configuration selected. Use the TAS3251EVM as reference. The LC Filter Design Guide and LC Filter Designer tool should be used to calculate the cutoff frequency and component values.
3. Select the switching frequency by configuring the resistor on pin 18, FREQ_ADJ.
4. Select the over-current threshold by configuring the resistor on pin 17, OC_ADJ.
5. Apply bypass and decoupling capacitors to power pins according to the Pin Function Table and the *Typical Application Schematic*.

9.1.4.1.1 Decoupling Capacitor Recommendations

To design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, good quality decoupling capacitors should be used. Ceramic type X7R should be used in this application.

Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the 1 μF that is placed on the PVDD power supply pins to each full-bridge. It must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output and the ripple current created by high power output. A minimum voltage rating of 50 V is required for use with a 36 V power supply.

9.1.4.1.2 PVDD Capacitor Recommendations

The large capacitors used in conjunction with each full-bridge, are referred to as the PVDD Capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well designed system power supply, 470 μF, 50 V supports most applications. The PVDD capacitors should be low ESR type because they are used in a circuit associated with high-speed switching.

9.1.4.1.3 BST Capacitors

To ensure large enough bootstrap energy storage for the high side gate drive to work correctly with all audio source signals, 33 nF / 25V X7R BST capacitors are recommended.

9.1.4.1.4 Heatsink

The heat sink should be attached to the device using a thermally conductive paste and have a good connection to board ground.

ADVANCE INFORMATION

9.1.4.2 Step Two: Configure the Fixed-Function Process Flow for Use with the Target System

Use the TAS3251EVM and PurePath™ Console 3 to characterize, tune and test the speaker system.

1. Use the TAS3251 Evaluation Module (TAS3251EVM) and PurePath™ Console 3 software to configure the device settings and audio processing. PurePath Console 3 can be requested and downloaded from TI.com.
2. Once the appropriate configuration has been finalized using the TAS3251EVM, use the In-System Programming mode in PurePath™ Console 3 to load the configuration to a TAS3251 in the final system (not on the TAS3251EVM). Connect the I2C traces from the TAS3251EVM to the final system for programming. Ensure the I2C lines have compatible voltages and resistor pull-ups.

9.1.4.3 Step Three: Software Integration

1. Use the export feature in PurePath™ Console 3 software to generate a register map configuration file to be used to initialize the TAS3251at system startup.
2. Include the configuration file in the main processor program to load during the TAS3251 initialization.
3. Integrate dynamic control commands (such as volume controls, mute commands, and mode-based EQ curves) into the main system program.

9.1.5 Two TAS3251 Device Configurations

This section describes hardware design requirements for systems using two TAS3251devices.

9.1.5.1 2 x PBTL Application

In this configuration both devices are configured in parallel bridge-tied load (PBTL) mode. Example use cases for a 2 x PBTL hardware configuration include:

- **Stereo Speaker Pair**, with left and right channel audio. This can be implemented in one of two ways:
  - Send left channel I^2S or TDM data to one device and send right channel I^2S or TDM data to the other device.
  - Or, send both left and right channel to one device and send the post-processed data through the SDOUT pin to the other device.
- **2-Way, Active Crossover Speaker**, with one amplifier driving a tweeter and the other driving a woofer.
  - Send the same audio channel to both devices and use the DSP in one device for the high-pass filter and the other device for the low-pass filter to form a 2-way, crossover.
  - Or, send the audio to one primary device, do the high-pass and low-pass processing in the primary device, and then send either the high-pass or low-pass data only to the other device using the SDOUT pin.

9.1.5.2 2 x BTL + 1 x PBTL Application

In this configuration one device is configured in two bridge-tied load (BTL) mode and the other device is configured in mono, parallel bridge-tied load (PBTL) mode. Example use cases for a 2 x BTL and 1 x PBTL hardware configuration include:

- **2.1 Speaker System**, with left, right and subwoofer audio channels. In this setup, process left, right and subwoofer audio in one device and then send the subwoofer data from SDOUT to another device.
- **3-Way, Active Crossover Speaker**, with one amplifier driving a tweeter and a mid-range speaker (BTL), and another (PBTL) driving a woofer or subwoofer. In this configuration, process everything in one device and send the subwoofer data from SDOUT to another device.

9.1.6 Three or More TAS3251 Device Configurations

This section describes hardware design requirements and considerations for systems using three or more TAS3251devices.

With three or more devices in a system, the processing power of a signle TAS3251 may be insufficient. To create a complex system, map out the audio path using multiple DSPs and use a combination of daisy-chained DSPs or paralleled DSPs to process the audio and create the speaker signal path.

ADVANCE INFORMATION

9.1.7 Application Curves

Table 101. Application Curves

Configuration	Performance Graph
BTL	Figure 5 Total Harmonic Distortion+Noise vs Output Power
BTL	Figure 6 Total Harmonic Distortion+Noise vs Frequency
PBTL	Figure 13 Total Harmonic Distortion+Noise vs Output Power
PBTL	Figure 14 Total Harmonic Distortion+Noise vs Frequency

10 Power Supply Recommendations

10.1 Power Supplies

The device requires three power supplies for proper operation. A 3.3 V rail for the low voltage circuitry and DAC, a 12 V rail for the amplifier gate-drive, and PVDD which is required to provide power to the output stage of the audio amplifier. The operating range for these supplies is shown in the Recommended Operating Conditions. TI recommends waiting 100 ms to 240 ms for the DVDD power supplies to stabilize before starting I^2C communication and providing stable I^2S clock before enabling the device outputs.

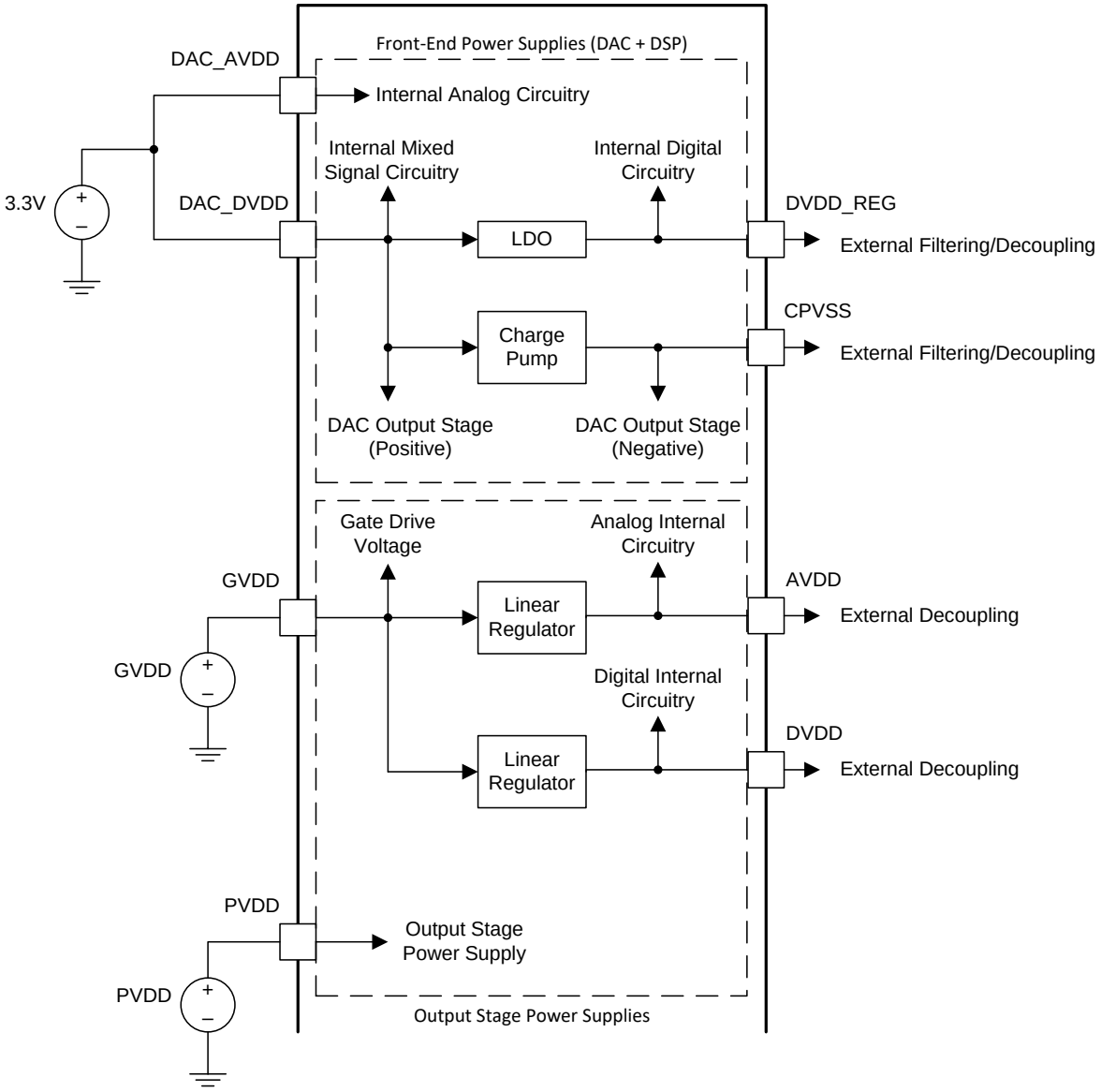


Figure 125. Power Supply Functional Block Diagram

Power Supplies (continued)

10.1.1 DAC_DVDD and DAC_AVDD Supplies

The DAC_DVDD supply is required from the system to power several portions of the device. As shown in *Figure 125*, it provides power to the DVDD_REG pin and the CPVDD pin. Proper connection, routing, and decoupling techniques are highlighted in the *EVM User's Guide* (as well as the *Application and Implementation* section and the *Layout Examples* section) and must be followed as closely as possible for proper operation and performance. Deviation from the guidance offered in the TAS3251*EVM User's Guide*, which follows the same techniques as those shown in the *Application and Implementation* section, can result in reduced performance, errant functionality, or even damage to the TAS3251 device.

Some portions of the device also require a separate power supply that is a lower voltage than the external DAC_DVDD supply. To simplify the power supply requirements for the system, the TAS3251 device includes an integrated low-dropout (LDO) linear regulator to create this supply. This linear regulator is internally connected to the DAC_DVDD supply and its output is presented on the DVDD_REG pin, providing a connection point for an external bypass capacitor. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

The outputs of the high-performance DACs used in the TAS3251 device are ground centered, requiring both a positive low-voltage supply and a negative low-voltage supply. The positive power supply for the DAC output stage is taken from the DAC_AVDD pin, which can be connected to the DAC_DVDD supply provided by the system. A charge pump is integrated in the TAS3251 device to generate the negative low-voltage supply. The power supply input for the charge pump is the CPVDD pin. The CPVSS pin is provided to allow the connection of a filter capacitor on the negative low-voltage supply. As is the case with the other supplies, the component selection, placement, and routing of the external components for these low voltage supplies are shown in the TAS3251 EVM User's Guide and should be followed as closely as possible to ensure proper operation of the device.

10.1.1.1 CPVSS, CN and CP Charge Pump

The TAS3251 has an integrated charge pump for generating the negative supply voltage for the DAC output stage. Connect a 1µF ceramic capacitor between CN and CP and connect a 1 µF ceramic capacitor from CPVSS to GND.

10.1.2 VDD Supply

The VDD supply required from the system is used to power several portions of the device. It provides power to internal regulators DVDD and AVDD that are used to power digital and analog sections of the device output power stage. Connect a 1 µF ceramic capacitor to GND and ensure capacitor voltage rating is sufficient for AVDD and DVDD. See DVDD and AVDD typical voltages in Amplifier Electrical Characteristics. Proper connection, routing, and decoupling techniques are highlighted in the Layout Section and the TAS3251EVM User's Guide, which must be followed as closely as possible for proper operation and performance. Deviation from the guidance offered in the section may result in reduced performance, errant functionality, or even damage to the TAS3251 device.

Some portions of the device also require a separate power supply which is a lower voltage than the VDD supply. To simplify the power supply requirements for the system, the TAS3251 device includes integrated low-dropout (LDO) linear regulators to create these supplies. These linear regulators are internally connected to the VDD supply and their outputs are presented on AVDD and DVDD pins, providing a connection point for an external bypass capacitors. It is important to note that the linear regulators integrated in the device have only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on these pins could cause the voltage to sag and increase noise injection, which negatively affects the performance and operation of the device.

Power Supplies (continued)

10.1.3 GVDD_X Supply

The GVDD_X supply required from the system is used to power the gate-drives for the output H-bridges. Connect 0.1 µF ceramic capacitor from pin to GND and place as close to pin as possible. The ceramic capacitor should have a voltage rating of at least 25V. Proper connection, routing, and decoupling techniques are highlighted in the Layout Section and the TAS3251EVM User's Guide and must be followed as closely as possible for proper operation and performance. Deviation from the guidance offered in the these sections may result in reduced performance, errant functionality, or even damage to the TAS3251 device.

10.1.4 PVDD Supply

The output stage of the amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the section and section and must be followed as closely as possible for proper operation and performance. Due to the high-voltage switching of the output stage, it is particularly important to properly decouple the output power stages. The lack of proper decoupling can results in voltage spikes which can damage the device, or cause poor audio performance and device shutdown faults. See the TAS3251EVM for proper component selection, placement and layout for best performance.

10.1.5 BST Supply

TAS3251 has built-in bootstrap supply for each half bridge gate drive to supply the high side MOSFETs, only requiring a single capacitor per half bridge. The capacitors are connected to each half bridge output and charged by the GVDD supply via an internal diode while the PWM outputs are in low state. The high side gate drive is supplied by the voltage across the BST capacitor while the output PWM is high. It is recommended to place the BST capacitors close to the TAS3251 device and keep the length of PCB traces to a minimum. Connect a 0.033 µF ceramic capacitor with a rating of at least 25V between BST_xx pin and the corresponding output stage SPK_OUTxx pin.

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

11.1.1 General Guidelines for TAS3251

Audio amplifiers which incorporate switching output stages require special attention to the device layout and supporting component layout. The system level performance, including electromagnetic compliance (EMC), device reliability and audio performance are all affected by the layout. See the section Layout Examples for layout recommendations based on amplifier output configuration. The list below provides general guidelinese to follow when placing components and routing.

- Use an unbroken ground plan for low impedance and low inductance return path to the power supply for power and audio signals.
- Keep the routing between the DAC and the amplifier inputs as short as possible. Maintain good grounding around these traces to prevent noise.
- The small bypass capacitors on the PVDD lines should be placed as close to the PVDD pins as possible.
- Reference all bypass and decoupling components to the TAS3251 ground by connecting the ground of the component directly to the ground of the device.
- Maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many ground pins as possible. This will help conduct heat through the pins of the package.

11.1.2 Importance of PVDD Bypass Capacitor Placement

Placing the bypass and decoupling capacitors close to supply pins is required for stability and best performance. This applies to DVDD, AVDD, CPVDD, and PVDD.

The small bypass capacitors on the PVDD lines of the TAS3251 must be placed as close to the PVDD pins as possible. Not only does placing these devices far away from the pins increase the electromagnetic interference in the system, but doing so can also negatively affect the reliability of the device. Placement of these components too far from the TAS3251 device can cause ringing on the output pins that can cause the voltage on the output pin to exceed the maximum allowable ratings shown in the *Absolute Maximum Ratings* table, damaging the device. For that reason, the capacitors on the PVDD net must be no further away from their associated PVDD pins than what is shown in the example layouts in the *Layout Examples* section

11.2 Layout Examples

11.2.1 Bridge-Tied Load (BTL) Layout Example

This section shows an example layout when operating in bridge-tied load (BTL) mode.

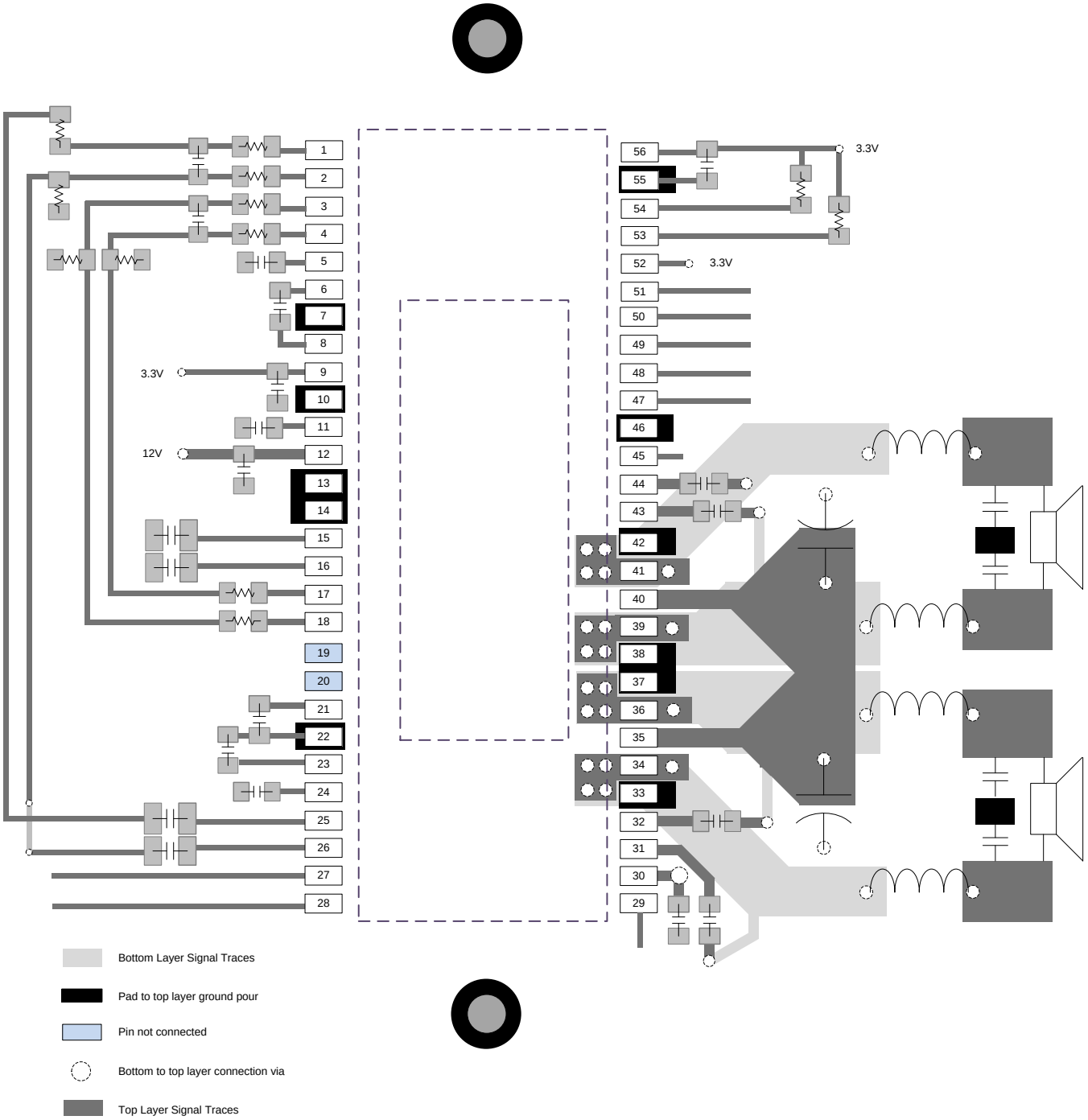


Figure 126. BTL Layout Example

Layout Examples (continued)

11.2.2 Parallel Bridge-Tied Load (PBTL), Pre-Filter

This section shows an example layout when operating in parallel bridge-tied load (PBTL) mode and connecting the output traces **before** the LC filter using two inductors. This layout requires fewer inductors compared with post-filter PBTL.

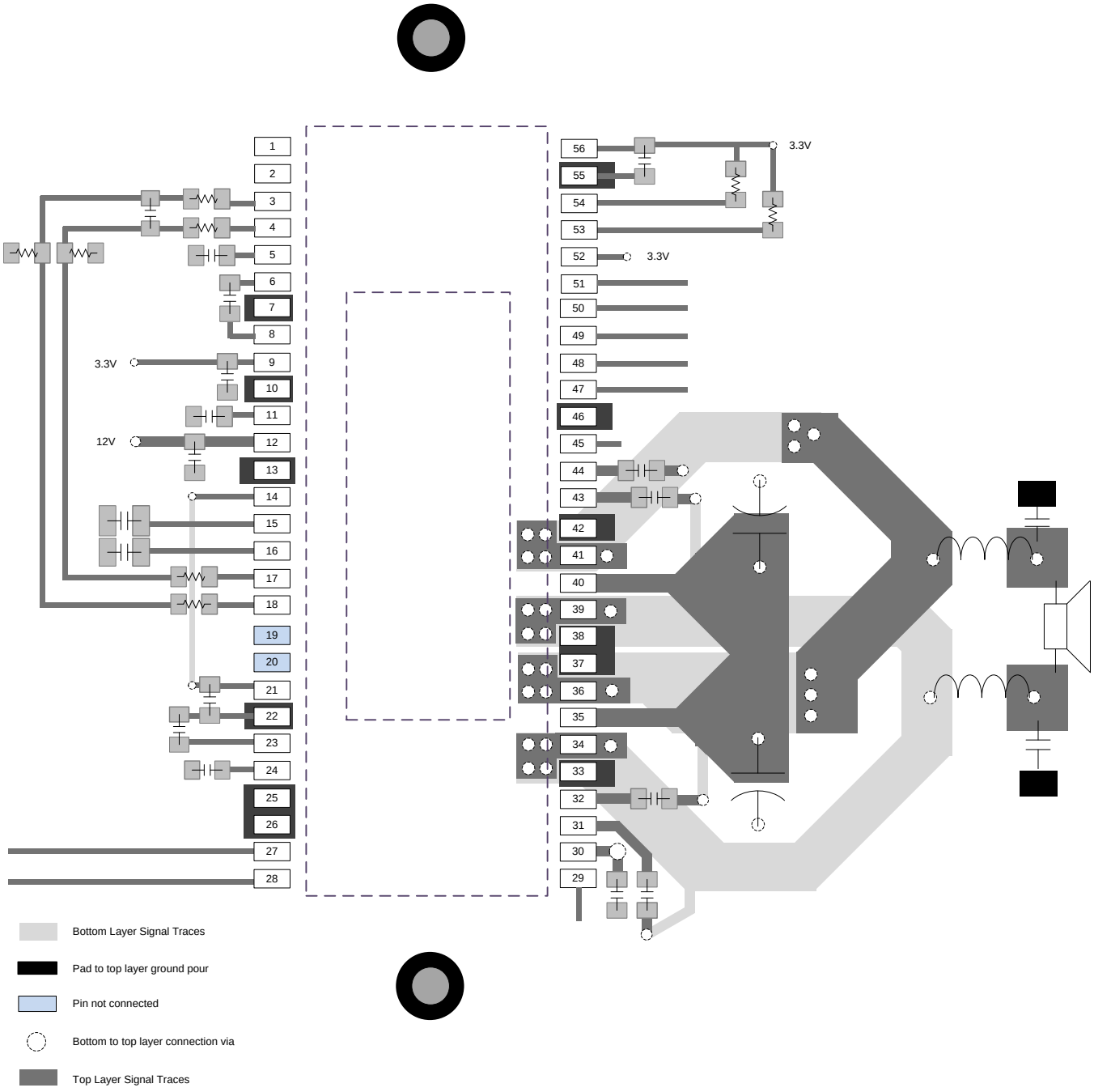


Figure 127. Pre-Filter PBTL Layout Example

ADVANCE INFORMATION

Layout Examples (continued)

11.2.3 Parallel Bridge-Tied Load (PBTL), Post-Filter

This section shows an example layout when operating in parallel bridge-tied load (PBTL) mode and connecting the output traces **after** the LC filter using four inductors. This layout requires fewer inductors compared with post-filter PBTL.

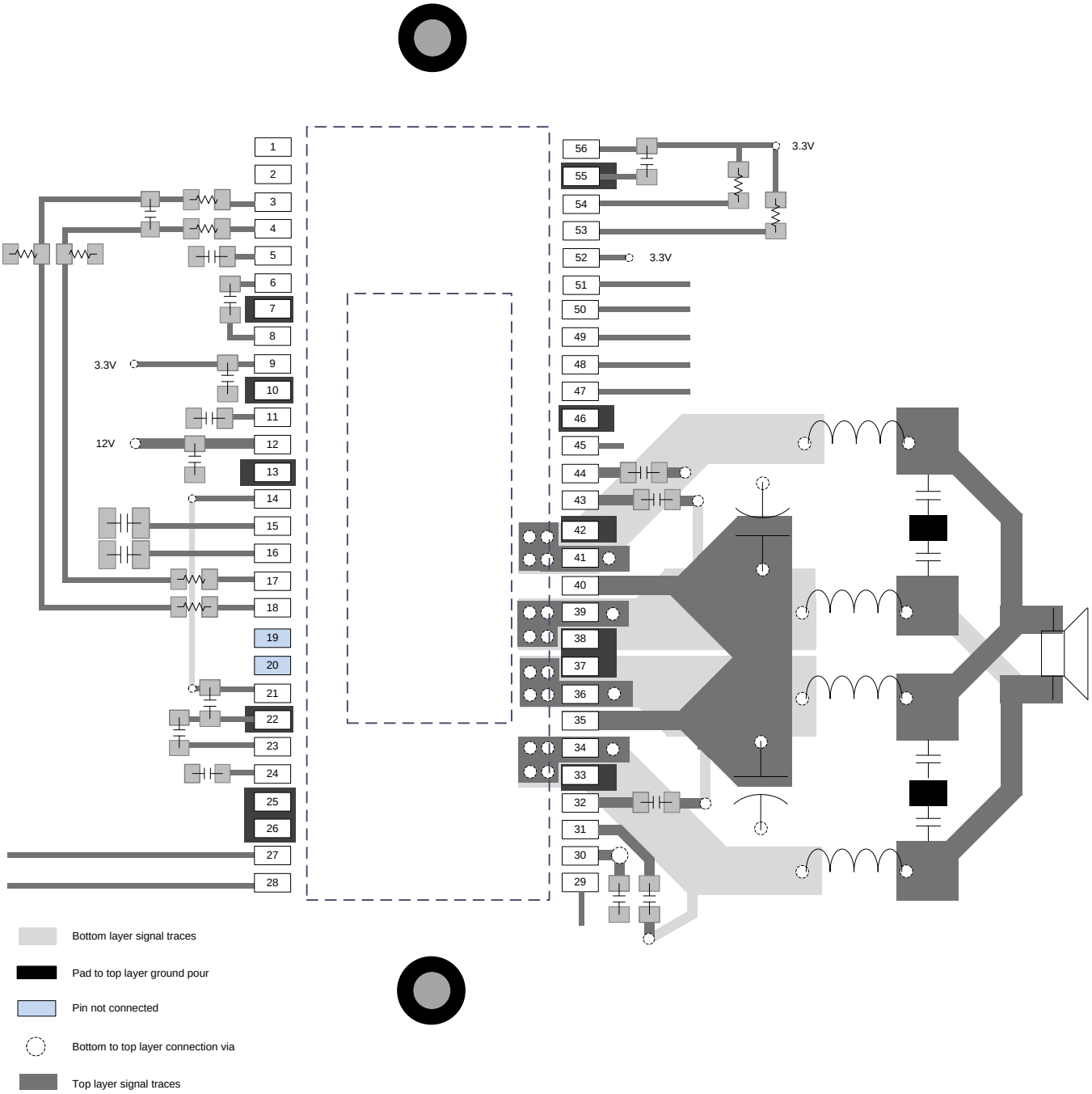


Figure 128. Post-Filter PBTL Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

The glossary listed in the *Glossary* section is a general glossary with commonly used acronyms and words which are defined in accordance with a broad TI initiative to comply with industry standards such as JEDEC, IPC, IEEE, and others. The glossary provided in this section defines words, phrases, and acronyms that are unique to this product and documentation, collateral, or support tools and software used with this product. For any additional questions regarding definitions and terminology, please see the e2e Audio Amplfier Forum.

Bridge tied load (BTL) is an output configuration in which one terminal of the speaker is connected to one half-bridge and the other terminal is connected to another half-bridge.

DUT refers to a *device under test* to differentiate one device from another.

Closed-loop architecture describes a topology in which the amplifier monitors the output terminals, comparing the output signal to the input signal and attempts to correct for non-linearities in the output.

Dynamic controls are those which are changed during normal use by either the system or the end-user.

GPIO is a general purpose input/output pin. It is a highly configurable, bi-directional digital pin which can perform many functions as required by the system.

Host processor (also known as System Processor, Scalar, Host, or System Controller) refers to device which serves as a central system controller, providing control information to devices connected to it as well as gathering audio source data from devices upstream from it and distributing it to other devices. This device often configures the controls of the audio processing devices (like the TAS3251) in the audio path in order to optimize the audio output of a loudspeaker based on frequency response, time alignment, target sound pressure level, safe operating area of the system, and user preference.

HybridFlow uses components which are built in RAM and components which are built in ROM to make a configurable device that is easier to use than a fully-programmable device while remaining flexible enough to be used in several applications

Maximum continuous output power refers to the maximum output power that the amplifier can continuously deliver without shutting down when operated in a 25°C ambient temperature. Testing is performed for the period of time required that their temperatures reach thermal equilibrium and are no longer increasing

Parallel bridge tied load (PBTL) is an output configuration in which one terminal of the speaker is connected to two half-bridges which have been placed in parallel and the other terminal is connected to another pair of half bridges placed in parallel

$r_{DS(on)}$ is a measure of the on-resistance of the MOSFETs used in the output stage of the amplifier.

Static controls/Static configurations are controls which do not change while the system is in normal use.

Vias are copper-plated through-hole in a PCB.

12.1.2 Development Support

- TAS3251 Evaluation Module (TAS3251EVM)
- PurePath™ Console 3 Software (PUREPATHCONSOLE)
- Speaker Characterization Board for PurePath™ Audio SmartAmp (PP-SALB-EVM)

ADVANCE INFORMATION

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

Burr-Brown, PurePath, PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTAS3251DKQ	ACTIVE	HSSOP	DKQ	56	20	TBD	Call TI	Call TI	0 to 70		Samples
TAS3251DKQ	ACTIVE	HSSOP	DKQ	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	3251	Samples
TAS3251DKQR	ACTIVE	HSSOP	DKQ	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	3251	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

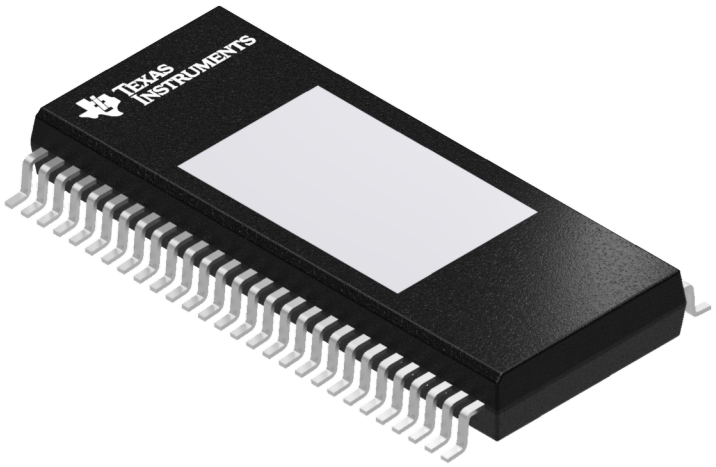
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DKQ 56 PowerPAD™ SSOP - 2.34 mm max height

PLASTIC SMALL OUTLINE



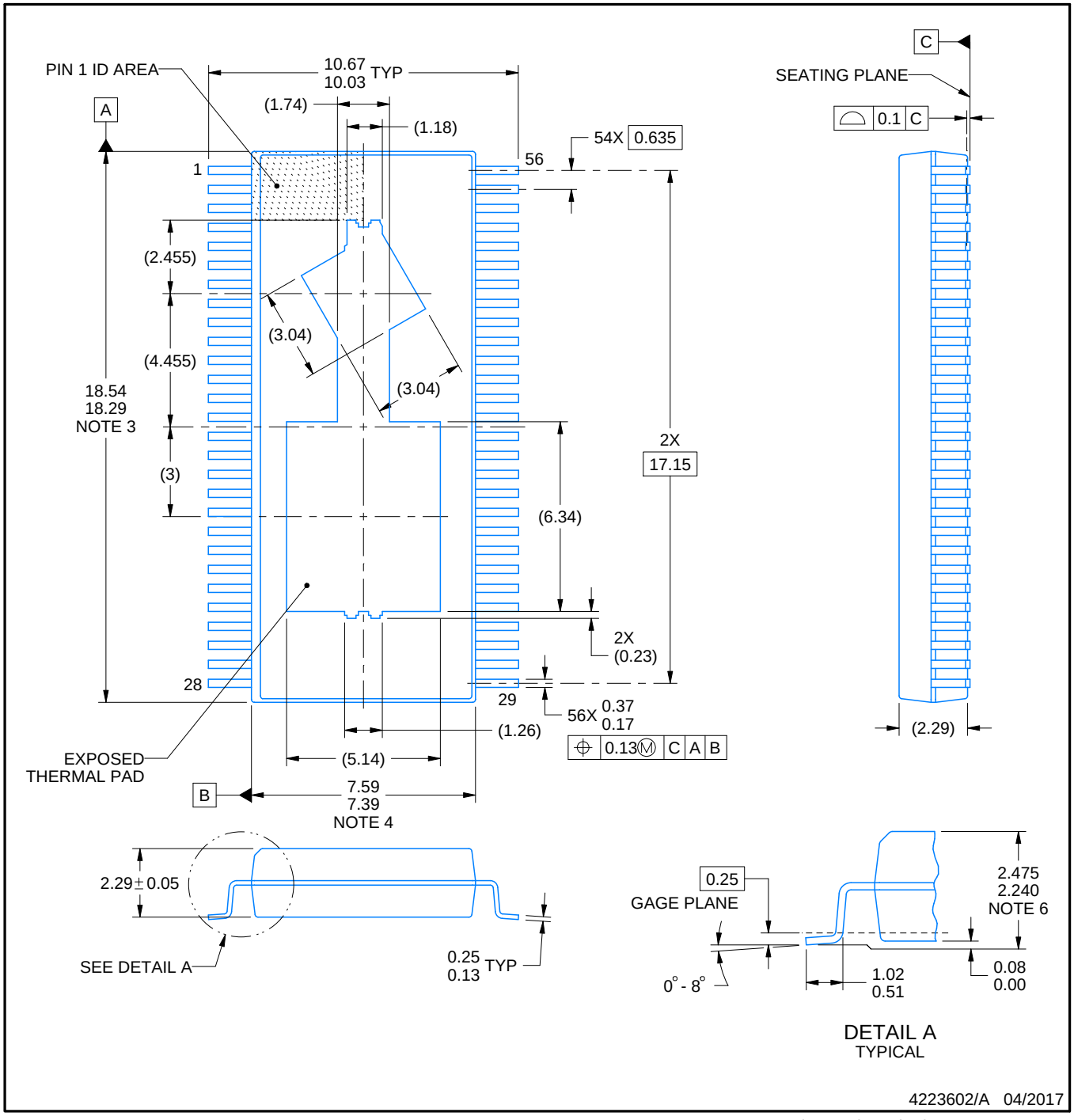
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DKQ0056B

PowerPAD™ SSOP - 2.475 mm max height

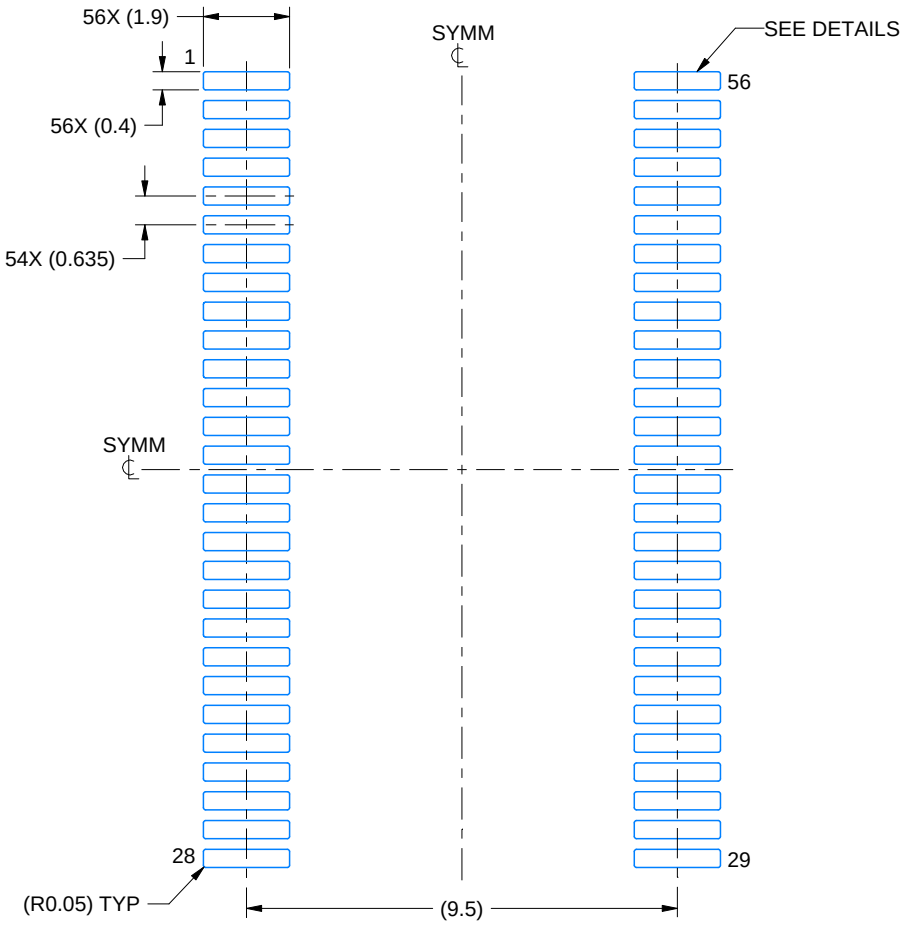
PLASTIC SMALL OUTLINE



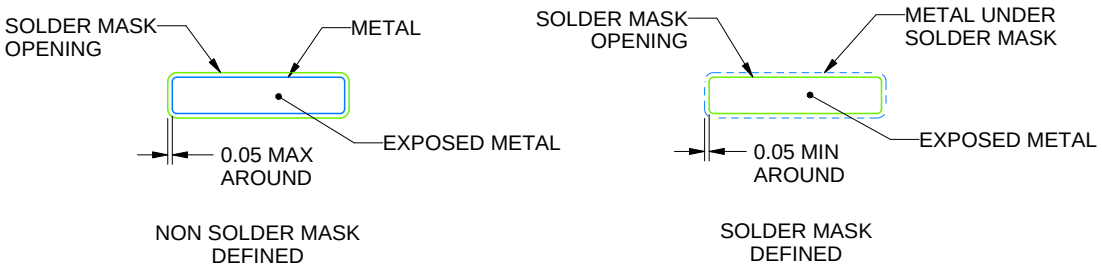
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. The exposed thermal pad is designed to be attached to an external heatsink.
6. For clamped heatsink design, refer to overall package height above the seating plane as 2.325 +/- 0.075 and molded body thickness dimension.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

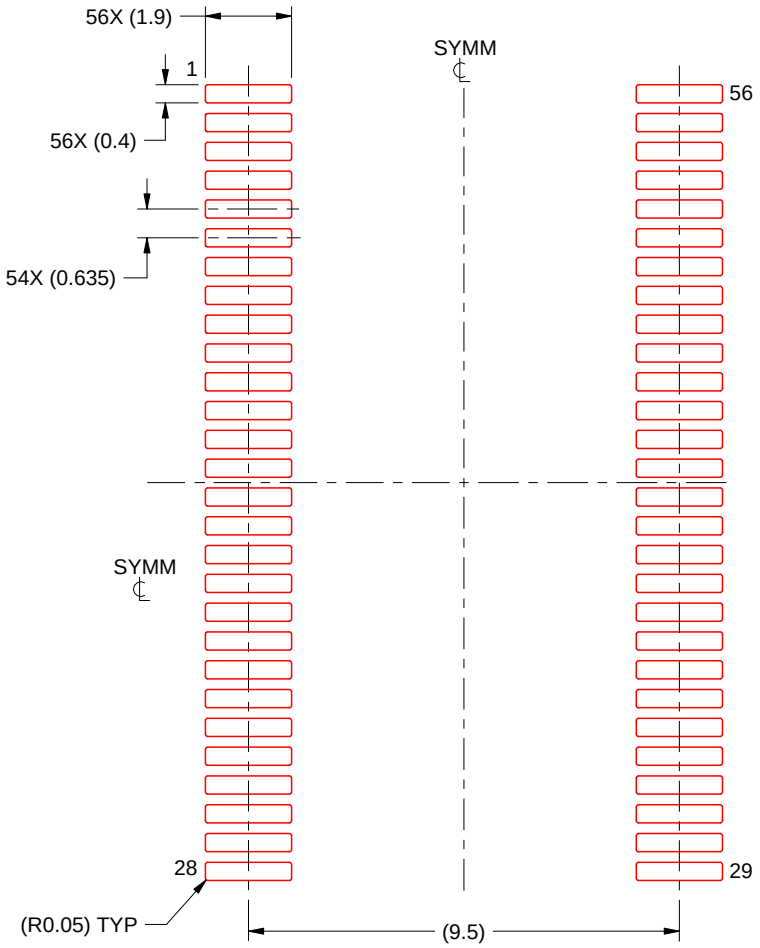


SOLDER MASK DETAILS
NOT TO SCALE

4223602/A 04/2017

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE:6X

4223602/A 04/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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