4.7V to 60V Input, 50mA Synchronous Step-Down Converter with Low IQ

Check for Samples: TPS54062

FEATURES

- **Integrated High Side and Low Side MOSFET**
- **Peak Current Mode Control**
- **Diode Emulation for Improved Light Load Efficiency**
- **89 µA (typical) Operating Quiescent Current**
- **100 kHz to 400 kHz Adjustable Switching Frequency**
- **Synchronizes to External Clock**
- **Internal Slow Start**
- **0.8 V ±2% Voltage Reference**
- **Stable with Ceramic Output Capacitors or Low Cost Aluminum Electrolytic**
- **Cycle-by-Cycle Current Limit, Thermal and Frequency Fold Back Protection**
- **MSOP-8 and 3mm x 3mm VSON-8 Packages**

APPLICATIONS

- **Low Power Standby or Bias Voltage Supplies**
- **4-20 mA Current-Loop Powered Sensors**
- **Industrial Process Control, Metering, and Security Systems**
- **High Voltage Linear Regulator Replacement**

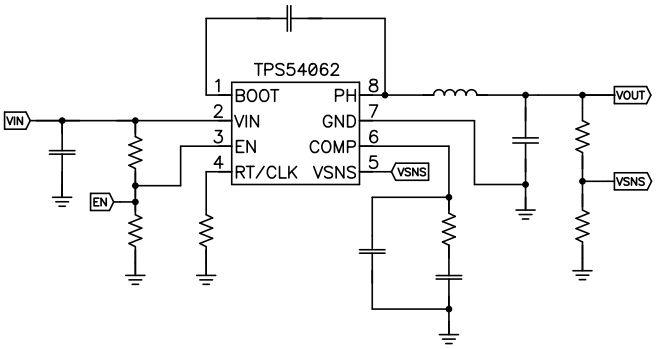
DESCRIPTION

The TPS54062 device is a 60 V, 50-mA, synchronous step-down converter with integrated high side and low side MOSFETs. Current mode control provides simple external compensation and flexible component selection. The non-switching supply current is 89 µA. Using the enable pin, shutdown supply current is reduced to 1.7 µA.

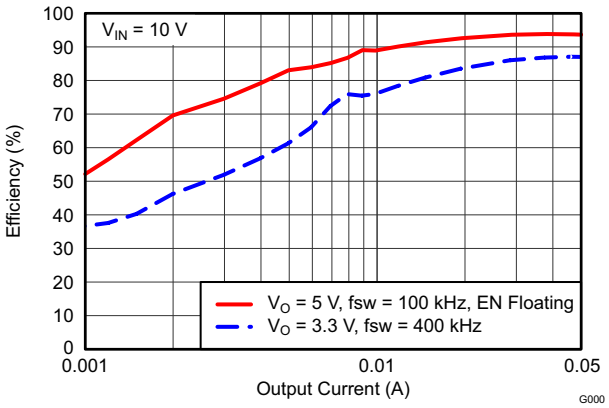
Under voltage lockout is internally set at 4.5 V, but can be increased using the accurate enable pin threshold. The output voltage startup ramp is controlled by the internal slow start time.

Adjustable switching frequency range allows efficiency and external component size to be optimized. Frequency fold back and thermal shutdown protects the part during an overload condition.

SIMPLIFIED SCHEMATIC



EFFICIENCY



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SwitcherPro is a trademark of Texas Instruments.

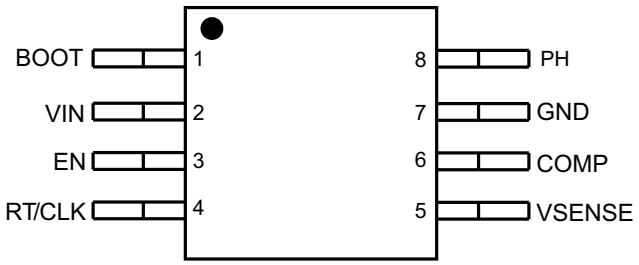
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Table 1. ORDERING INFORMATION(1)

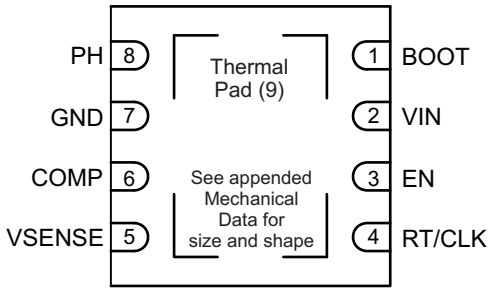
T_J	PACKAGE	PART NUMBER(2)
–40°C to 125°C	MSOP-8 DGK	TPS54062DGK
	VSON-8 DRB	TPS54062DRB

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The DGK and DRB packages are also available taped and reeled. Add an R suffix to the device type (i.e., TPS54062DGKR).

PIN CONFIGURATION MSOP-8 PACKAGE (TOP VIEW)



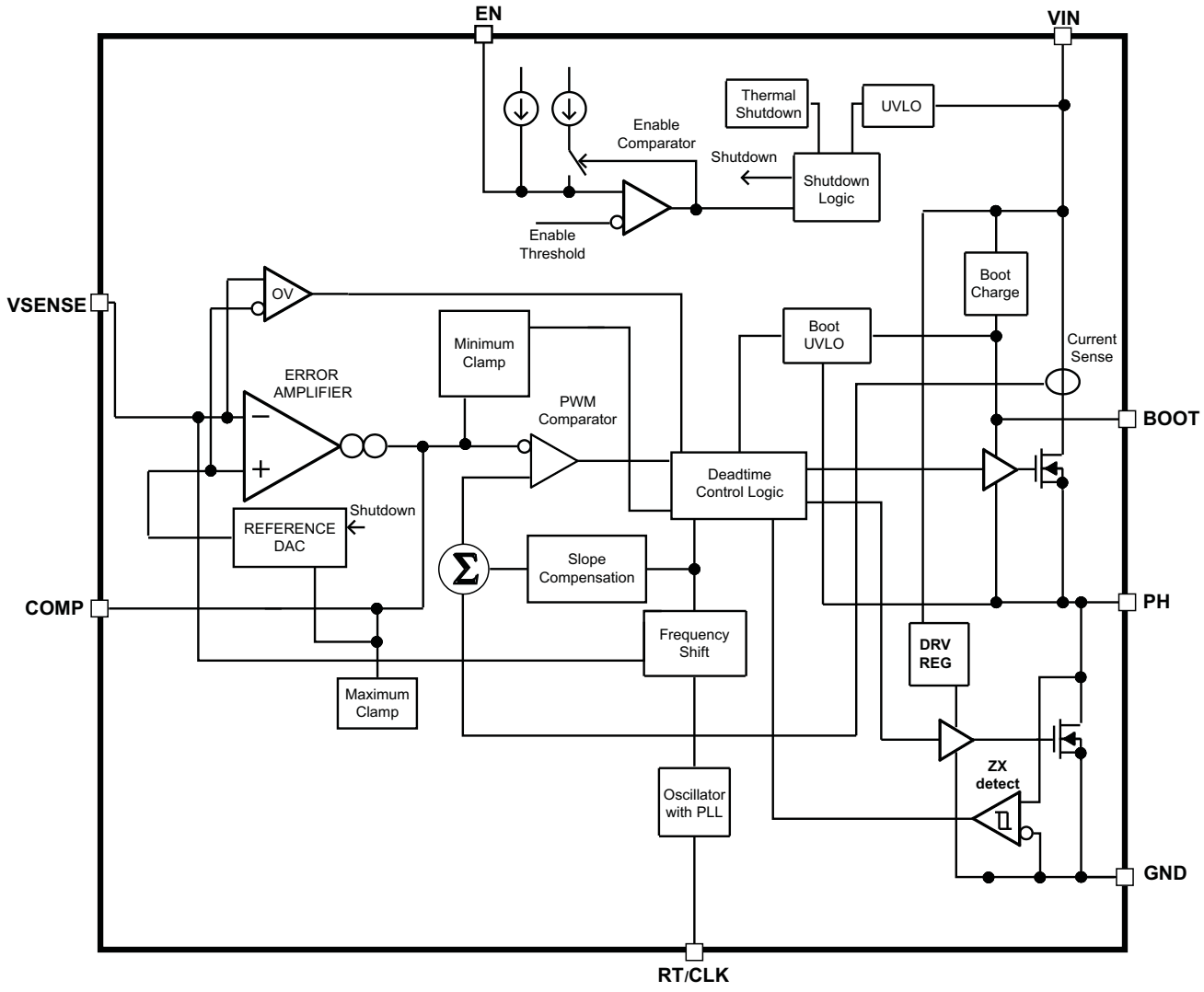
PIN CONFIGURATION VSON-8 PACKAGE (BOTTOM VIEW)



PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NUMBER	
BOOT	1	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the output device, the output is forced to switch off until the capacitor is refreshed.
VIN	2	Input supply voltage, 4.7 V to 60 V.
EN	3	Enable pin, internal pull-up current source. Pull below 1.14 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors, see the Enable and Adjusting Undervoltage Lockout section.
RT/CLK	4	Resistor Timing and External Clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the mode returns to a resistor frequency programming.
VSENSE	5	Inverting input of the transconductance (gm) error amplifier.
COMP	6	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
GND	7	Ground
PH	8	The source of the internal high-side power MOSFET and drain of the internal low side MOSFET
Thermal Pad	9	GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation. VSON-8 package only.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Voltage	VIN	–0.3	62	V
	EN	–0.3	8	V
	PH-BOOT		8	V
	BOOT		70	V
	VSENSE	–0.3	6	V
	COMP	–0.3	3	V
	PH	–0.6	62	V
	PH, 10ns Transient	–2	62	V
	RT/CLK	–0.3	6	V
Current	VIN	Internally Limited		A
	EN		100	µA
	BOOT		100	mA
	VSENSE		10	µA
	COMP		100	µA
	PH	Internally Limited		A
	RT/CLK		200	µA
Electrostatic discharge	(HBM) QSS 009-105 (JESD22-A114A)		2	kV
	(CDM) QSS 009-147 (JESD22-C101B.01)		500	V
Operating junction temperature		–40	125	ºC
Storage temperature		–65	150	ºC

(1) The Absolute Maximum Ratings specified in this section will apply to all specifications of this document unless otherwise noted. These specifications will be interpreted as the conditions which may damage the device with a single occurrence.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS54062		UNITS
		MSOP-8	VSON-8	
θ_{JA}	Junction-to-ambient thermal resistance	127.1	40.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	33.4	49.7	
θ_{JB}	Junction-to-board thermal resistance	80	15.7	
ψ_{JT}	Junction-to-top characterization parameter	1	0.6	
ψ_{JB}	Junction-to-board characterization parameter	79	15.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	4.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS(1)

TEST CONDITIONS: T_J = –40°C to 125°C, VIN = 4.7 To 60 V ((unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Operating input voltage	VIN	4.7		60	V
Shutdown supply current	EN = 0V		1.7		µA
Iq Operating – Non switching	VSENSE = 0.9V, VIN = 12V		89	110	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising		1.24	1.4	V
	Falling	1	1.14		V
Input current	Enable threshold +50 mV		–4.7		µA
	Enable threshold –50 mV		–1.2		µA
Hysteresis			3.5		µA
Enable to start switching time			450		µs
VIN					
VIN start voltage	VIN rising		4.53		V
VOLTAGE REFERENCE					
Voltage reference	1mA < I_{OUT} < Minimum Current Limit	0.784	0.8	0.816	V
HIGH-SIDE MOSFET					
Switch resistance	BOOT-PH = 5.7V		1.5	2.8	Ω
LOW-SIDE MOSFET					
Switch resistance	VIN = 12V		0.8	1.5	Ω
ERROR AMPLIFIER					
Input Current	VSENSE pin		20		nA
Error amp gm	–2µA < $I_{(COMP)}$ < 2µA, $V_{(COMP)}$ = 1V		102		µMhos
EA gm during slow start	–2µA < $I_{(COMP)}$ < 2µA, $V_{(COMP)}$ = 1V, VSENSE = 0.4V		26		µMhos
Error amp dc gain	VSENSE = 0.8V		1000		V/V
Min unity gain bandwidth			0.5		MHz
Error amp source/sink	$V_{(COMP)}$ = 1V, 100 mV Overdrive		±8		µA
Start Switching Threshold			0.57		V
COMP to Iswitch gm			0.65		A/V
CURRENT LIMIT					
High side sourcing current limit threshold	VIN = 12V BOOT-PH = 5.7V	75	134		mA
Zero cross detect current			–0.7		mA
THERMAL SHUTDOWN					
Thermal shutdown			146		C
RT/CLK					
Operating frequency using RT mode		100		400	kHz
Switching frequency	$R_{(RT/CLK)}$ = 510kΩ	192	240	288	kHz
Minimum CLK pulse width			40		ns
RT/CLK voltage	$R_{(RT/CLK)}$ = 510kΩ		0.53		V
RT/CLK high threshold				1.3	V
RT/CLK low threshold		0.5			V
RT/CLK falling edge to PH rising edge delay	Measure at 240 kHz with RT resistor in series		100	200	ns
PLL lock in time	Measure at 240 kHz		100		µs
PLL frequency range		300		400	kHz

(1) The Electrical Ratings specified in this section will apply to all specifications in this document unless otherwise noted. These specifications will be interpreted as conditions that will not degrade the device's parametric or functional specifications for the life of the product containing it.

ELECTRICAL CHARACTERISTICS(1) (continued)

TEST CONDITIONS: T_J = –40°C to 125°C, VIN = 4.7 To 60 V ((unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
PH					
Minimum On time	Measured at 50% to 50% of VIN I_{OUT} = 50mA		120		ns
Dead time	VIN = 12V, I_{OUT} = 50mA, One transition		30		ns
BOOT					
BOOT to PH regulation voltage	VIN = 12V		5.7		V
BOOT-PH UVLO			2.9		V
INTERNAL SLOW START TIME					
Slow start time	f_{SW} = 240kHz, RT = 510kΩ, 10% to 90%		4.1		ms

TYPICAL CHARACTERISTICS

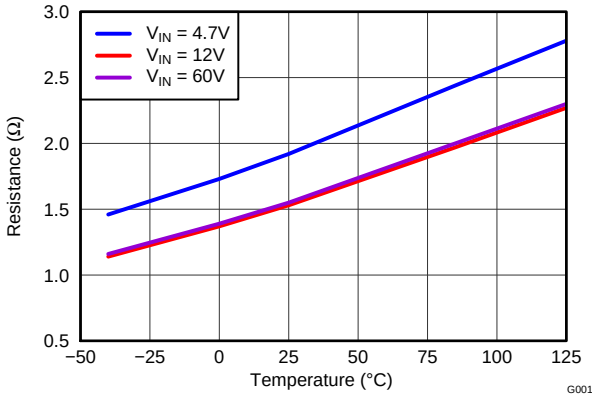


Figure 1. High Side $R_{DS(on)}$ vs Temperature

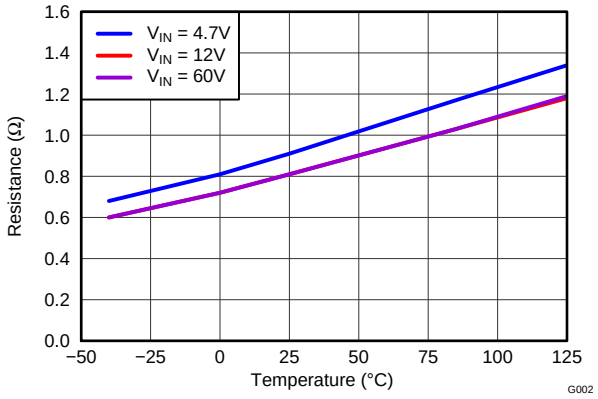


Figure 2. Low Side $R_{DS(on)}$ vs Temperature

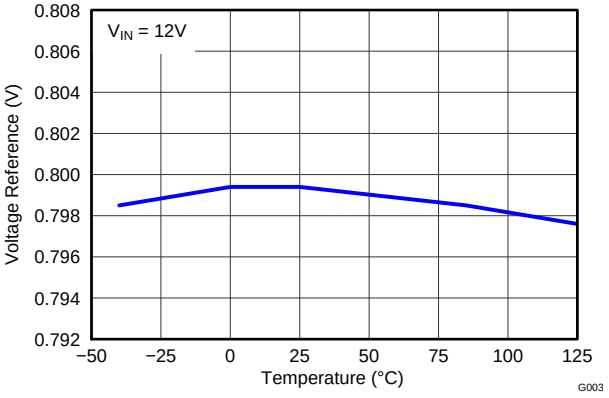


Figure 3. V_{REF} Voltage vs Temperature

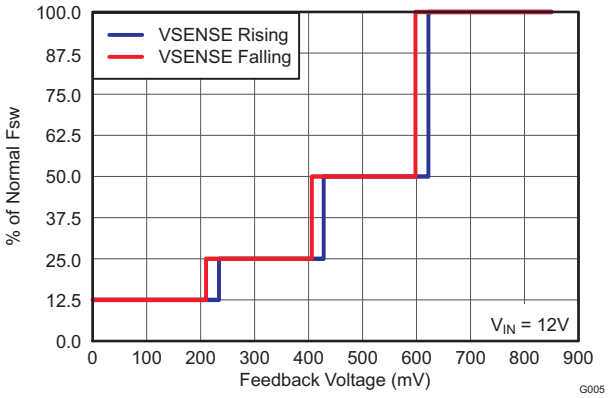


Figure 4. Frequency vs VSENSE Voltage

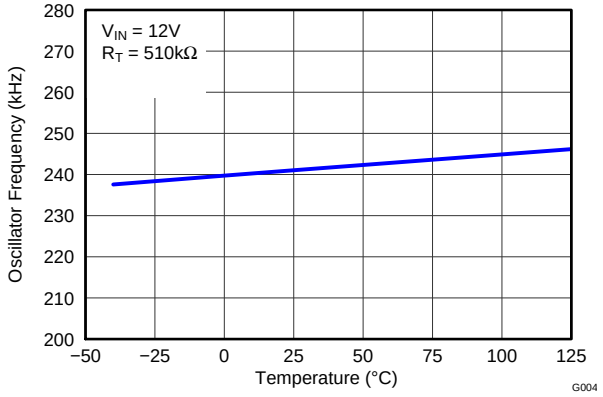


Figure 5. Frequency vs Temperature

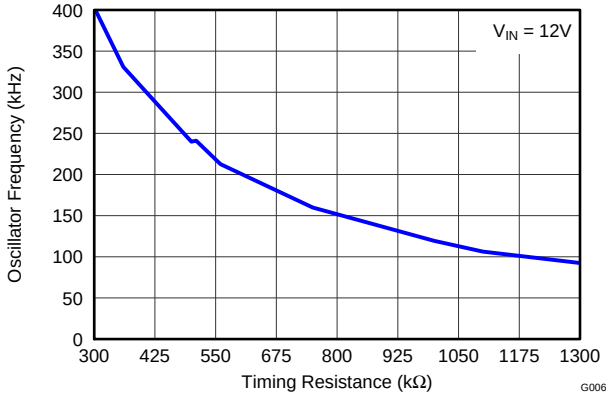


Figure 6. Frequency vs RT/CLK Resistance

TYPICAL CHARACTERISTICS (continued)

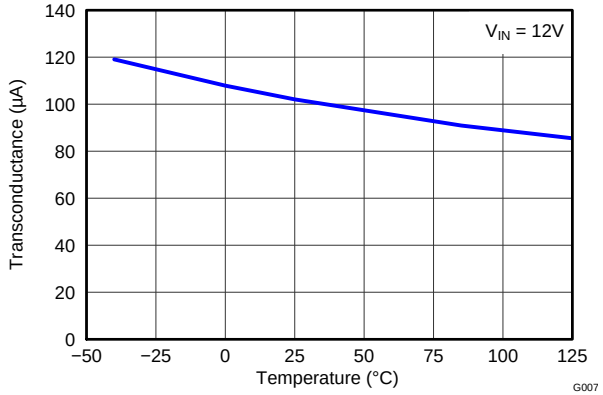


Figure 7. Error Amp Transconductance vs Temperature

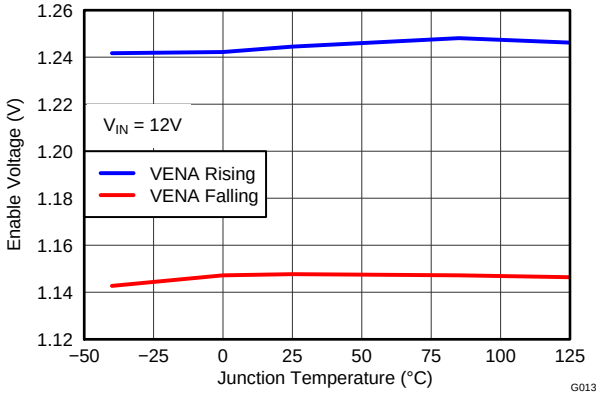


Figure 8. Enable Pin Voltage vs Temperature

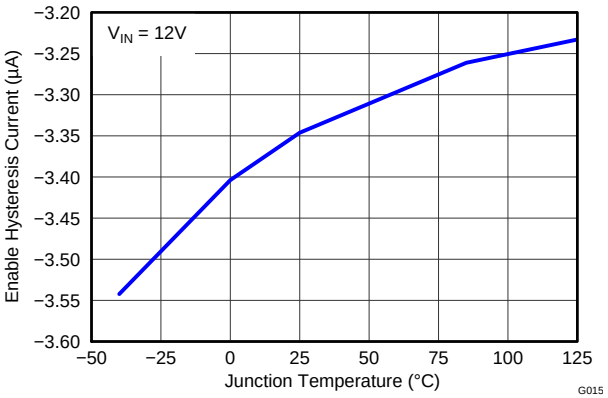


Figure 9. Enable Pin Hysteresis Current vs Temperature

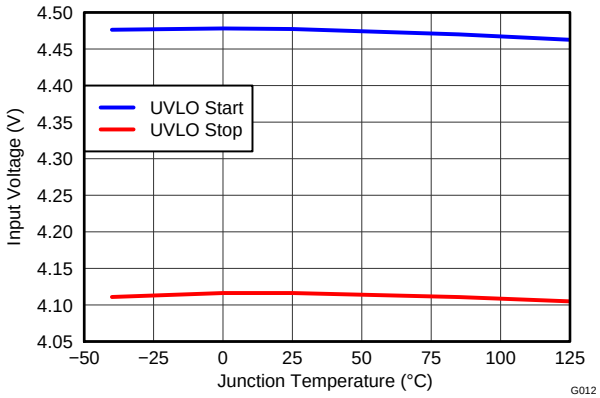


Figure 10. Input Voltage (UVLO) vs Temperature

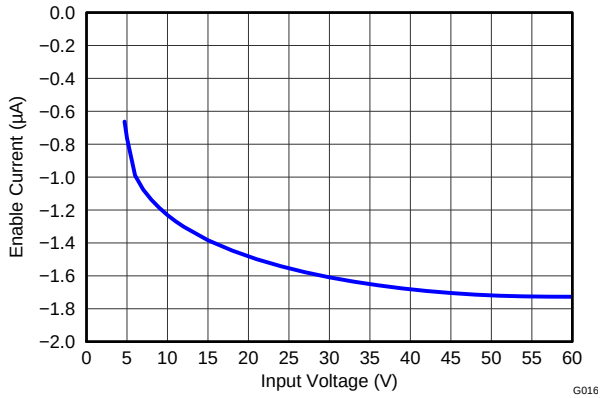


Figure 11. Enable Pin Pull Up Current vs Input Voltage

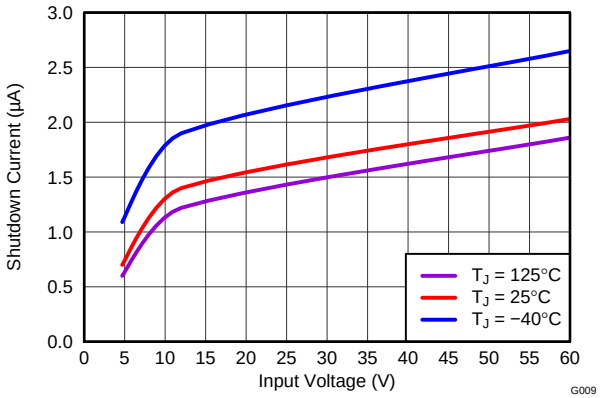


Figure 12. Shutdown Supply Current (VIN) vs Input Voltage

TYPICAL CHARACTERISTICS (continued)

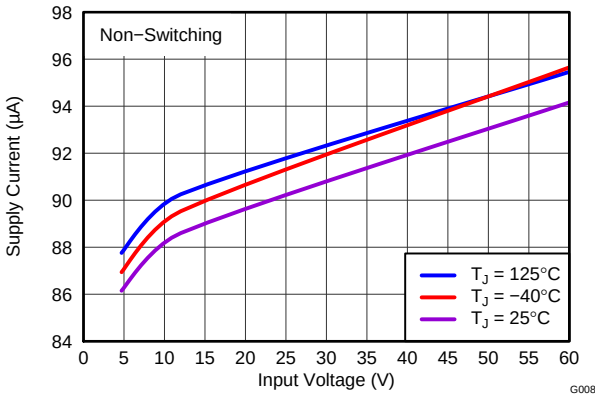


Figure 13. Supply Current (VIN pin) vs Input Voltage

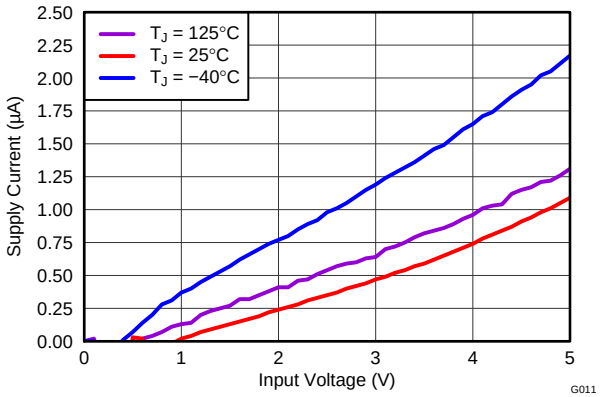


Figure 14. Supply Current (VIN pin) vs Input Voltage (0V to VSTART) EN Pin Low

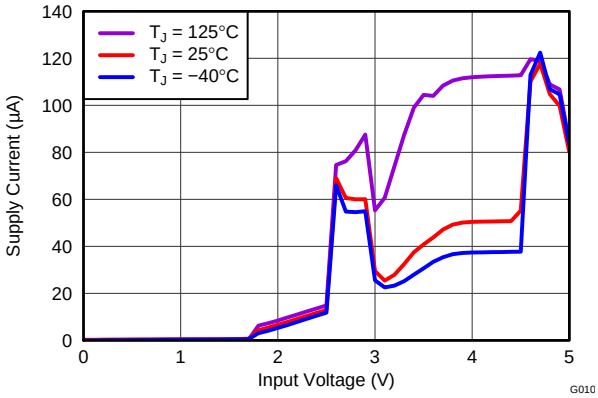


Figure 15. Supply Current (VIN pin) vs Input Voltage (0V to V_{START}) EN Pin Open

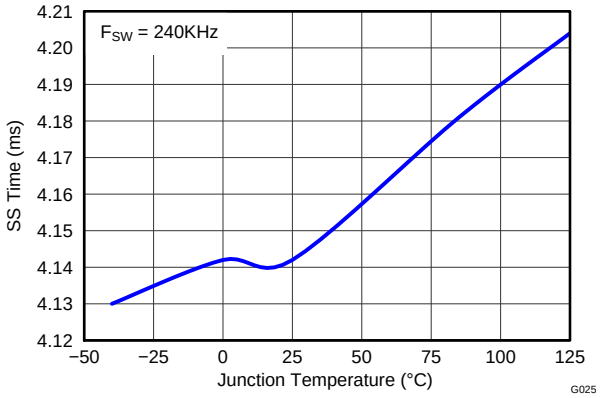


Figure 16. Slow Start Time vs Temperature

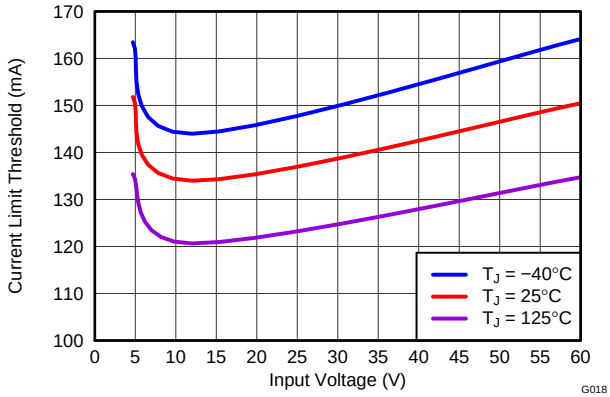


Figure 17. Current Limit vs Input Voltage

OVERVIEW

The TPS54062 device is a 60 V, 50 mA, step-down (buck) regulator with an integrated high side and low side n-channel MOSFET. To improve performance during line and load transients the device implements a constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design.

The switching frequency of 100 kHz to 400 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The device has an internal phase lock loop (PLL) on the RT/CLK pin that is used to synchronize the power switch turn on to a falling edge of an external system clock.

The TPS54062 has a default start up voltage of approximately 4.5V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage undervoltage lockout (UVLO) threshold with two external resistors. In addition, the pull up current provides a default condition. When the EN pin is floating the device will operate. The operating current is 89uA when not switching and under no load. When the device is disabled, the supply current is 1.7µA.

The integrated 1.5Ω high side MOSFET and 0.8Ω low side MOSFET allows for high efficiency power supply designs capable of delivering 50 milliamperes of continuous current to a load.

The TPS54062 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high side MOSFET is supplied by a capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high side MOSFET off when the boot voltage falls below a preset threshold. The TPS54062 can operate at high duty cycles because of the boot UVLO. The output voltage can be stepped down to as low as the 0.8 V reference.

The TPS54062 has an internal output OV protection that disables the high side MOSFET if the output voltage is 109% of the nominal output voltage.

The TPS54062 reduces external component count by integrating the slow start time using a reference DAC system.

The TPS54062 resets the slow start times during overload conditions with an overload recovery circuit. The overload recovery circuit will slow start the output from the fault voltage to the nominal regulation voltage once a fault condition is removed. A frequency foldback circuit reduces the switching frequency during startup and overcurrent fault conditions to help control the inductor current.

DETAILED DESCRIPTION

Fixed Frequency PWM Control

The TPS54062 uses an adjustable fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the level set by the COMP voltage, the power switch is turned off. The COMP pin voltage will increase and decrease as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level.

Slope Compensation Output Current

The TPS54062 adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations.

Error Amplifier

The TPS54062 has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the lower of the internal slow start voltage or the internal 0.8 V voltage reference. The transconductance (gm) of the error amplifier is 102 µA/V during normal operation. During the slow start operation, the transconductance is a fraction of the normal operating gm. The frequency compensation components (capacitor, series resistor and capacitor) are added to the COMP pin to ground.

Voltage Reference

The voltage reference system produces a precise ±2 voltage reference over temperature by scaling the output of a temperature stable band-gap circuit

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the VSENSE pin. It is recommended to use 1% tolerance or better divider resistors. Start with a 10kΩ for the R_{LS} resistor and use the Equation 1 to calculate R_{HS}.

$$R_{HS} = R_{LS} \times \left(\frac{V_{OUT} - 0.8\ V}{0.8\ V} \right) \quad (1)$$

Enable and Adjusting Undervoltage Lockout

The TPS54062 is enabled when the VIN pin voltage rises above 4.53 V and the EN pin voltage exceeds the EN rising threshold of 1.24 V. The EN pin has an internal pull-up current source, I1, of 1.2 µA that provides the default enabled condition when the EN pin floats.

If an application requires a higher input undervoltage lockout (UVLO) threshold, use the circuit shown in Figure 18 to adjust the input voltage UVLO with two external resistors. When the EN pin voltage exceeds 1.24 V, an additional 3.5 µA of hysteresis current, Ihys, is sourced out of the EN pin. When the EN pin is pulled below 1.14 V, the 3.5 µA Ihys current is removed. This additional current facilitates adjustable input voltage hysteresis. Use Equation 2 to calculate R_{UVLO1} for the desired input start and stop voltages . Use Equation 3 to similarly calculate R_{UVLO2}.

In applications designed to start at relatively low input voltages (e.g., from 4.7 V to 10V) and withstand high input voltages (e.g., from 40 V to 60 V), the EN pin may experience a voltage greater than the absolute maximum voltage of 8 V during the high input voltage condition. It is recommended to use a zener diode to clamp the pin voltage below the absolute maximum rating.

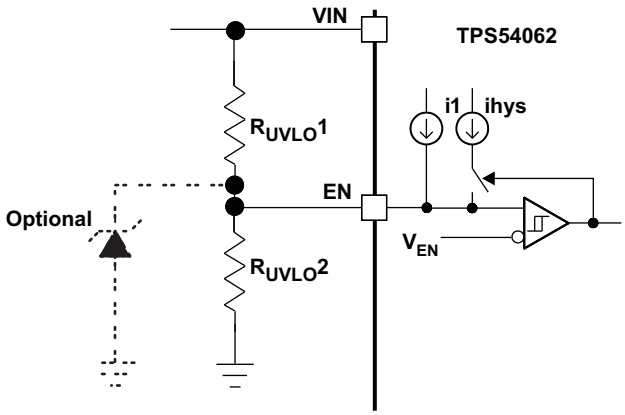


Figure 18. Adjustable Undervoltage Lock Out

$$R_{UVLO}1 = \frac{V_{START}\left(\frac{V_{ENAFALLING}}{V_{ENARISING}}\right) - V_{STOP}}{I1 \times \left(1 - \frac{V_{ENAFALLING}}{V_{ENARISING}}\right) + I_{HYS}} \quad (2)$$

$$R_{UVLO}2 = \frac{R_{UVLO}1 \times V_{ENAFALLING}}{V_{STOP} - V_{ENAFALLING} + R_{UVLO}1 \times \left(I_1 + I_{HYS}\right)} \quad (3)$$

Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS54062 is adjustable over a wide range from approximately 100 kHz to 400 kHz by placing a resistor on the RT/CLK pin. The RT/CLK pin voltage is typically 0.53 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 4. To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the supply efficiency, maximum input voltage and minimum controllable on time should be considered. The minimum controllable on time is typically 130ns and limits the maximum operating input voltage. The maximum switching frequency is also limited by the frequency shift circuit. More discussion on the details of the maximum switching frequency is located below.

$$R_T(k\Omega) = \frac{116720}{f_{SW}(kHz)^{0.9967}} \quad (4)$$

Selecting the Switching Frequency

The TPS54062 implements current mode control which uses the COMP pin voltage to turn off the high side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and COMP pin voltage are compared, when the peak switch current intersects the COMP voltage, the high side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier will respond by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally, which functions as a switch current limit.

To increase the maximum operating switching frequency at high input voltages the TPS54062 implements a frequency shift. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 to 0.8 volts on VSENSE pin. The device implements a digital frequency shift to enable synchronizing to an external clock during normal startup and fault conditions. Since the device can only divide the switching frequency by 8, there is a maximum input voltage limit in which the device operates and still have frequency shift protection. During short-circuit events (particularly with high input voltage applications), the control loop has a finite minimum controllable on time and the output has a low voltage. During the switch on time, the inductor current ramps to the peak current limit because of the high input voltage and minimum on time. During the switch off time, the inductor would normally not have enough off time and output voltage for the inductor to ramp down by the ramp up amount. The frequency shift effectively increases the off time allowing the current to ramp down.

$$f_{SW}(\text{maxskip}) = \left(\frac{1}{t_{ON}}\right) \times \left(\frac{V_{OUT} + R_{LS} \times I_O + R_{DC} \times I_O}{V_{IN} - I_O \times R_{HS} + I_O \times R_{LS}}\right) \quad (5)$$

$$f_{SW}(\text{shift}) = \left(\frac{f\text{div}}{t_{ON}}\right) \times \left(\frac{V_{OUTSC} + R_{LS} \times I_{CL} + R_{DC} \times I_{CL}}{V_{IN} - I_{CL} \times R_{HS} + I_{CL} \times R_{LS}}\right) \quad (6)$$

Where:

I_O = Output current
I_{CL} = Current Limit
V_{IN} = Input Voltage
V_{OUT} = Output Voltage
V_{OUTSC} Output Voltage during short
R_{DC} = Inductor resistance
R_{HS} = High side MOSFET resistance
R_{LS} = Low side MOSFET resistance
t_{on} = Controllable on time
fdiv = Frequency divide (equals 1, 2, 4, or 8)

How to Interface to RT/CLK Pin

The RT/CLK pin can be used to synchronize the regulator to an external system clock. To implement the synchronization feature connect a square wave to the RT/CLK pin through one of the circuit networks shown in Figure 19. The square wave amplitude must transition lower than 0.5 V and higher than 1.3V on the RT/CLK pin and have an on time greater than 40 ns and an off time greater than 40ns. The synchronization frequency range is 300 kHz to 400 kHz. The rising edge of the PH will be synchronized to the falling edge of RT/CLK pin signal. The external synchronization circuit should be designed in such a way that the device will have the default frequency set resistor connected from the RT/CLK pin to ground should the synchronization signal turn off. It is recommended to use a frequency set resistor connected as shown in Figure 19 through another resistor (e.g., 50Ω) to ground for clock signal that are not Hi-Z or 3-state during the off state. The sum of the resistance should set the switching frequency close to the external CLK frequency. It is recommended to ac couple the synchronization signal through a 10pF ceramic capacitor to RT/CLK pin. The first time the CLK is pulled above the CLK threshold the device switches from the RT resistor frequency to PLL mode. The internal 0.5 V voltage source is removed and the CLK pin becomes high impedance as the PLL starts to lock onto the external signal. Since there is a PLL on the regulator the switching frequency can be higher or lower than the frequency set with the external resistor. The device transitions from the resistor mode to the PLL mode and then will increase or decrease the switching frequency until the PLL locks onto the CLK frequency within 100 microseconds. When the device transitions from the PLL to resistor mode the switching frequency will slow down from the CLK frequency to 150 kHz, then reapply the 0.5V voltage and the resistor will then set the switching frequency. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 to 0.8 volts on VSENSE pin. The device implements a digital frequency shift to enable synchronizing to an external clock during normal startup and fault conditions.

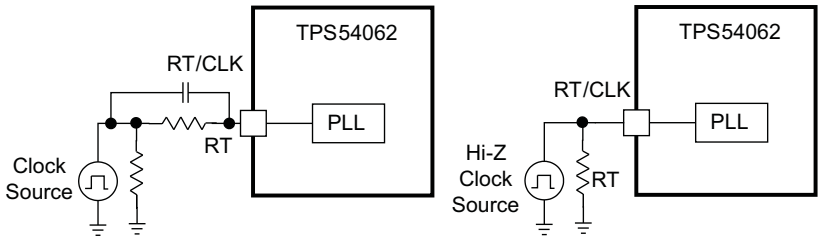


Figure 19. Synchronizing to a System Clock

Overvoltage Transient Protection

The TPS54062 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients on power supply designs with low value output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier will respond by clamping the error amplifier output to a high voltage. Thus, requesting the maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state duty cycle. In some applications, the power supply output voltage can respond faster than the error amplifier output can respond, this actuality leads to the possibility of an output overshoot.

The OVTP feature minimizes the output overshoot, when using a low value output capacitor, by implementing a circuit to compare the VSENSE pin voltage to OVTP threshold which is 109% of the internal voltage reference. If the VSENSE pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVTP threshold, the high side MOSFET is allowed to turn on at the next clock cycle.

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 146°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 146°C, the device reinitiates the power up sequence by restarting the internal slow start.

DESIGN GUIDE – STEP-BY-STEP DESIGN PROCEDURE No.1

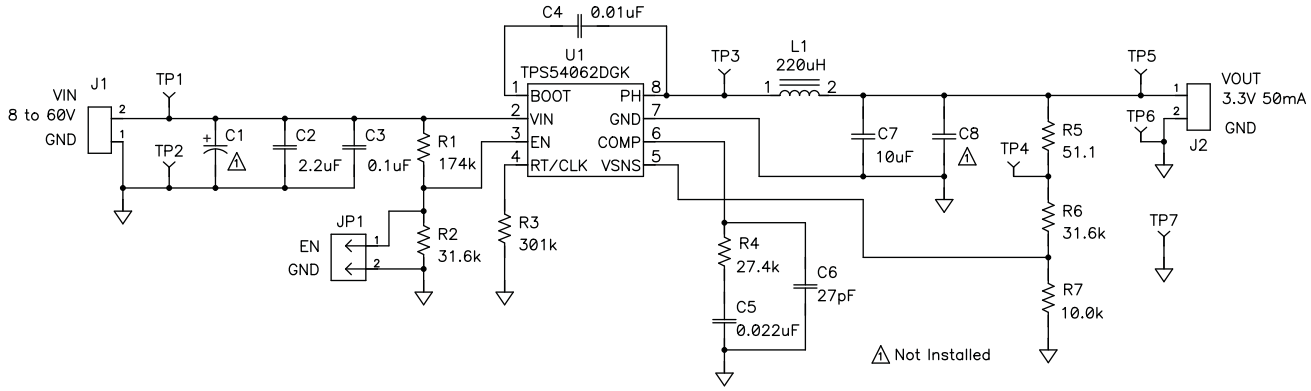


Figure 20. Application Schematic

This example details the design of a continuous conduction mode (CCM) switching regulator design using ceramic output capacitors. If a low output current design is needed go to the design procedure Number 2. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level. For this example, we will start with the following known parameters:

Output Voltage	3.3V
Transient Response 0 to 50mA load step	ΔV_{OUT} = 4%
Maximum Output Current	50mA
Input Voltage	24 V nom. 8V to 60V
Output Voltage Ripple	0.5% of V_{OUT}
Start Input Voltage (rising VIN)	7.88V
Stop Input Voltage (falling VIN)	6.66V

Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, the user will want to choose the highest switching frequency possible since this will produce the smallest solution size. The high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The switching frequency that can be selected is limited by the minimum on-time of the internal power switch, the input voltage and the output voltage and the frequency shift limitation.

Equation 5 and Equation 6 must be used to find the maximum switching frequency for the regulator, choose the lower value of the two equations. Switching frequencies higher than these values will result in pulse skipping or the lack of overcurrent protection during a short circuit. The typical minimum on time, t_{on}min, is 130ns for the TPS54062. For this example, the output voltage is 3.3V and the maximum input voltage is 60 V, which allows for a maximum switch frequency up to 400 kHz when including the inductor resistance, on resistance and diode voltage in Equation 5 or Equation 6. To ensure overcurrent runaway is not a concern during short circuits in your design use Equation 6 to determine the maximum switching frequency. With a maximum input voltage of 60V, inductor resistance of 3.7 Ω, high side switch resistance of 2.3 Ω, low side switch resistance of 1.1Ω, a current limit value of 120 mA and a short circuit output voltage of 0.1 V.

The maximum switching frequency is 400 kHz in both cases and a switching frequency of 400 kHz is used. To determine the timing resistance for a given switching frequency, use Equation 4. The switching frequency is set by resistor R3 shown in Figure 20. R3 is calculated to be 298 kΩ. A standard value of 301 kΩ is used.

Output Inductor Selection (LO)

To calculate the minimum value of the output inductor, use Equation 7. KIND is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current will be filtered by the output capacitor. Therefore, choosing high inductor ripple currents will impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, the following guidelines may be used. Typically it is recommended to use KIND values in the range of 0.2 to 0.4; however, for designs using low ESR output capacitors such as ceramics and low output currents, a value as high as KIND = 1 may be used. In a wide input voltage regulator, it is best to choose an inductor ripple current on the larger side. This allows the inductor to still have a measurable ripple current with the input voltage at its minimum. For this design example, use KIND = 0.8 and the minimum inductor value is calculated to be 195 µH. For this design, a near standard value was chosen: 220 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 9 and Equation 10.

For this design, the RMS inductor current is 50 mA and the peak inductor current is 68 mA. The chosen inductor is a Coilcraft LPS4018-224ML. It has a saturation current rating of 235 mA and an RMS current rating of 200 mA. As the equation set demonstrates, lower ripple currents will reduce the output voltage ripple of the regulator but will require a larger value of inductance. Selecting higher ripple currents will increase the output voltage ripple of the regulator but allow for a lower inductance value. The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

$$L_O\text{min} \geq \left(\frac{V_{IN}\text{max} - V_{OUT}}{\text{Kind} \times I_O} \right) \times \frac{V_{OUT}}{V_{IN}\text{max} \times f_{SW}} \tag{7}$$

$$I_{RIPPLE} \geq \frac{V_{OUT} \times (V_{IN}\text{max} - V_{OUT})}{V_{IN}\text{max} \times L_O \times f_{SW}} \tag{8}$$

$$I_L\text{rms} = \sqrt{I_O^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times (V_{IN}\text{max} - V_{OUT})}{V_{IN}\text{max} \times L_O \times f_{SW}} \right)^2} \tag{9}$$

$$I_L\text{peak} = I_{OUT} + \frac{I_{RIPPLE}}{2} \tag{10}$$

Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor will determine the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these three criteria. The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator can not. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator also will temporarily not be able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 14 shows the minimum output capacitance necessary to accomplish this. Where ΔIout is the change in output current, f_{sw} is the regulators switching frequency and ΔVout is the allowable change in the output voltage.

For this example, the transient load response is specified as a 4% change in Vout for a load step from 0A (no load) to 50 mA (full load). For this example, ΔI_{OUT} = 0.05-0 = 0.05 and ΔV_{OUT} = 0.04 × 3.3 = 0.132.

Using these numbers gives a minimum capacitance of 1.89 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR that should be taken into account. The low side FET of the regulator emulates a diode so it can not sink current so any stored energy in the inductor will produce an output voltage overshoot when the load current rapidly decreases, see Figure 26. The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high load current to a lower load current. The excess energy that gets stored in the output capacitor will increase the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Equation 13 is used to calculate the minimum capacitance to keep the output voltage overshoot to a desired value. Where L is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, VF is the final peak output voltage, and Vi is the initial capacitor voltage. For this example, the worst case load step will be from 50 mA to 0A. The output voltage will increase during this load transition and the stated maximum in our specification is 4% of the output voltage. This will make VF = 1.04 × 3.3 = 3.432 V. Vi is the initial capacitor voltage which is the nominal output voltage of 3.3 V. Using these numbers in Equation 14 yields a minimum capacitance of 0.619 µF.

Equation 12 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where f_{SW} is the switching frequency, Voripple is the maximum allowable output voltage ripple, and Iripple is the inductor ripple current. Equation 13 yields 0.671 µF. Equation 15 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 15 indicates the ESR should be less than 0.466Ω.

The most stringent criteria for the output capacitor is 1.89 µF of capacitance to keep the output voltage in regulation during an load transient.

Additional capacitance de-ratings for aging, temperature and dc bias should be factored in which will increase this minimum value. For this example, 10 µF, 10V X5R ceramic capacitor with 0.003 Ω of ESR will be used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the Root Mean Square (RMS) value of the maximum ripple current.

Equation 11 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 11 yields 10.23 mA.

$$IC_Orms = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times (V_{IN}max - V_{OUT})}{V_{IN}max \times L_O \times f_{SW}} \right) \quad (11)$$

$$C_O1 \geq \frac{I_{RIPPLE}}{V_{RIPPLE}} \times \left(\frac{1}{8 \times f_{SW}} \right) \quad (12)$$

$$C_O2 \geq L_O \times \frac{\left(I_O^2 - 0^2\right)}{\left(V_O + \Delta V\right)^2 - V_O^2} \quad (13)$$

$$C_O3 \geq \frac{I_O}{\Delta V} \frac{2}{f_{SW}} \quad (14)$$

$$R_C \leq \frac{V_{RIPPLE}}{I_{RIPPLE}} \quad (15)$$

Input capacitor

The TPS54062 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 1µF of effective capacitance and in some applications a bulk capacitance. The effective capacitance includes any dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a rms current rating greater than the maximum rms input current of the TPS54062. The input rms current can be calculated using Equation 16. The value of a ceramic capacitor varies significantly over temperature and the amount of dc bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the dc bias taken into account. The capacitance value of a capacitor decreases as the dc bias across a capacitor increases. For this example design, a ceramic capacitor with at least a 100 V voltage rating is required to support the maximum input voltage. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using rearranging Equation 17.

Using the design example values, Ioutmax = 50 mA, C_{IN} = 2.2 µF, f_{SW} = 400 kHz, yields an input voltage ripple of 14.2 mV and a rms input ripple current of 24.6 mA.

$$IC_{IN}rms = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}min} \times \frac{\left(V_{IN}min - V_{OUT}\right)}{V_{IN}Min}} \quad (16)$$

$$C_{IN} \geq \frac{I_O}{V_{IN}ripple} \times \left(\frac{0.25}{f_{SW}}\right) \quad (17)$$

Bootstrap Capacitor Selection

A 0.01-µF ceramic capacitor must be connected between the BOOT and PH pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have a 10V or higher voltage rating.

Under Voltage Lock Out Set Point

The Under Voltage Lock Out (UVLO) can be adjusted using an external voltage divider on the EN pin of the TPS54062. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 7.88 V (enabled). After the regulator starts switching, it should continue to do so until the input voltage falls below 6.66 V (UVLO stop). The programmable UVLO and enable voltages are set using a resistor divider between Vin and ground to the EN pin. Equation 2 through Equation 3 can be used to calculate the resistance values necessary. For the example application, a 174 kΩ resistor between Vin and EN and a 31.6 kΩ resistor between EN and ground are required to produce the 7.88 and 6.66 volt start and stop voltages.

Output Voltage and Feedback Resistors Selection

For the example design, 10 kΩ was selected for R_{LS}. Using Equation 1, R_{HS} is calculated as 31.25 kΩ. The nearest standard 1% resistor is 31.6 kΩ.

Closing the Loop

There are several methods used to compensate DC/DC regulators. The method presented here is easy to calculate and ignores the effects of the slope compensation that is internal to the device. Since the slope compensation is ignored, the actual cross over frequency will usually be lower than the cross over frequency used in the calculations. This method assume the crossover frequency is between the modulator pole and the ESR zero and the ESR zero is at least 10 times greater the modulator pole. Use SwitcherPro™ software for a more accurate design.

To get started, the modulator pole, fpole, and the ESR zero, fzero must be calculated using Equation 18 and Equation 19. For Cout, use a derated value of 8.9 µF. Use Equation 21 and Equation 22, to estimate a starting point for the crossover frequency, fco, to design the compensation. For the example design, fpole is 271 Hz and fzero is 5960 kHz.

Equation 21 is the geometric mean of the modulator pole and the esr zero and Equation 22 is the mean of modulator pole and the switching frequency. Equation 21 yields 40.29 kHz and Equation 22 gives 7.36 kHz. Use a frequency near the lower value of Equation 21 or Equation 22 for an initial crossover frequency.

For this example, fco is 7.8 kHz. Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole.

To determine the compensation resistor, R4, use Equation 22. Assume the power stage transconductance, gmps, is 0.65 A/V. The output voltage, Vo, reference voltage, V_{REF}, and amplifier transconductance, gmea, are 3.3 V, 0.8 V and 102 µA/V, respectively.

R4 is calculated to be 27.1 kΩ, use the nearest standard value of 27.4 kΩ. Use Equation 23 to set the compensation zero to the modulator pole frequency. Equation 23 yields 0.021.4 µF for compensating capacitor C5, a 0.022 µF is used on the board. Use the larger value of Equation 24 and Equation 25 to calculate the C6 value, to set the compensation pole. Equation 25yields 29 pF so the nearest standard of 27 pF is used.

$$fpole(Hz) = \frac{1}{\frac{V_O}{I_O} \times C_O \times 2 \times \pi} \quad (18)$$

$$fzero(Hz) = \frac{1}{R_C \times C_O \times 2 \times \pi} \quad (19)$$

$$fco1(Hz) = \left(fzero \times fpole\right)^{0.5} \quad (20)$$

$$fco2(Hz) = \left(\frac{fsw}{2} \times fpole\right)^{0.5} \quad (21)$$

$$R4 = \frac{2 \times \pi \times f_{CO} \times C_O}{gmps} \times \frac{V_O}{V_{REF} \times gmea} \quad (22)$$

$$C5 = \frac{1}{2 \times \pi \times R4 \times f_{POLE}} \quad (23)$$

$$C6 = \frac{R_C \times C_O}{R4} \quad (24)$$

$$C6 = \frac{1}{R4 \times f_{SW} \times \pi} \quad (25)$$

Characteristics

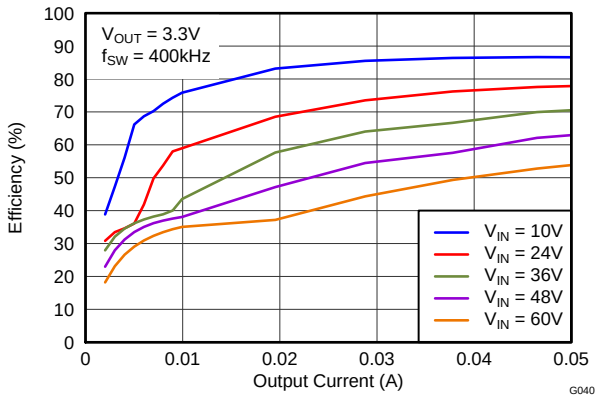


Figure 21. Efficiency vs Output Current

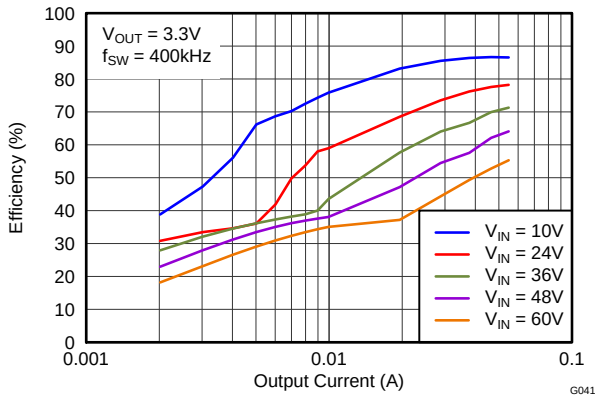


Figure 22. Efficiency vs Output Current

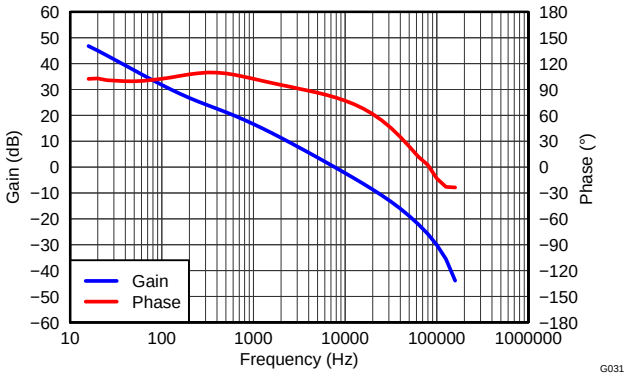


Figure 23. Gain vs Phase

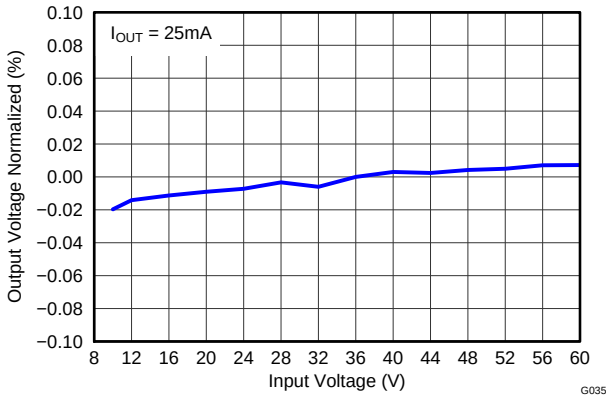


Figure 24. Output Voltage vs Input Voltage

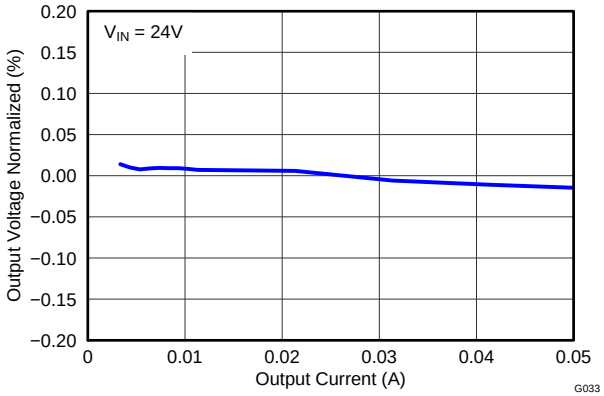


Figure 25. Output Voltage vs Output Current

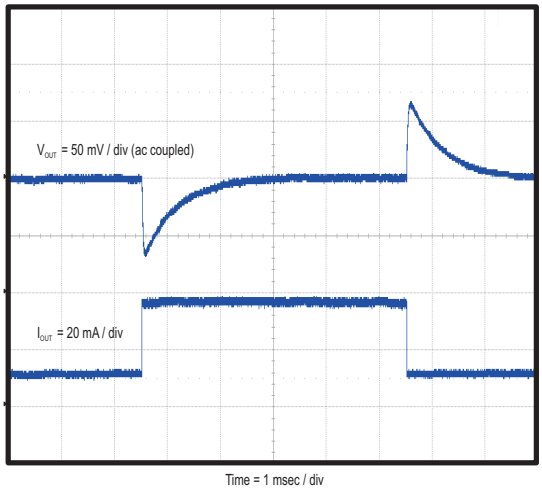


Figure 26. Load Transient

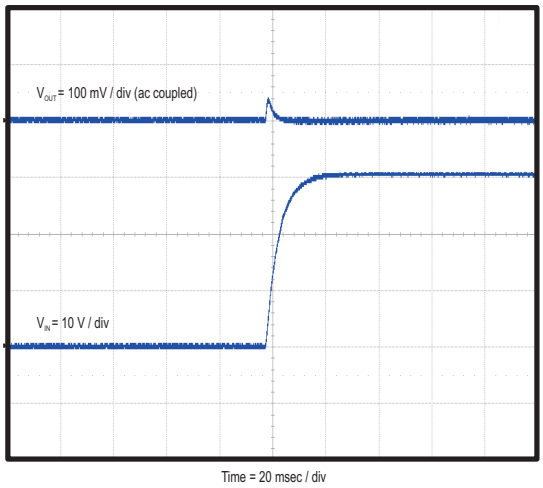


Figure 27. Line Transient

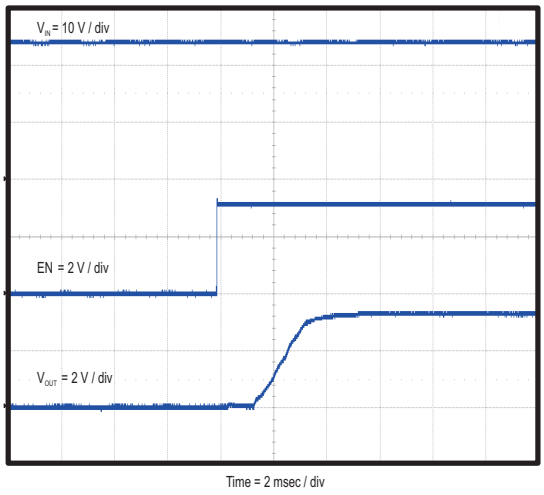


Figure 28. Startup with ENA

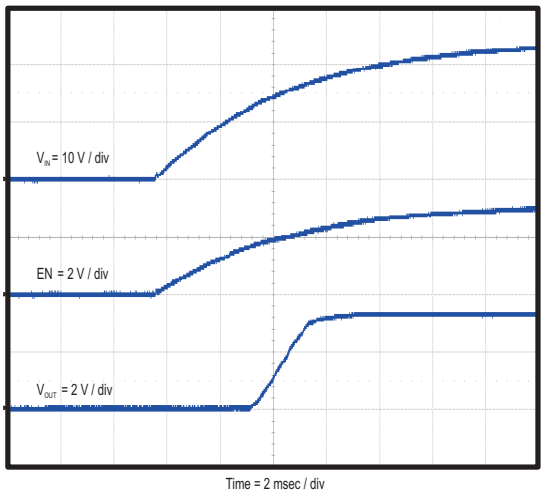


Figure 29. Startup with V_{IN}

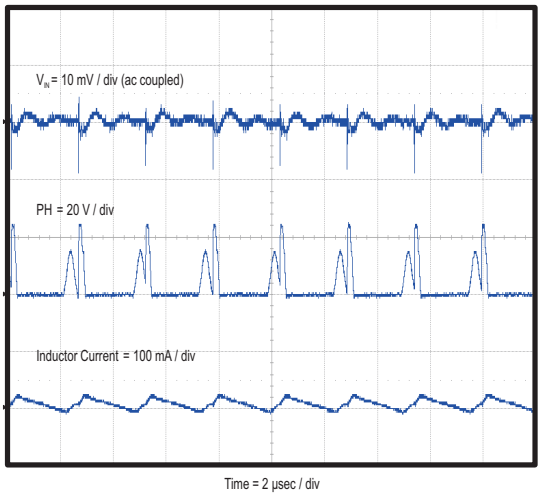


Figure 30. Input Ripple in DCM

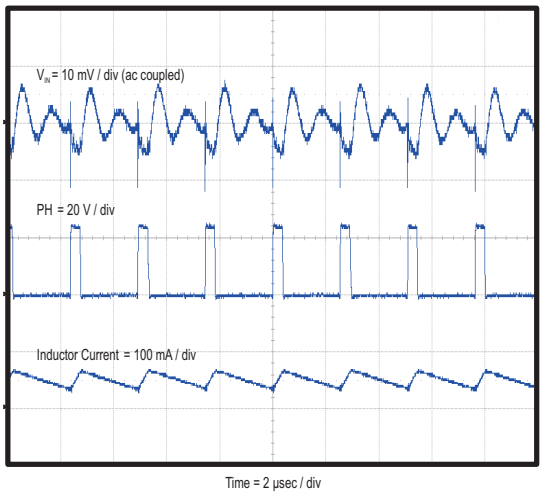


Figure 31. Input Ripple in CCM

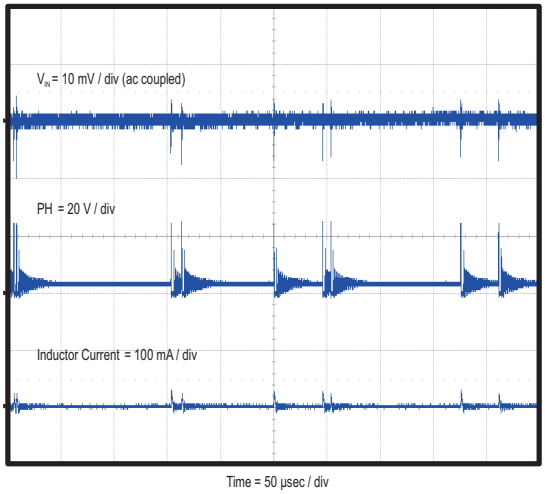


Figure 32. Input Ripple Skip

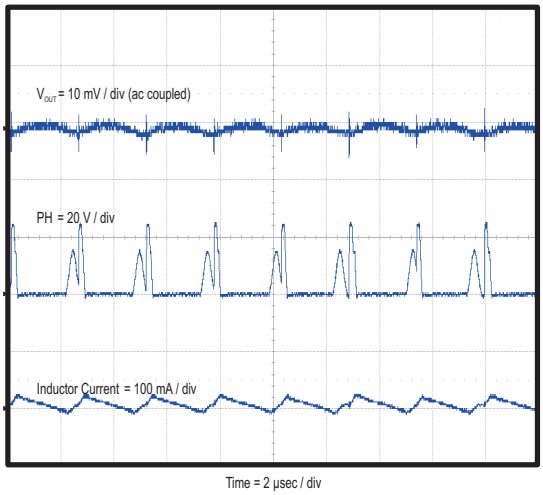


Figure 33. Output Ripple in DCM

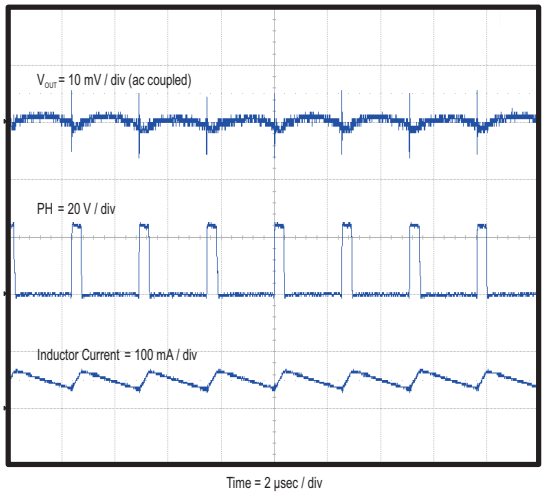


Figure 34. Output Ripple in CCM

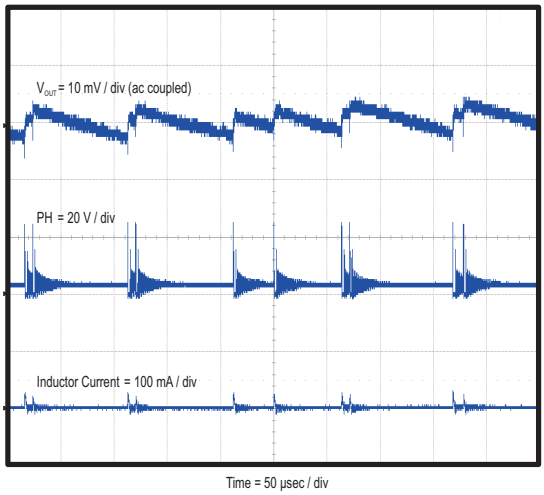


Figure 35. Output Ripple Skip

DESIGN GUIDE – STEP-BY-STEP PROCEDURE Number 2

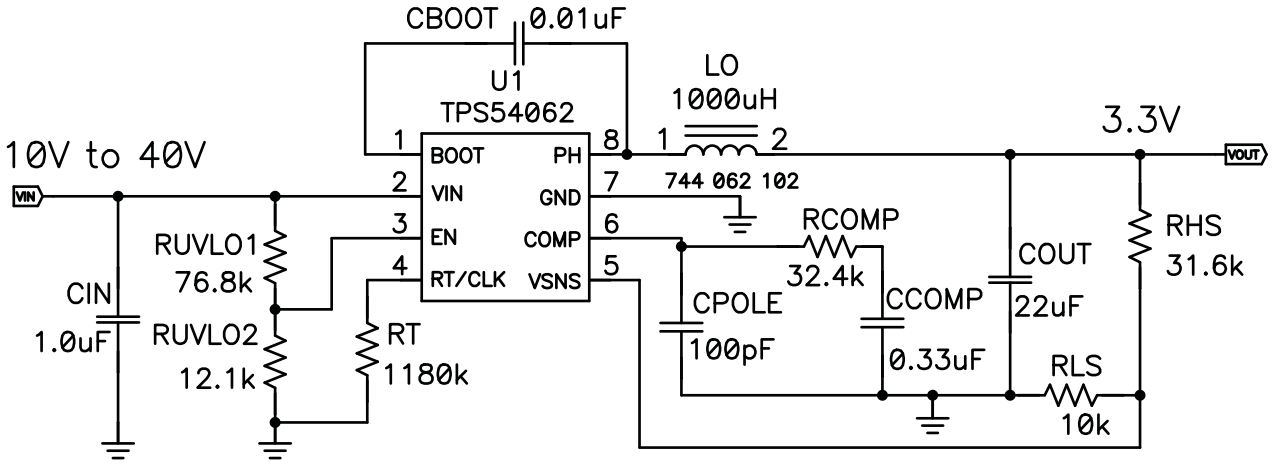


Figure 36. DCM Application Schematic

For Designing an Efficient, Low Output Current Power Supply at a Fixed Switching Frequency

This example details the design of a low output current, fixed switching regulator design using ceramic output capacitors. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level. For this example, we will start with the following known parameters:

Output Voltage	3.3 V
Transient Response 0 to 15 mA load step	ΔV_{OUT} = 4%
Maximum Output Current	10 mA
Minimum Output Current	3 mA
Input Voltage	24 V nom. 10 V to 40 V
Output Voltage Ripple	0.5% of V_{OUT}
Switching Frequency	100 kHz
Start Input Voltage (rising VIN)	9 V
Stop Input Voltage (falling VIN)	8 V

It is most desirable to have a power supply that is efficient and has a fixed switching frequency at low output currents. A fixed frequency power supply will have a predictable output voltage ripple and noise. Using a traditional continuous conduction mode (CCM) design method to calculate the output inductor will yield a large inductance for a low output current supply. Using a CCM inductor will result in a large sized supply or will affect efficiency from the large dc resistance an alternative is to operate in discontinuous conduction mode (DCM). Use the procedure below to calculate the components values for designing a power supply operating in discontinuous conduction mode. The advantage of operating a power supply in DCM for low output current is the fixed switching frequency, lower output inductance, and lower dc resistance on the inductor. Use the frequency shift and skip equations to estimate the maximum switching frequency.

The TPS54062 is designed for applications which require a fixed operating frequency and low output voltage ripple at low output currents, thus, the TPS54062 does not have a pulse skip mode at light loads. Since the device has a minimum controllable on time, there is an output current at which the power supply will pulse skip. To ensure that the supply does not pulse skip at output current of the application the inductor value will be need to be selected greater than a minimum value. The minimum inductance needed to maintain a fixed switching frequency at the minimum load is calculated to be 0.9mH using Equation 26. Since the equation is ideal and was derived without losses, assume the minimum controllable light load on time, tonminll, is 350ns. To maintain DCM operation the inductor value and output current need to stay below a maximum value. The maximum inductance is calculated to be 1.42mH using Equation 27. A 744062102 inductor from Wurth Elektronik is selected. If CCM operation is necessary, use the previous design procedure.

Use Equation 28, to make sure the minimum current limit on the high side power switch is not exceeded at the maximum output current. The peak current is calculated as 23.9mA and is lower than the 134 mA current limit. To determine the rms current for the inductor and output capacitor, it is necessary to calculate the duty cycle. The duty cycle, D1, for a step down regulator in DCM is calculated in Equation 29. D1 is the portion of the switching cycle the high side power switch is on, and is calculated to be 0.1153. D2 is the portion of the switching cycle the low side power switch is on, and is calculated to be 0.7253.

Using the Equation 31 and Equation 32, the rms current of the inductor and output capacitor are calculated, to be 12.8mA and 7.6mA respectively. Select components that ratings exceed the calculated rms values. Calculate the output capacitance using the Equation 33 to Equation 35 and use the largest value, Vripple is the steady state voltage ripple and deltaV is voltage change during a transient. A minimum of 1.5 µF capacitance is calculated. Additional capacitance de-ratings for aging, temperature and dc bias should be factored in which increases this minimum value. For this example, a 22 µF 6.3 V X7R ceramic capacitor with 5mΩ ESR is used. To have a low output ripple power supply use a low esr capacitor. Use Equation 36 to estimate the maximum esr for the output capacitor. Equation 37 and Equation 38 estimate the rms current and capacitance for the input capacitor. An rms current of 3.7 mA and capacitance of 0.2 µF is calculated. A 1 µF 100V/X7R ceramic is used for this example.

$$L_O\text{min} \geq \left(\frac{V_S\text{max} - V_O}{V_O}\right) \times \left(\frac{V_S\text{max}}{2}\right) \times \frac{t_O\text{nmin}^2}{I_O\text{min}} \; x \, f_{SW} \tag{26}$$

$$L_O\text{max} \leq \left(\frac{V_S\text{min} - V_O}{2}\right) \times \left(\frac{V_O}{V_S\text{min}}\right) \times \frac{1}{f_{SW} \times I_O} \tag{27}$$

$$I_L\text{peak} = \left(\frac{2 \times V_O \times I_O\text{max} \times (V_S\text{max} - V_O)}{V_S\text{max} \times L_O \times f_{SW}}\right)^{0.5} \tag{28}$$

$$D1 = \left(\frac{2 \times V_O \times I_O \times L_O \times f_{SW}}{V_S \times (V_S - V_O)}\right)^{0.5} \tag{29}$$

$$D2 = \left(\frac{V_S - V_O}{V_O}\right) \times D1 \tag{30}$$

$$I_L\text{rms} = I_L\text{peak} \times \left(\frac{D1 + D2}{3}\right)^{0.5} \tag{31}$$

$$I_{CO}\text{rms} = I_L\text{peak} \times \left(\left(\frac{D1 + D2}{3}\right) - \left(\frac{D1 + D2}{4}\right)^2\right)^{0.5} \tag{32}$$

$$C_O1 \leq \frac{I_L\text{peak}}{V_{RIPPLE}} \times \left(\frac{D1 + D2}{8 \times f_{SW}}\right) \tag{33}$$

$$C_O2 \geq L_O \times \frac{\left(Io^2 - 0^2\right)}{(V_O + \Delta V)^2 - V_O{}^2} \tag{34}$$

$$C_O3 \geq \frac{I_O}{\Delta V} \frac{1}{f_{CO}} \tag{35}$$

$$R_C \leq \frac{V_{RIPPLE}}{I_L\text{peak}} \tag{36}$$

$$I_{CIN}\text{rms} = I_L\text{peak} \times \left(\left(\frac{D1}{3}\right) - \left(\frac{D1}{4}\right)^2\right)^{0.5} \tag{37}$$

$$C_{IN} \geq \frac{I_O}{V_{IN}\text{RIPPLE}} \times \left(\frac{0.25}{f_{SW}}\right) \tag{38}$$

Closing the Feedback Loop

The method presented here is easy to calculate and includes the effect of the slope compensation that is internal to the device. This method assumes the crossover frequency is between the modulator pole and the esr zero and the esr zero is at least 10 times greater the modulator pole. Once the output components are determined, use the equations below to close the feedback loop. A current mode controlled power supply operating in DCM has a transfer function which has an esr zero and pole as shown in Equation 39. To calculate the current mode power stage gain, first calculate, Kdcm, DCM gain, and Fm, modulator gain, in Equation 40 and Equation 41. Kdcm and Fm are 26.3 and 1.34 respectively. The location of the pole and esr zero are calculated using Equation 42 and Equation 43 . The pole and zero are 67 Hz and 2 MHz, respectively. Use the lower value of Equation 44 and Equation 45 as a starting point for the crossover frequency. Equation 44 is the geometric mean of the power stage pole and the esr zero and Equation 45 is the mean of power stage pole and the switching frequency. The crossover frequency is chosen as 2.5 kHz from Equation 45.

To determine the compensation resistor, R_{COMP}, use Equation 46. Assume the power stage transconductance, gmps, is 0.65 A/V. The output voltage, V_O, reference voltage, V_{REF}, and amplifier transconductance, gmea, are 3.3 V, 0.8 V and 102 µA/V, respectively. R_{COMP} is calculated to be 32.7 kΩ, use the nearest standard value of 32.4 kΩ. Use Equation 47 to set the compensation zero to the modulator pole frequency. Equation 47 yields 139 nF for compensating capacitor C_{COMP}, a 330 nF is used on the board. Use the larger value of Equation 48 or Equation 49 to calculate the C_{POLE}, to set the compensation pole. Equation 49 yields 98 pF so the nearest standard of 100 pF is used.

$$Gdcm(s) \approx Fm \times Kdcm \times \frac{1 + \frac{s}{2 \times \pi \times f_{ZERO}}}{1 + \frac{s}{2 \times \pi \times f_{POLE}}} \tag{39}$$

$$Kdcm = \frac{2}{D1} \times \frac{V_O \times (V_S - V_O)}{V_S \times \left(2 + \frac{Rdc}{\frac{V_O}{I_O}}\right) - V_O} \tag{40}$$

$$Fm = \frac{gmps}{\left(\frac{V_S - V_O}{L_O \times f_{SW}}\right) + 0.277} \tag{41}$$

$$f_{POLE}(Hz) = \frac{1}{\frac{V_O}{I_O} \times C_O \times 2 \times \pi} \times \left(\frac{2 - \frac{V_O}{V_S}}{1 - \frac{V_O}{V_S}}\right) \tag{42}$$

$$f_{ZERO}(Hz) = \frac{1}{R_C \times C_O \times 2 \times \pi} \tag{43}$$

$$f_{CO1}(Hz) = \left(f_{ZERO} \times f_{POLE}\right)^{0.5} \tag{44}$$

$$f_{CO2}(Hz) = \left(f_{SW} \times f_{POLE}\right)^{0.5} \tag{45}$$

$$R_{COMP} = \frac{f_{CO}}{Kdcm \; x \; Fm \; x \; f_{POLE}} \; x \; \frac{V_O}{V_{REF} \; x \; gmea} \tag{46}$$

$$C_{COMP} = \frac{1}{2 \times \pi \times R_{COMP} \times Kdcm \times Fm} \tag{47}$$

$$C_{POLE1} = \frac{R_C \times C_O}{R_{COMP}} \tag{48}$$

$$C_{POLE2} = \frac{1}{R_{COMP} \times f_{SW} \times \pi} \tag{49}$$

Characteristics

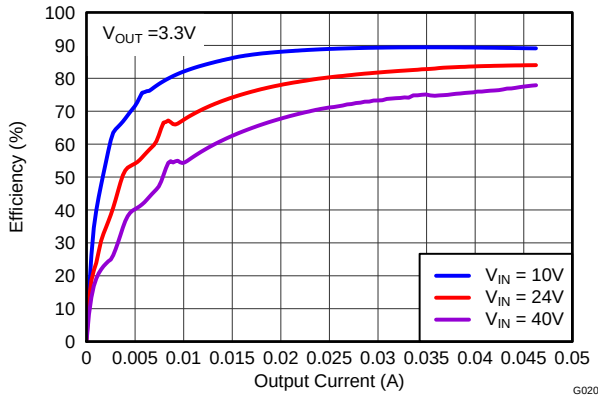


Figure 37. Efficiency vs Output Current

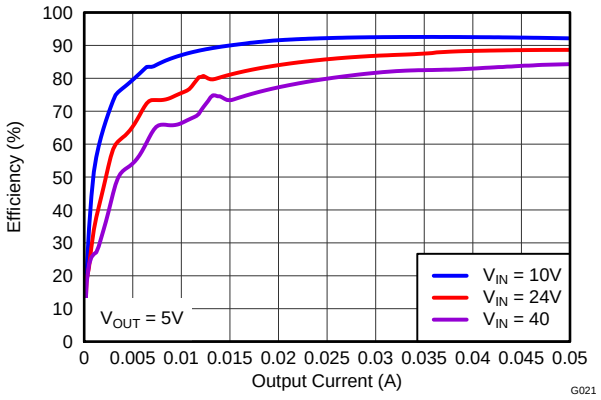


Figure 38. Efficiency vs Output Current

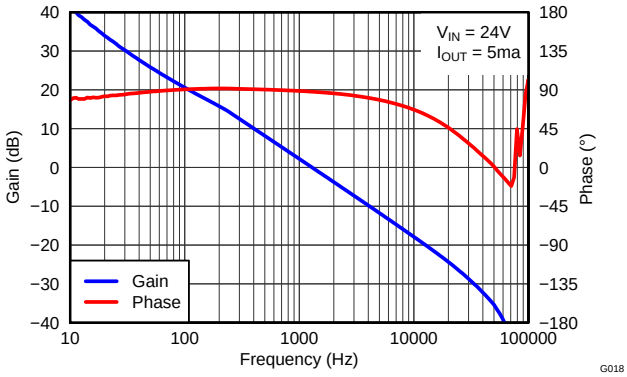


Figure 39. Gain vs Phase

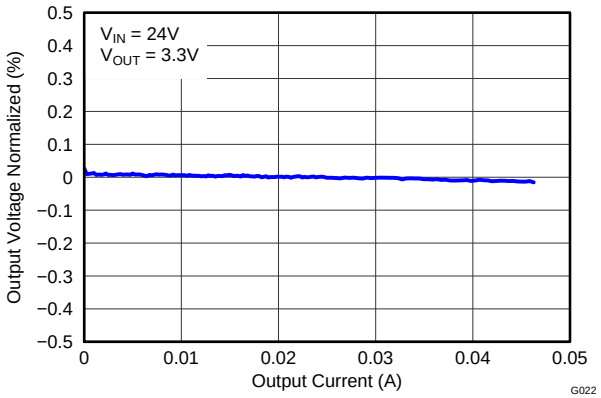


Figure 40. Output Voltage vs Output Current

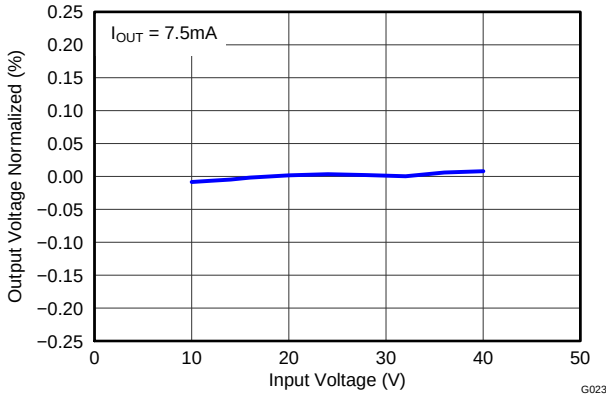


Figure 41. Output Voltage vs Input Voltage

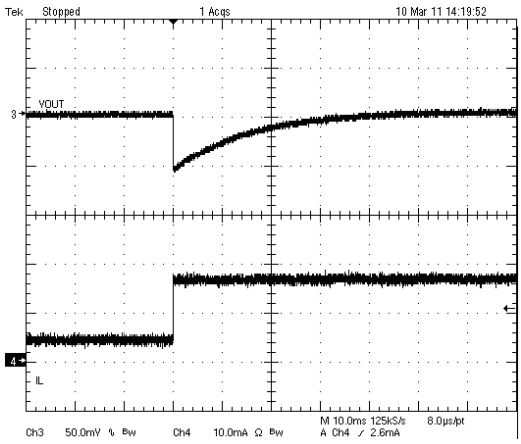


Figure 42. Load Transient

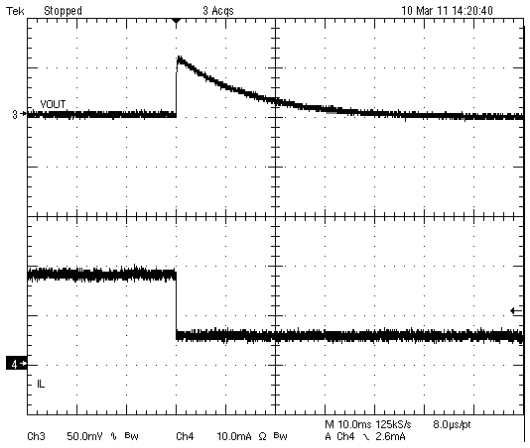


Figure 43. Unload Transient

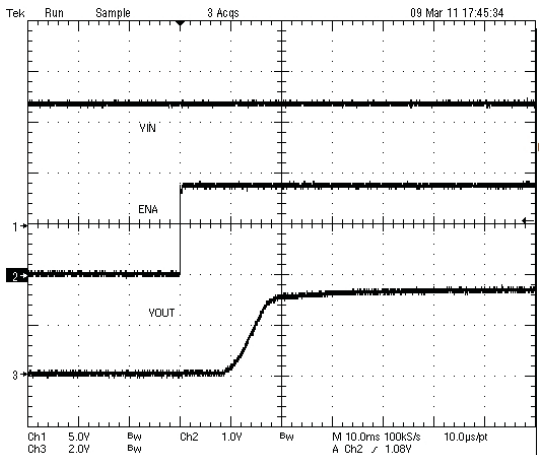


Figure 44. Startup With ENA

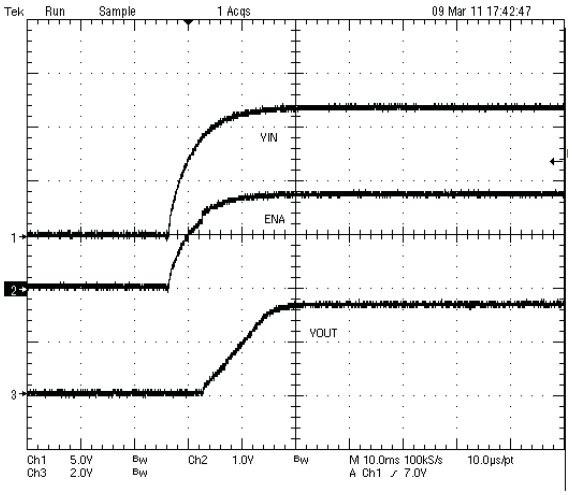


Figure 45. Startup With V_{IN}

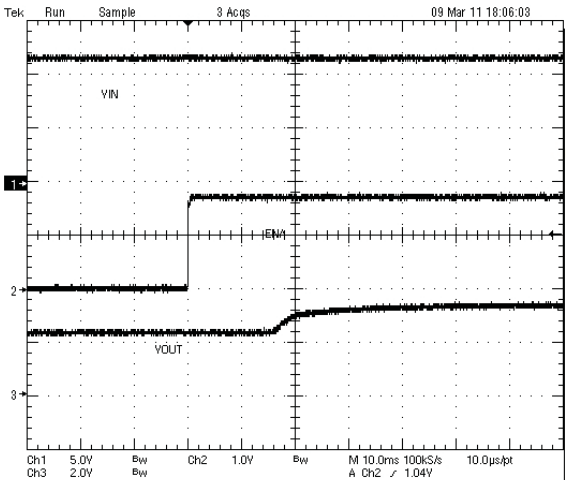


Figure 46. Prebias Startup With ENA

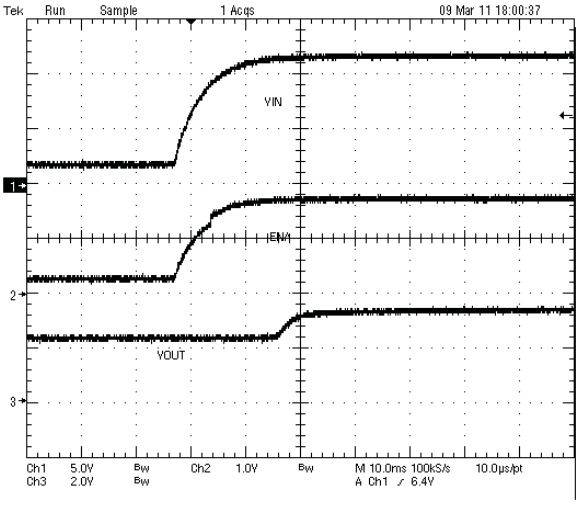


Figure 47. Prebias Startup With V_{IN}

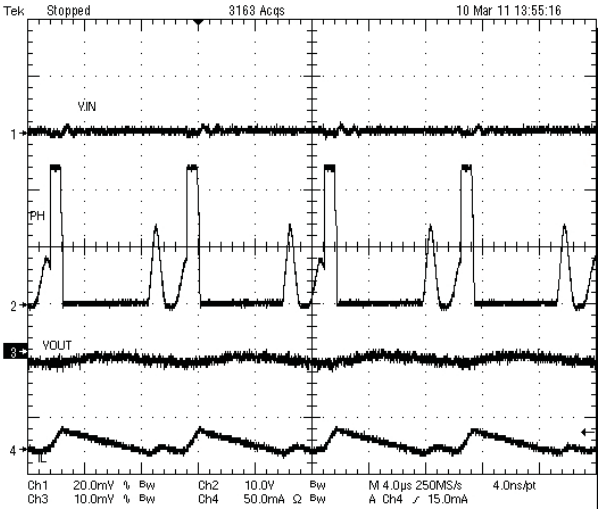


Figure 48. Input and Output Ripple in DCM

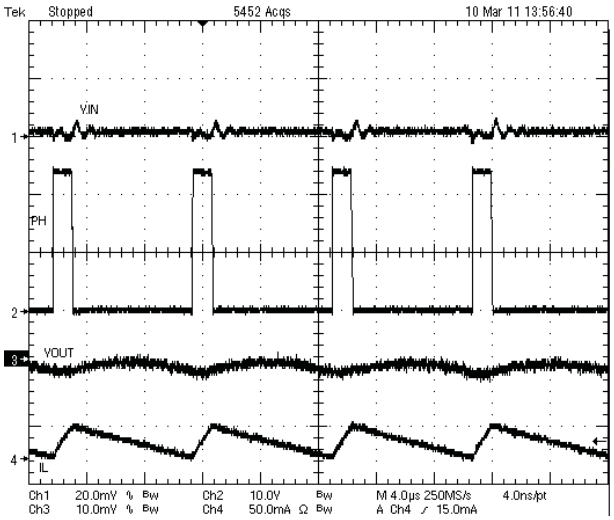


Figure 49. Input and Output Ripple in CCM

Layout

Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the GND pin. See Figure 50 for a PCB layout example. Since the PH connection is the switching node and output inductor should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The RT/CLK pin is sensitive to noise. so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts; however; this layout has been shown to produce good results and is meant as a guideline.

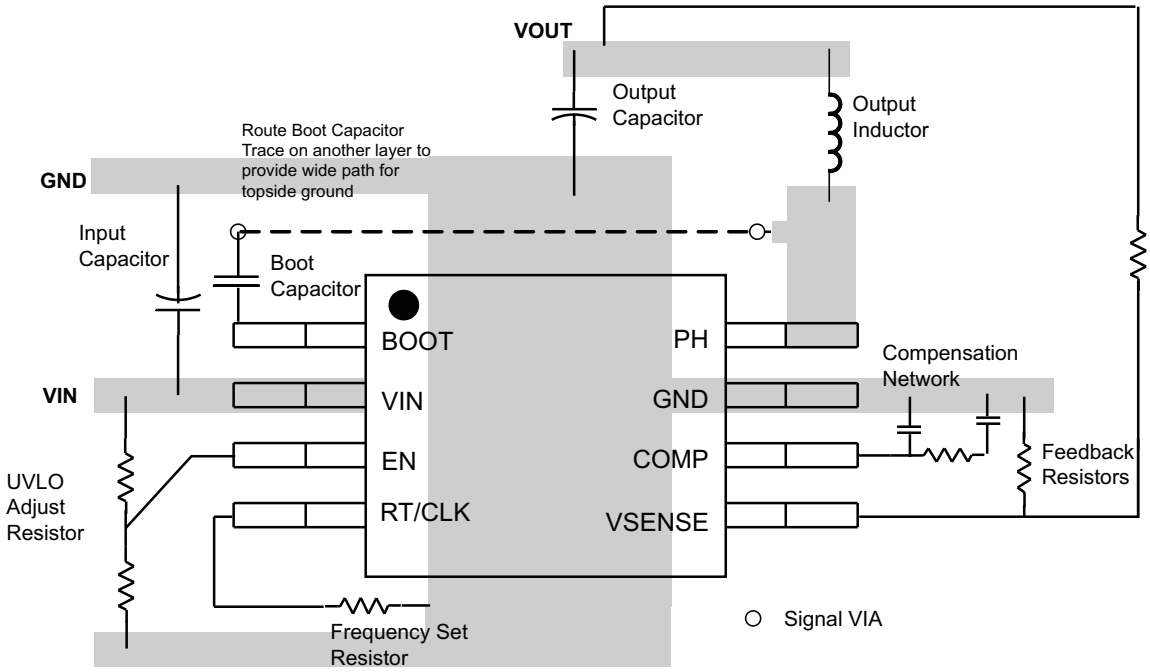


Figure 50. PCB Layout Example

REVISION HISTORY

Changes from Original (May 2011) to Revision A **Page**

- Changed Features Item From: MSOP8 and WSON8 Packages To: MSOP-8 and 3 mm x 3 mm VSON-8 Packages 1
- Changed the Efficiency Graph 1
- Added the ORDERING INFORMATION table 2
- Added the VSON (DRB-8 Pin) Package 2
- Added Thermal Pad information to the Pin Functions table 2
- Changed the RT/CLK pin Description 2
- Added VSON-8 Pins values to the Thermal Information table 4
- Changed the PLL lock in time Unit of Measure From: µA To: µs 5
- Changed Equation 22 18
- Changed the Efficiency vs Output Current Graphs, Figure 21 and Figure 22 19

Changes from Revision A (October 2011) to Revision B **Page**

- Added features Item: Diode Emulation for Improved Light Load Efficiency 1
- Changed Features Item From: 100 kHz to 400 kHz Switching Frequency To: 100 kHz to 400 kHz Adjustable Switching Frequency 1
- Changed the Efficiency Graph 1
- Changed VSON-8 package graphic to clarify ThermalPAD area 2
- Changed the EN pin MAX value From: 5 V To: 8 V 4
- Changed the Enable and Adjusting Undervoltage Lockout section 11
- Changed Equation 22 through Equation 25 18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS54062DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS54062DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS54062DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

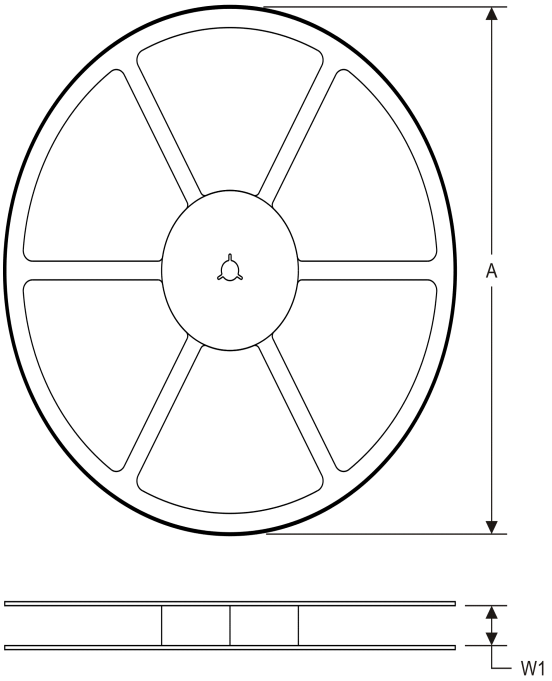
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

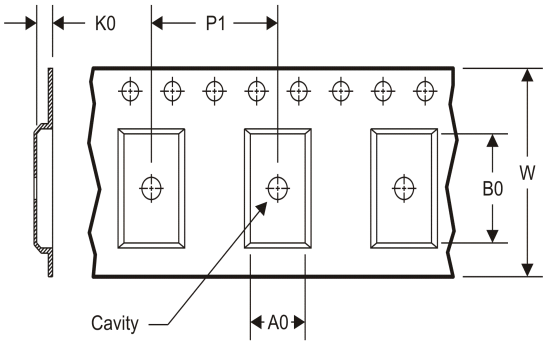
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



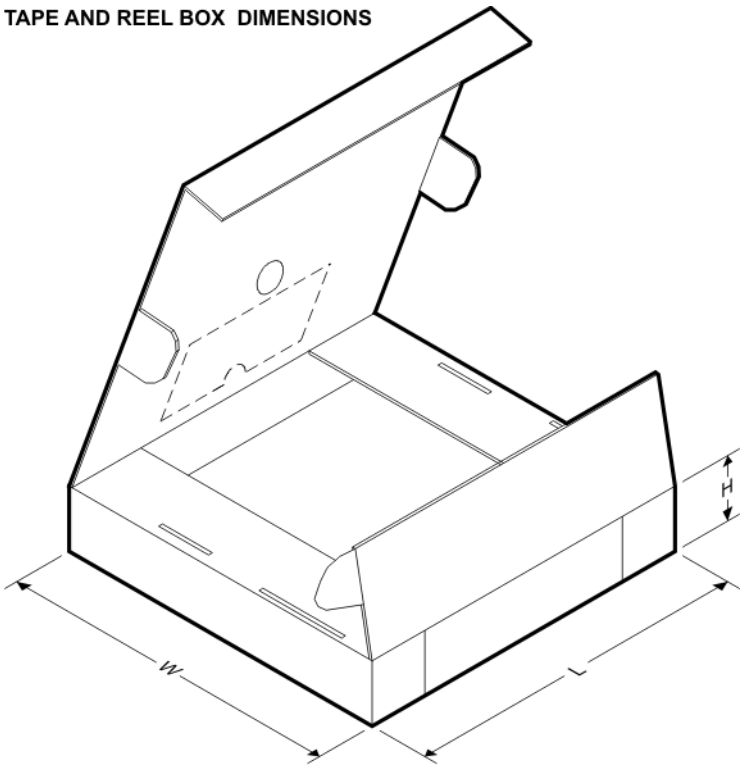
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54062DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS54062DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54062DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

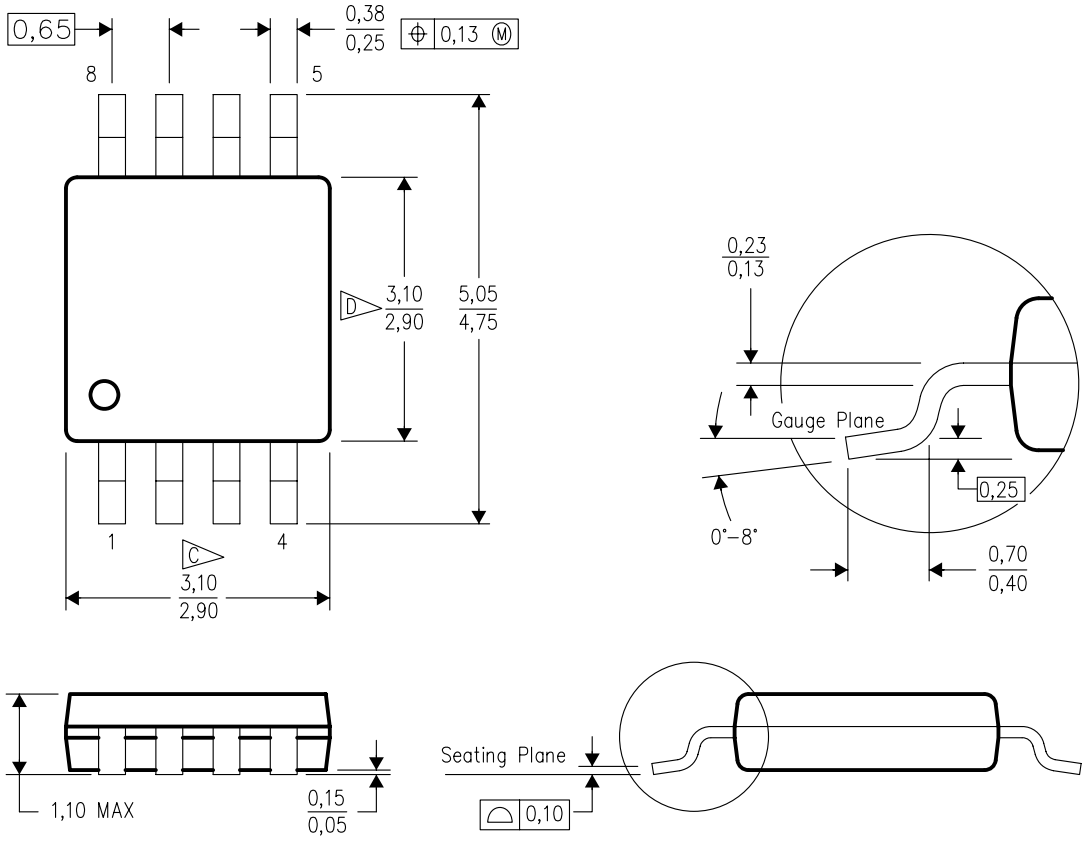
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54062DGKR	VSSOP	DGK	8	2500	370.0	355.0	55.0
TPS54062DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS54062DRBT	SON	DRB	8	250	210.0	185.0	35.0

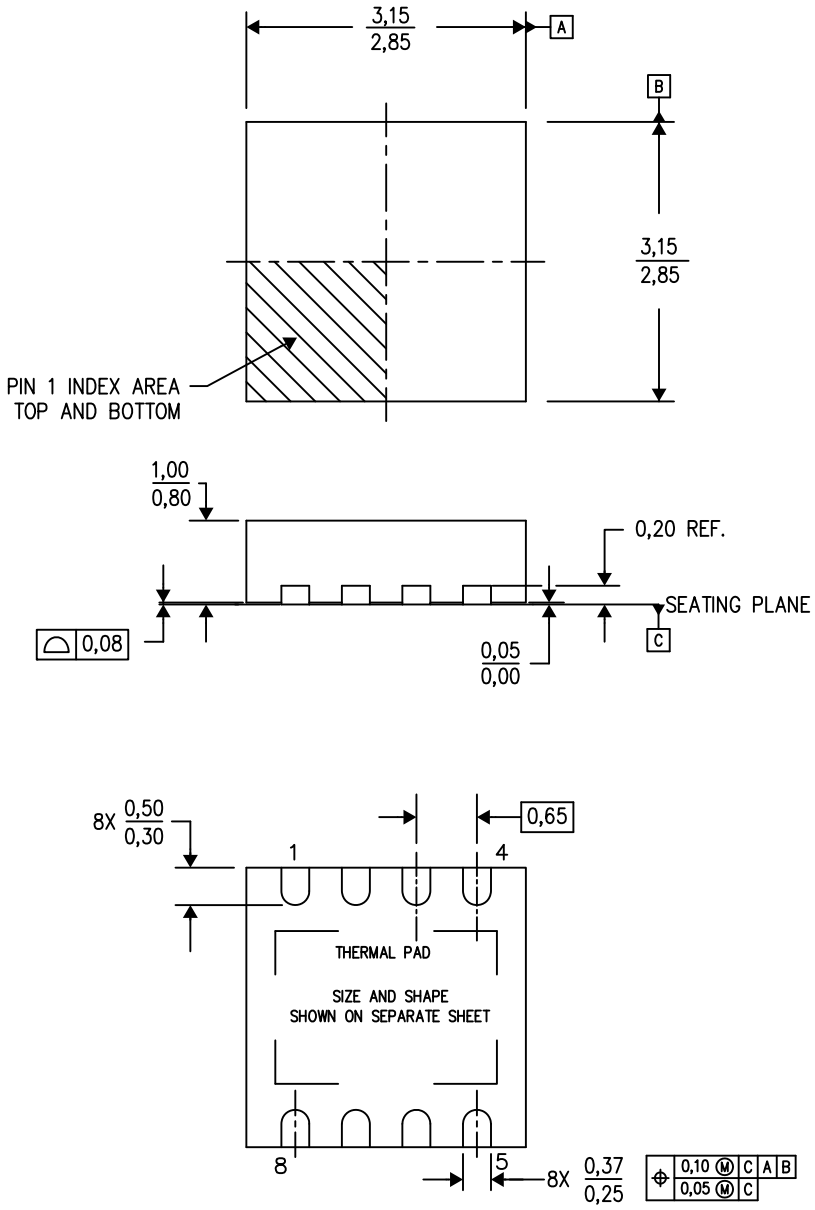
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4203482–2/K 06/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

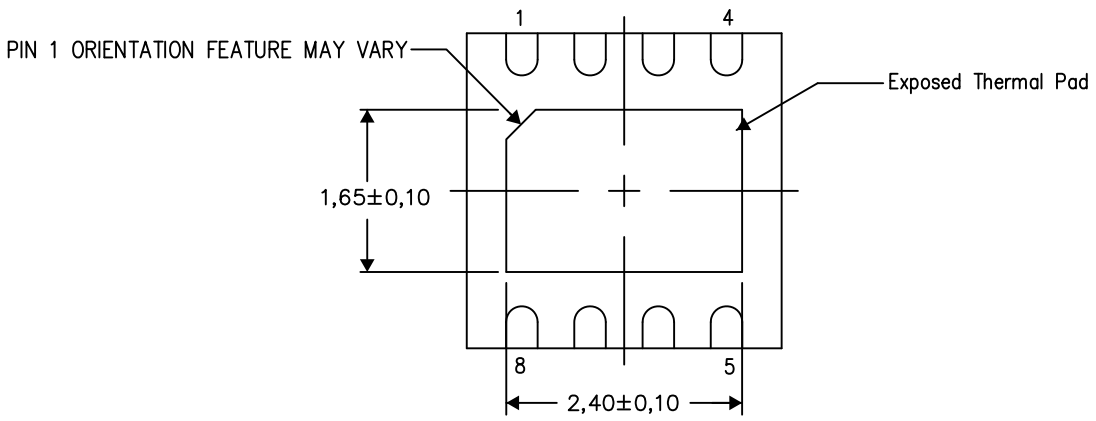
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



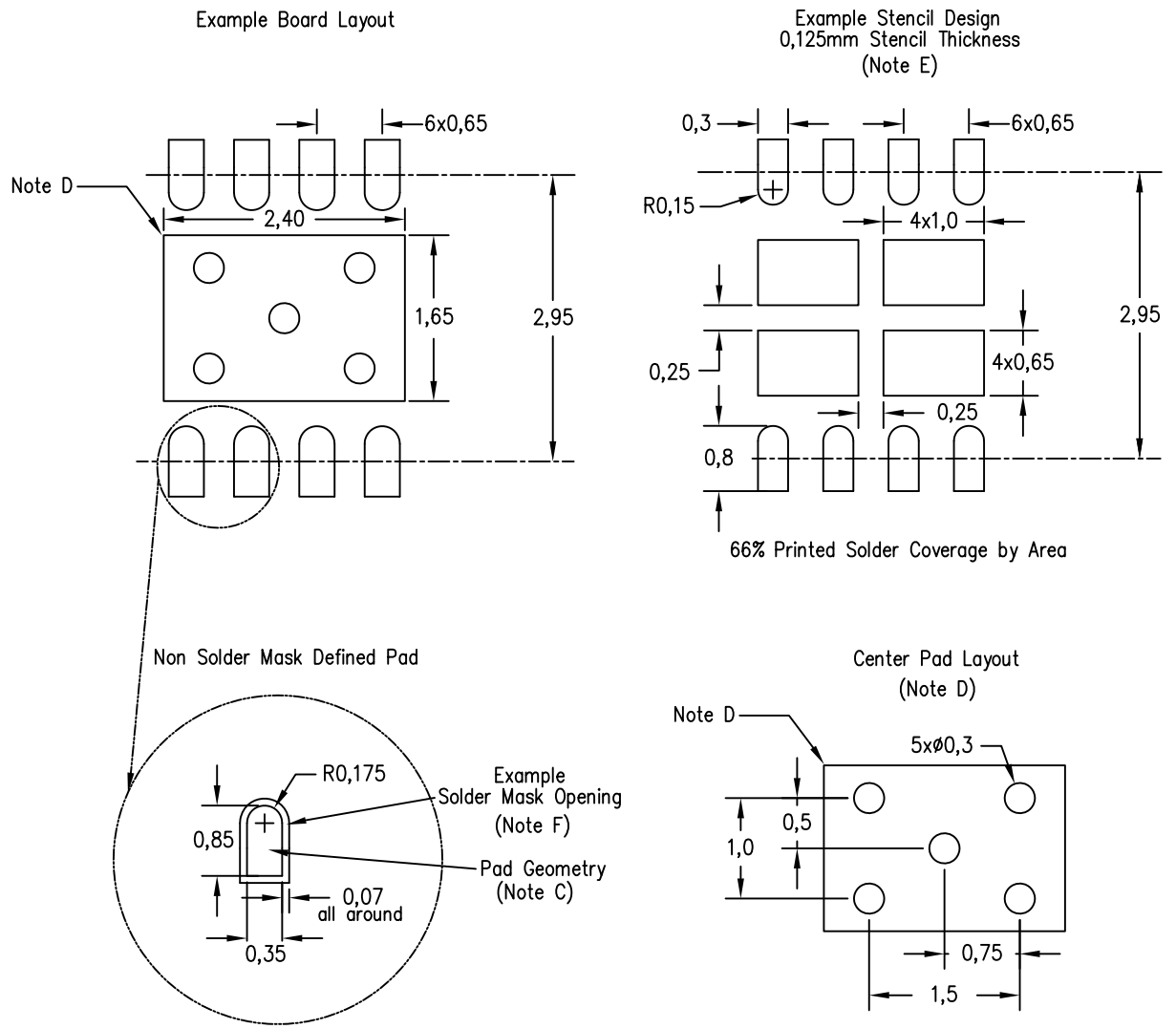
Bottom View

Exposed Thermal Pad Dimensions

4206340–3/M 06/12

NOTE: All linear dimensions are in millimeters

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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