SLUS669G – AUGUST 2005 – REVISED AUGUST 2008

VOLTAGE PROTECTION FOR 2-, 3-, OR 4-CELL Li-Ion BATTERIES (2nd-LEVEL PROTECTION)

Check for Samples: bq29410, bq29411, bq29412, bq29413, bq29414, bq29415, bq29419

FEATURES

- **2-, 3-, or 4-Cell Secondary Protection**
- **Low Power Consumption I_{CC} < 2 µA [$VCELL_{(ALL)}$ < $V_{(PROTECT)}$]**
- **Fixed High Accuracy Overvoltage Protection Threshold**
  - **bq29410 = 4.35 V**
  - **bq29411 = 4.40 V**
  - **bq29412 = 4.45 V**
  - **bq29413 = 4.50 V**
  - **bq29414 = 4.55 V**
  - **bq29415 = 4.60 V**
  - **bq29419 = 4.30 V**
- **Programmable Delay Time of Detection**
- **High Power Supply Ripple Rejection**
- **Stable During Pulse Charge Operation**

APPLICATIONS

- **2nd-Level Overvoltage Protection in Li-Ion Battery Packs in:**
  - **Notebook Computers**
  - **Portable Instrumentation**
  - **Portable Equipment**

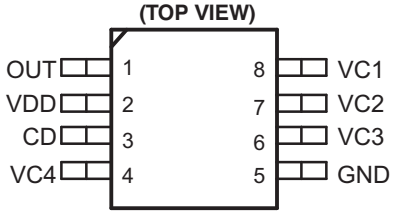
DESCRIPTION

The bq2941x is a secondary overvoltage protection IC for 2-, 3-, or 4-cell lithium-ion battery packs that incorporates a high-accuracy precision overvoltage detection circuit. It includes a programmable delay circuit for overvoltage detection time.

FUNCTION

Each cell in a multiple-cell pack is compared to an internal reference voltage. If one cell reaches an overvoltage condition, the protection sequence begins. The bq2941x device starts charging an external capacitor through the CD pin. When the CD pin voltage reaches 1.2 V, the OUT pin changes from a low level to a high level.

DCT PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	$V_{(PROTECT)}$ (2)	PACKAGE(3)			
		MSOP (DCT)	SYMBOL	SSOP (PW)	
–40°C to 110°C	4.30 V	bq29419DCTR	CJQ	bq29419PWG4	bq29419PWRG4
		bq29419DCTT			
	4.35 V	bq29410DCT3R	CJG	bq29410PW bq29410PWG4	bq29410PWR bq29410PWRG4
		bq29410DCTR			
		bq29410DCTT			
	4.40 V	bq29411DCT3R	CJH	bq29411PW bq29411PWG4	bq29411PWR bq29411PWRG4
		bq29411DCTR			
		bq29411DCTT			
	4.45 V	bq29412DCT3R	CJJ	bq29412PW bq29412PWG4	bq29412PWR bq29412PWRG4
		bq29412DCTR			
		bq29412DCTT			
	4.50 V	bq29413DCTR	CJk	bq29413PW	bq29413PWR
		bq29413DCTT			
	4.55 V	bq29414DCTR	CJL	bq29414PW	bq29414PWR
		bq29414DCTT			
	4.60 V	bq29415DCTR	CJM	bq29415PW	bq29415PWR
		bq29415DCTT			

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Contact your local Texas Instruments representative or sales office for alternative overvoltage threshold options.
(3) The "R" suffix indicates tape-and-reel packaging.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1) (2)

		UNIT
Supply voltage range	VDD	–0.3 V to 28 V
Input voltage range	VC1, VC2, VC3, VC4	–0.3 V to 28 V
	VC1 TO VC2, VC2 TO VC3, VC3 TO VC4, VC4 TO GND	–0.3 V to 8 V
Output voltage range	OUT	–0.3 V to 28 V
	CD	–0.3 V to 28 V
Continuous total power dissipation		See Dissipation Rating Table
Storage temperature range, T_{stg}		–65°C to 150°C
Lead temperature (soldering, 10 s)		300°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground of this device except the differential voltage of VC1-VC2, VC2-VC3, VC3-VC4, and VC4-GND.

PACKAGE DISSIPATION RATINGS

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DCT	412 mW	3.3 mW/°C	264 mW	214 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4		25	V
V_I	Input voltage range	VC1, VC2, VC3, VC4	0		25	V
		VCn – VC (n=1), (n=1, 2, 3), VC4 – GND	0		5	
$t_{d(CD)}$	Delay time capacitance			0.22		µF
R_{IN}	Voltage-monitor filter resistance		100	1k		Ω
C_{IN}	Voltage-monitor filter capacitance		0.01	0.1		µF
R_{VD}	Supply-voltage filter resistance		0		1	kΩ
C_{VD}	Supply-voltage filter capacitance			0.1		µF
T_A	Operating ambient temperature range		–40		110	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
$V_{(OA)}$	Overvoltage detection accuracy	T_A = 25°C		25	35	mV
		T_A = –20°C to 85°C		25	50	
		T_A = –40°C to 110°C			80	
$V_{(PROTECT)}$	Overvoltage detection voltage	bq29410		4.35		V
		bq29411		4.40		
		bq29412		4.45		
		bq29413		4.50		
		bq29414		4.55		
		bq29415		4.60		
		bq29419		4.30		
V_{hys}	Overvoltage detection hysteresis	bq29410/11/12/13/14/15		320		mV
		bq29419	250	320	450	
I_{IN}	Input current	V2, V3 , VC4 input ,V_{DD} = VC1 VC1 = VC2 = VC3 = VC4 = 3.5 V (see Figure 1)			0.3	µA
t_{D1}	Overvoltage detection delay time	V_{DD} = VC1, CD = 0.22 µF	1	1.5	2	S
$I_{(CD\_dis)}$	CD GND clamp current	V_{DD} = VC1, CD = 1 V	5	12		µA
I_{CC}	Supply current	V_{DD} = VC1, VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = 3.5 V (see Figure 1)		2	3	µA
		V_{DD} = VC1, VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = 2.3 V (see Figure 1)		1.5	2.5	
$V_{(OUT)}$	OUT pin drive voltage	VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = $V_{(PROTECT)}$Max, V_{DD} = 14 V, I_{OH} = 0 mA		7		V
		VC1 = VC2 = VC3 = VC4 = $V_{(PROTECT)}$Max, V_{DD} = 4.3 V, T_A = 0°C to 70°C, I_{OH} = 40 µA	1.5	2	2.5	
I_{OH}	High-level output current	OUT = 3 V, VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = $V_{(PROTECT)}$Max, V_{DD} = 14 V			–1	mA
I_{OL}	Low-level output current	OUT = 0.1 V, V_{DD} = VC1, VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = 3.5 V	5			µA

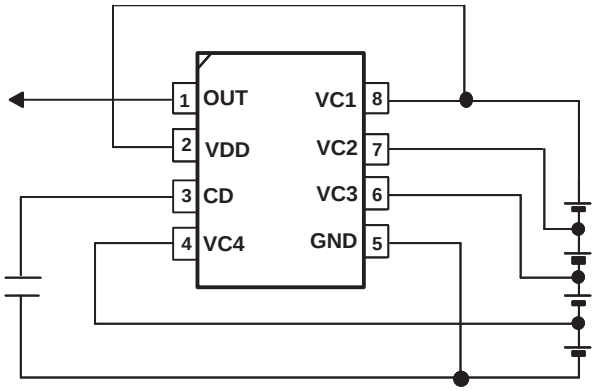
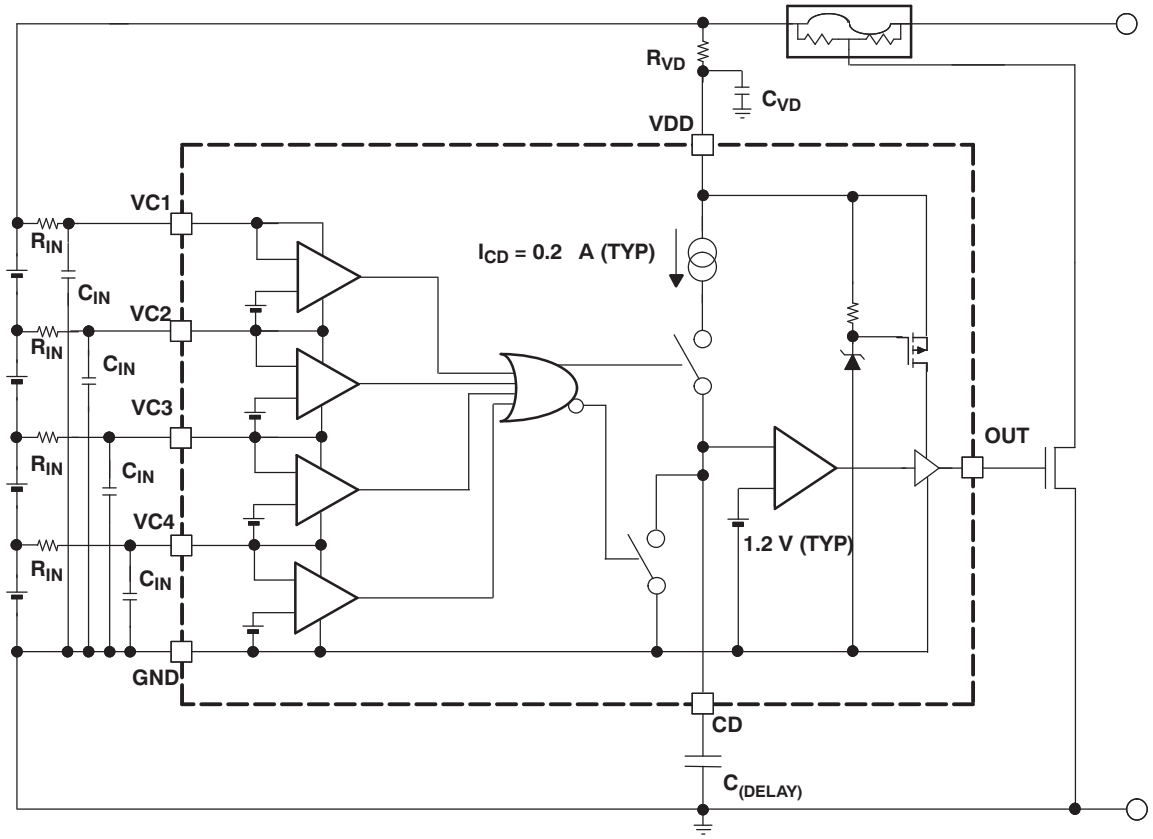


Figure 1. I_{CC}, I_{IN} Measurement (DCT Package)

Terminal Functions

TERMINAL			DESCRIPTION
MSOP (DCT)	TSSOP (PW)	NAME	
8	1	VC1	Sense voltage input for most positive cell
7	2	VC2	Sense voltage input for second most positive cell
6	3	VC3	Sense voltage input for third most positive cell
5	4	GND	Ground pin
4	5	VC4	Sense voltage input for least positive cell
3	6	CD	An external capacitor is connected to determine the programmable delay time
2	7	VDD	Power supply
1	8	OUT	Output

FUNCTIONAL BLOCK DIAGRAM



OVERVOLTAGE PROTECTION

When one of the cell voltages exceeds $V_{(PROTECT)}$, an internal current source begins to charge the capacitor, $C_{(DELAY)}$, connected to the CD pin. If the voltage at the CD pin, $V_{CD,}$ reaches 1.2 V, the OUT pin is activated and transitions high. An externally connected NCH FET is activiated and blows the external fuse in the positive battery rail; see the functional block diagram.

If all cell voltages fall below $V_{(PROTECT)}$ before the voltage at pin CD reaches 1.2 V, the delay time does not run out. An internal switch clamps the CD pin to GND and discharges the capacitor, $C_{(DELAY)}$, and secures the full delay time for the next occurring overvoltage event.

Once the pin OUT is activated, it transitions back from high to low after all battery cells reach $V_{(PROTECT)} - V_{hys.}$

DELAY TIME CALCULATION

The delay time is calculated as follows:

$$t_d = \frac{\left[1.2\ V \times C_{(DELAY)}\right]}{I_{CD}}$$

$$C_{(DELAY)} = \frac{\left[t_d \times I_{CD}\right]}{1.2\ V}$$

Where $I_{(CD)}$ = CD current source = 0.18 µA

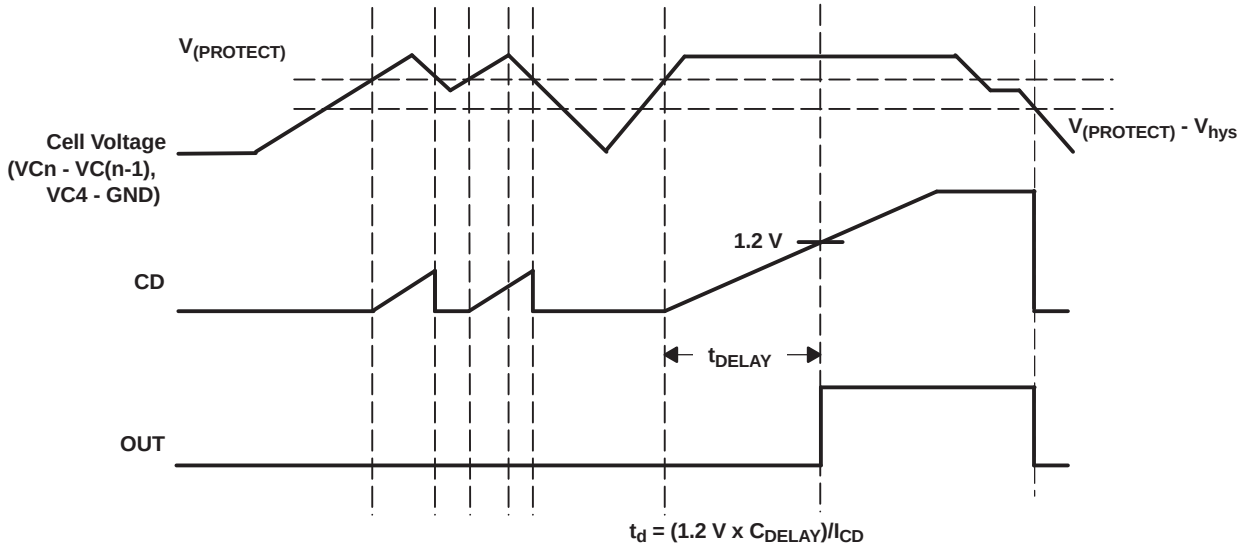


Figure 2. Timing for Overvoltage Sensing

APPLICATION INFORMATION

BATTERY CONNECTIONS

The following diagrams show the DCT package device in different cell configurations.

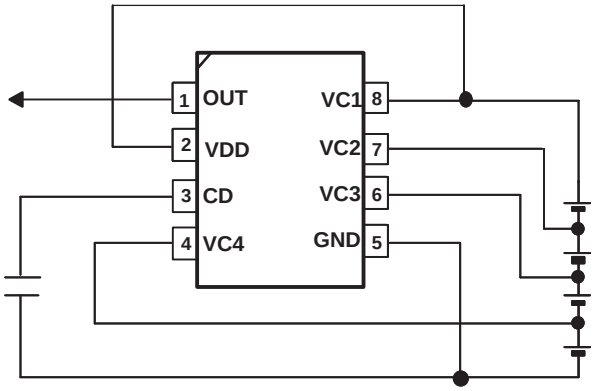


Figure 3. 4-Series Cell Configuration

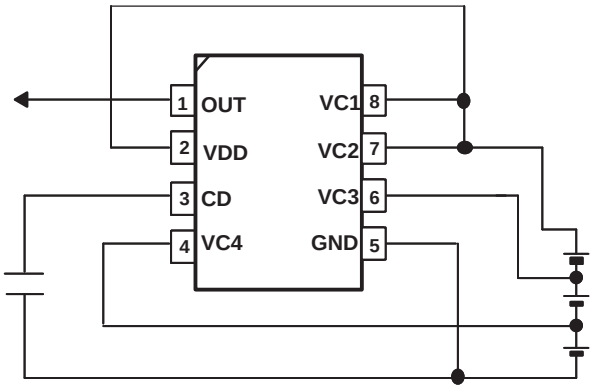


Figure 4. 3-Series Cell Configuration (Connect together VC1 and VC2)

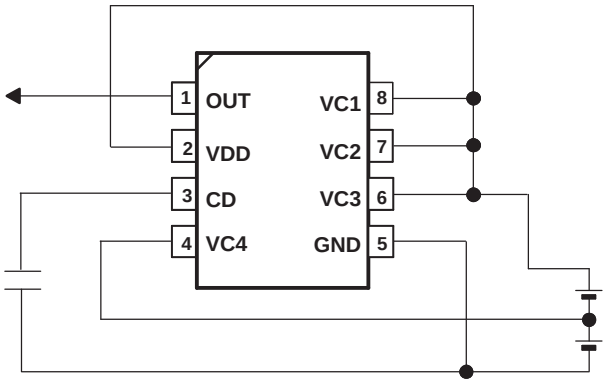


Figure 5. 2-Series Cell Configuration

CELL CONNECTIONS

To prevent incorrect output activation, the following connection sequences must be used.

4-Series Cell Configuration

- VC1(=VDD) → VC2 → VC3 → VC4 → GND or
- GND → VC4 → VC3 → VC2 → VC1(=VDD)

3-Series Cell Configuration

- VC1(=VC2=VDD) → VC3 → VC4 → GND or
- GND → VC4 → VC3 → VC1(=VC2=VDD)

2-Series Cell Configuration

- VC1(=VC2=VC3=VDD) → VC4 → GND or
- GND → VC4 → VC1(=VC2=VC3=VDD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ29410DCT3R	NRND	SM8	DCT	8	3000	Pb-Free (RoHS)	CU SNBI	Level-1-260C-UNLIM	-40 to 110	CJG W	
BQ29410DCT3RE6	NRND	SM8	DCT	8	3000	Pb-Free (RoHS)	CU SNBI	Level-1-260C-UNLIM	-40 to 110	CJG W	
BQ29410DCTR	NRND	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJG W	
BQ29410DCTRG4	NRND	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJG W	
BQ29410DCTT	NRND	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJG W	
BQ29410DCTTG4	NRND	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJG W	
BQ29410PW	NRND	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	29410	
BQ29410PWR	NRND	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	29410	
BQ29410PWRG4	NRND	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	29410	
BQ29411DCT3R	NRND	SM8	DCT	8	3000	Pb-Free (RoHS)	CU SNBI	Level-1-260C-UNLIM	-40 to 110	CJH W	
BQ29411DCTR	NRND	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJH W	
BQ29411DCTRG4	NRND	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJH W	
BQ29411DCTT	NRND	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJH W	
BQ29411PW	NRND	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	29411	
BQ29411PWR	NRND	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	29411	
BQ29411PWRG4	NRND	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	29411	
BQ29412DCT3R	NRND	SM8	DCT	8	3000	Pb-Free (RoHS)	CU SNBI	Level-1-260C-UNLIM	-40 to 110	CJJ W	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ29412DCT3RE6	NRND	SM8	DCT	8	3000	Pb-Free (RoHS)	CU SNBI	Level-1-260C-UNLIM	-40 to 110	CJJ W	
BQ29412DCTR	NRND	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJJ W	
BQ29412DCTRG4	NRND	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJJ W	
BQ29412DCTT	NRND	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJJ W	
BQ29412DCTTG4	NRND	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJJ W	
BQ29412PW	NRND	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	29412	
BQ29412PWG4	NRND	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	29412	
BQ29412PWR	NRND	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		29412	
BQ29412PWRG4	NRND	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		29412	
BQ29413DCTR	NRND	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJK W	
BQ29413DCTRG4	NRND	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJK W	
BQ29413DCTT	NRND	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJK W	
BQ29413PWR	NRND	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	29413	
BQ29414DCTR	NRND	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJL W	
BQ29414DCTRG4	NRND	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJL W	
BQ29414PW	NRND	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	2914	
BQ29414PWR	NRND	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	2914	
BQ29414PWRG4	NRND	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	2914	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ29415DCTR	NRND	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJM W	
BQ29415PWR	NRND	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	2915	
BQ29419PW	NRND	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	29419	
BQ29419PWG4	NRND	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	29419	
BQ29419PWR	NRND	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	29419	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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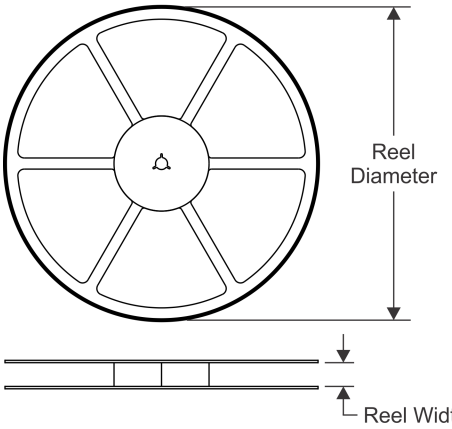
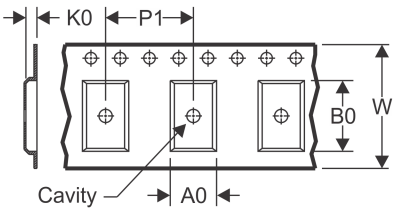
TAPE AND REEL INFORMATION

REEL DIMENSIONS

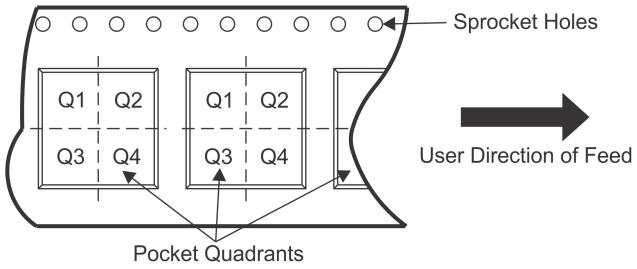


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

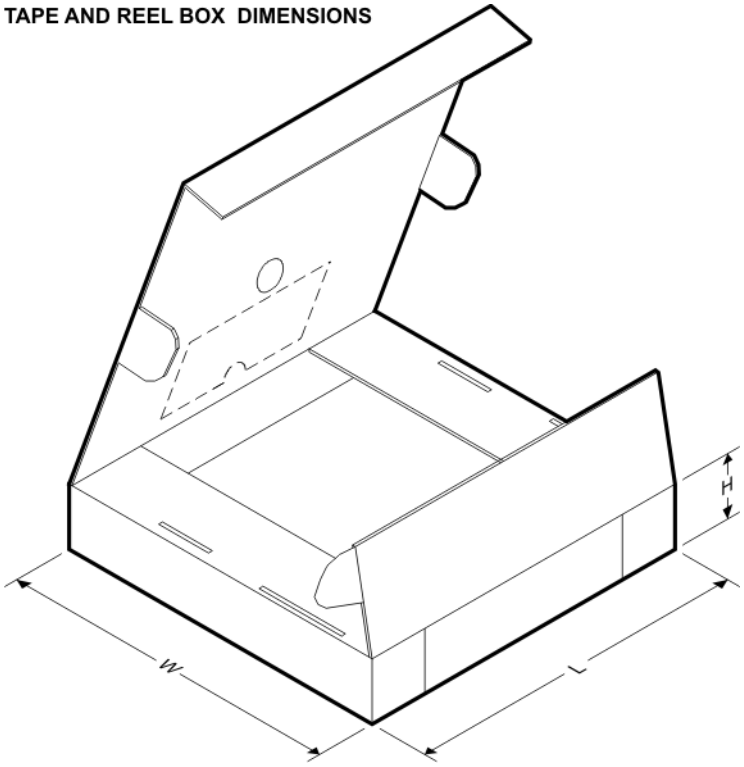
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29410DCT3R	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29410DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29410DCTT	SM8	DCT	8	250	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29410PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
BQ29410PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
BQ29411DCT3R	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29411DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29411DCTT	SM8	DCT	8	250	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29411PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
BQ29411PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
BQ29413DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29413DCTT	SM8	DCT	8	250	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29413PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
BQ29414DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29414PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
BQ29415DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29415PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
BQ29419PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29410DCT3R	SM8	DCT	8	3000	182.0	182.0	20.0
BQ29410DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
BQ29410DCTT	SM8	DCT	8	250	182.0	182.0	20.0
BQ29410PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
BQ29410PWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
BQ29411DCT3R	SM8	DCT	8	3000	182.0	182.0	20.0
BQ29411DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
BQ29411DCTT	SM8	DCT	8	250	182.0	182.0	20.0
BQ29411PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
BQ29411PWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
BQ29413DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
BQ29413DCTT	SM8	DCT	8	250	182.0	182.0	20.0
BQ29413PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
BQ29414DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
BQ29414PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
BQ29415DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
BQ29415PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
BQ29419PWR	TSSOP	PW	8	2000	367.0	367.0	35.0

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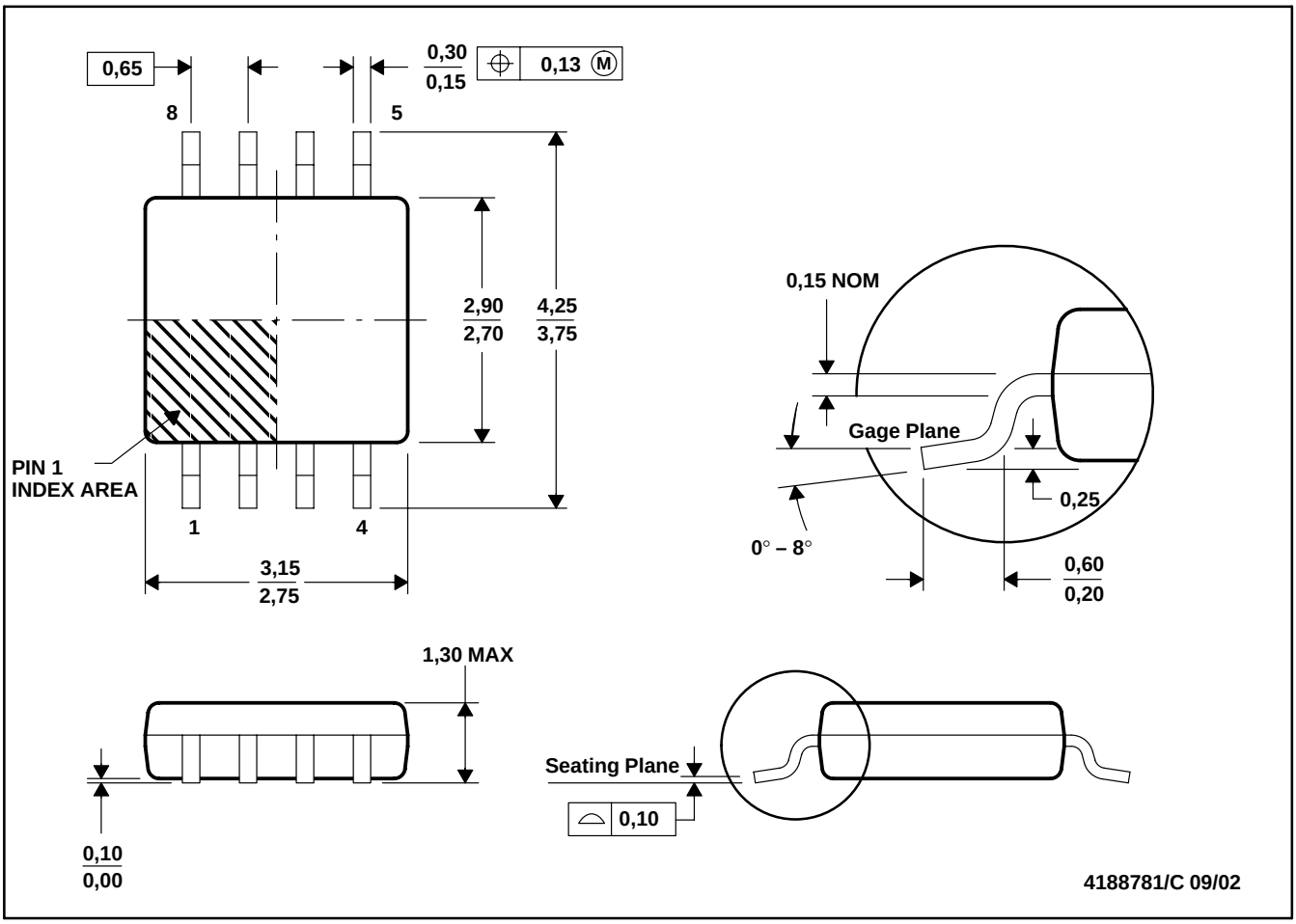
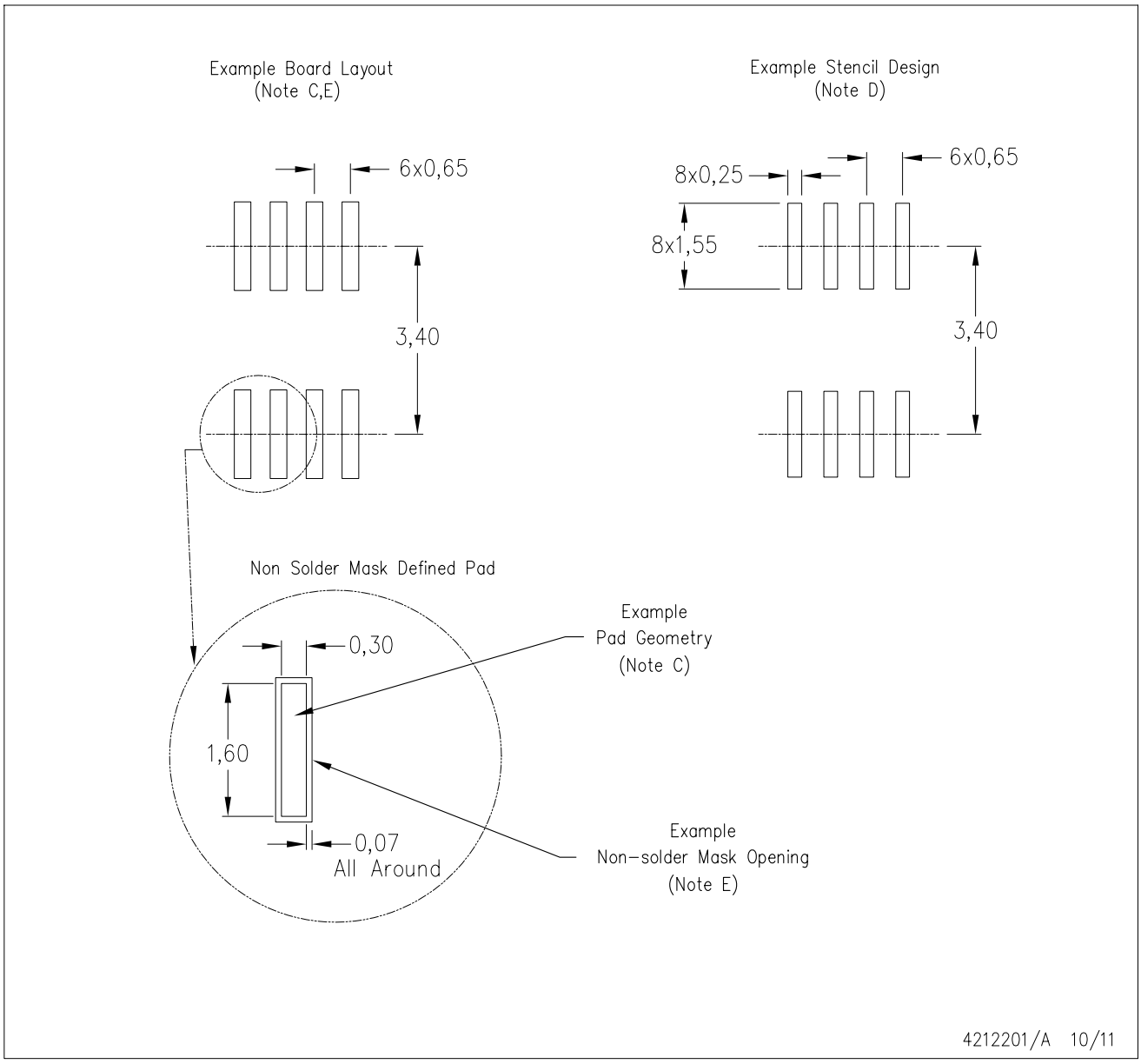
DCT (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. Falls within JEDEC MO-187 variation DA.

DCT (R–PDSO–G8) PLASTIC SMALL OUTLINE



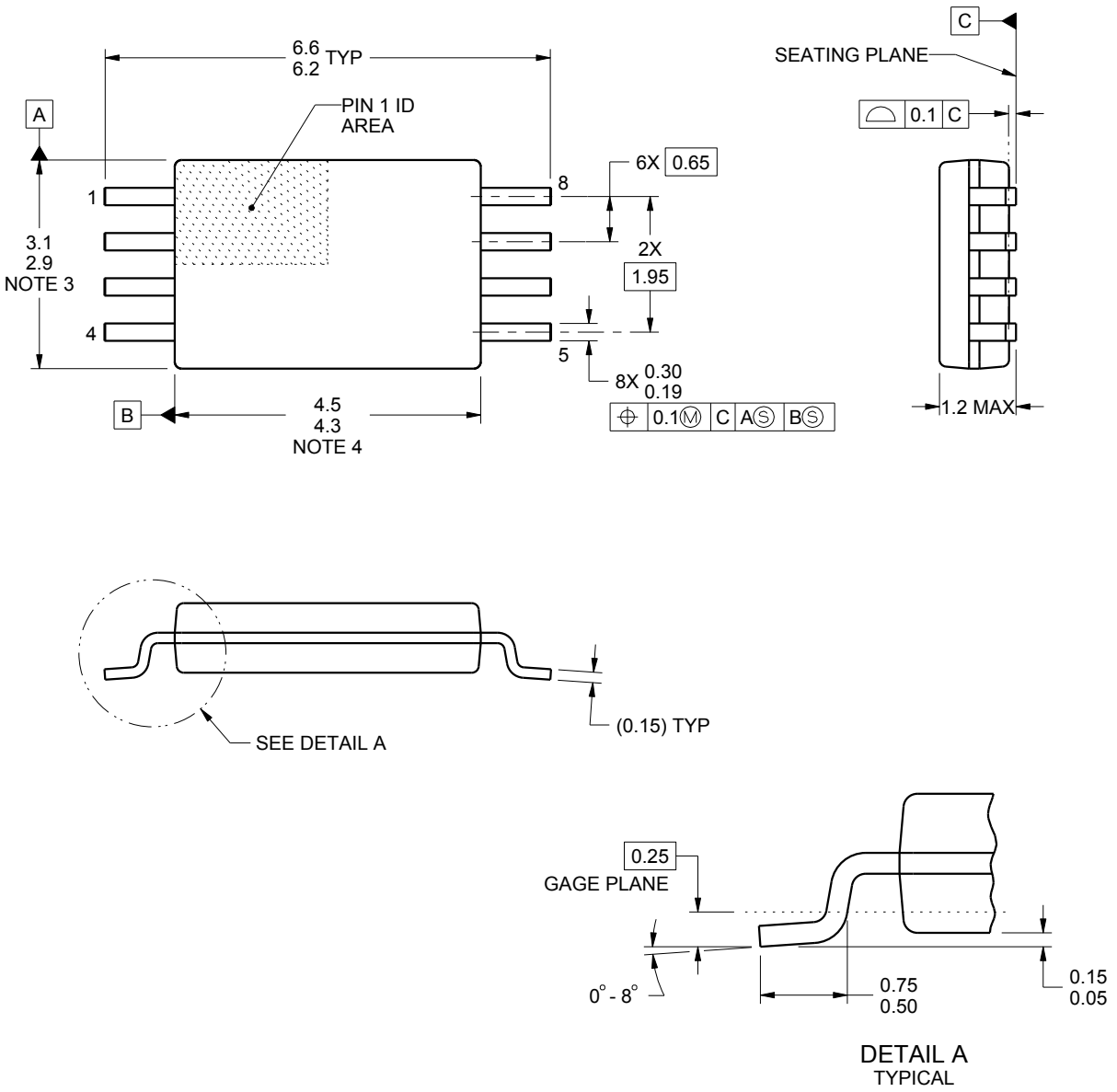
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0008A

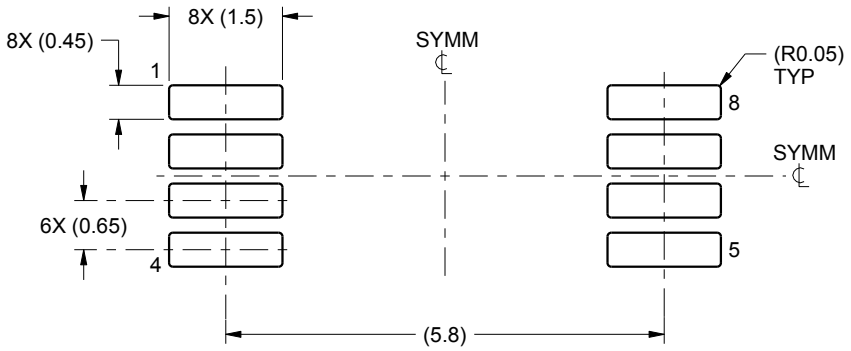
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

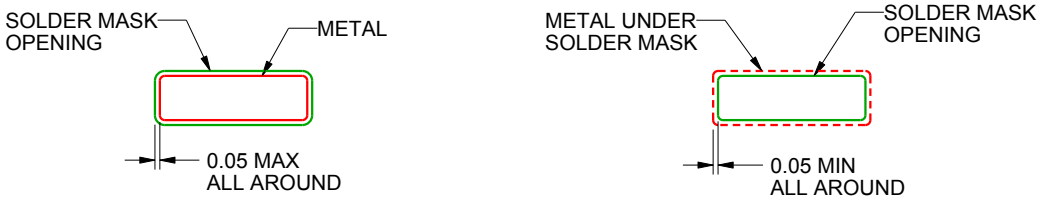


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

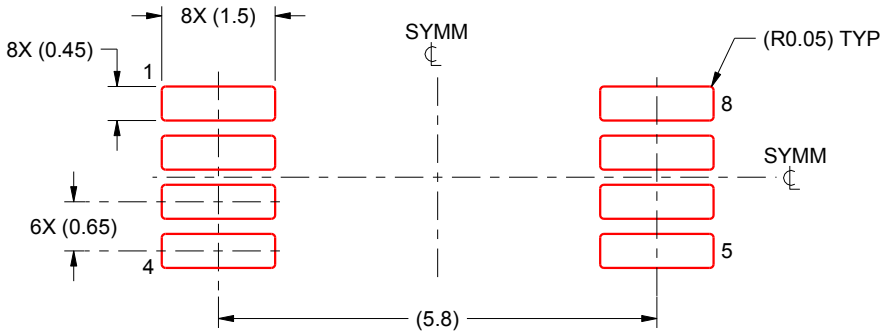


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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