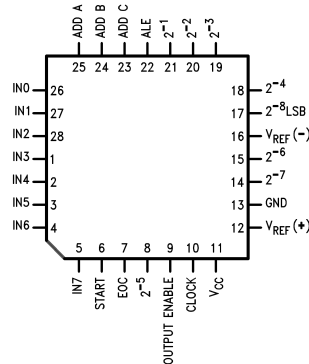


**Figure 1. PDIP Package**  
See Package N0028E



**Figure 2. PLCC Package**  
See Package FN0028A



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Absolute Maximum Ratings** <sup>(1)(2)(3)</sup>

Supply Voltage ( $V_{CC}$ ) <sup>(4)</sup>	6.5V		
Voltage at Any Pin Except Control Inputs	-0.3V to ( $V_{CC}+0.3V$ )		
Voltage at Control Inputs (START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	-0.3V to +15V		
Storage Temperature Range	-65°C to +150°C		
Package Dissipation at $T_A=25^\circ\text{C}$	875 mW		
Lead Temp. (Soldering, 10 seconds)	PDIP Package (plastic)	260°C	
	PLCC Package	Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C
ESD Susceptibility <sup>(5)</sup>	400V		

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
- (2) All voltages are measured with respect to GND, unless otherwise specified.
- (3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (4) A Zener diode exists, internally, from  $V_{CC}$  to GND and has a typical breakdown voltage of 7  $V_{DC}$ .
- (5) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

**Operating Conditions** <sup>(1)(2)</sup>

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$ -40°C $\leq T_A \leq$ +85°C
Range of $V_{CC}$	4.5 $V_{DC}$ to 6.0 $V_{DC}$

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
- (2) All voltages are measured with respect to GND, unless otherwise specified.

**Electrical Characteristics – Converter Specifications**

**Converter Specifications:**  $V_{CC}=5$   $V_{DC}=V_{REF+}$ ,  $V_{REF(-)}=GND$ ,  $T_{MIN} \leq T_A \leq T_{MAX}$  and  $f_{CLK}=640$  kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808	25°C			$\pm\frac{1}{2}$	LSB
	Total Unadjusted Error <sup>(1)</sup>	$T_{MIN}$ to $T_{MAX}$			$\pm\frac{3}{4}$	LSB

- (1) Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See Figure 5. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See Figure 15.

## Electrical Characteristics – Converter Specifications (continued)

**Converter Specifications:**  $V_{CC}=5$   $V_{DC}=V_{REF+}$ ,  $V_{REF(-)}=GND$ ,  $T_{MIN} \leq T_A \leq T_{MAX}$  and  $f_{CLK}=640$  kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0809 Total Unadjusted Error <sup>(1)</sup>	0°C to 70°C $T_{MIN}$ to $T_{MAX}$			$\pm 1$ $\pm 1\frac{1}{4}$	LSB LSB
	Input Resistance	From Ref(+) to Ref(-)	1.0	2.5		k $\Omega$
	Analog Input Voltage Range	See <sup>(2)</sup> V(+) or V(-)	GND - 0.1		$V_{CC} + 0.1$	$V_{DC}$
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		$V_{CC}$	$V_{CC} + 0.1$	V
$\frac{V_{REF(+)} + V_{REF(-)}}{2}$	Voltage, Center of Ladder		$(V_{CC}/2) - 0.1$	$V_{CC}/2$	$(V_{CC}/2) + 0.1$	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(-)	-0.1	0		V
$I_{IN}$	Comparator Input Current	$f_c=640$ kHz, <sup>(3)</sup>	-2	$\pm 0.5$	2	$\mu$ A

- (2) Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the  $V_{CCn}$  supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog  $V_{IN}$  does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute  $0V_{DC}$  to  $5V_{DC}$  input voltage range will therefore require a minimum supply voltage of  $4.900 V_{DC}$  over temperature variations, initial tolerance and loading.
- (3) Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence (Figure 8). See [ANALOG COMPARATOR INPUTS](#)

## Electrical Characteristics – Digital Levels and DC Specifications

**Digital Levels and DC Specifications:** ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV,  $4.75 \leq V_{CC} \leq 5.25V$ ,  $-40^\circ C \leq T_A \leq +85^\circ C$  unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>ANALOG MULTIPLEXER</b>						
$I_{OFF(+)}$	OFF Channel Leakage Current	$V_{CC}=5V$ , $V_{IN}=5V$ , $T_A=25^\circ C$ $T_{MIN}$ to $T_{MAX}$		10	200 1.0	nA $\mu$ A
$I_{OFF(-)}$	OFF Channel Leakage Current	$V_{CC}=5V$ , $V_{IN}=0$ , $T_A=25^\circ C$ $T_{MIN}$ to $T_{MAX}$	-200 -1.0	-10		nA $\mu$ A
<b>CONTROL INPUTS</b>						
$V_{IN(1)}$	Logical "1" Input Voltage		$(V_{CC} - 1.5)$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	$V_{IN}=15V$			1.0	$\mu$ A
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	$V_{IN}=0$	-1.0			$\mu$ A
$I_{CC}$	Supply Current	$f_{CLK}=640$ kHz		0.3	3.0	mA
<b>DATA OUTPUTS AND EOC (INTERRUPT)</b>						
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 4.75V$ $I_{OUT} = -360\mu A$ $I_{OUT} = -10\mu A$	2.4 4.5			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O=1.6$ mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	$I_O=1.2$ mA			0.45	V
$I_{OUT}$	TRI-STATE Output Current	$V_O=5V$ $V_O=0$			3	$\mu$ A $\mu$ A

## Electrical Characteristics – Timing Specifications

**Timing Specifications**  $V_{CC}=V_{REF(+)}=5V$ ,  $V_{REF(-)}=GND$ ,  $t_r=t_f=20$  ns and  $T_A=25^\circ C$  unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{STCLK}$	Start Time Delay from Clock	(Figure 7)	300		900	ns

## Electrical Characteristics – Timing Specifications (continued)

**Timing Specifications**  $V_{CC}=V_{REF(+)}=5V$ ,  $V_{REF(-)}=GND$ ,  $t_r=t_f=20$  ns and  $T_A=25^\circ C$  unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{WS}$	Minimum Start Pulse Width	(Figure 7)		100	200	ns
$t_{WALE}$	Minimum ALE Pulse Width	(Figure 7)		100	200	ns
$t_s$	Minimum Address Set-Up Time	(Figure 7)		25	50	ns
$t_H$	Minimum Address Hold Time	(Figure 7)		25	50	ns
$t_D$	Analog MUX Delay Time From ALE	$R_S=0\Omega$ (Figure 7)		1	2.5	$\mu s$
$t_{H1}, t_{H0}$	OE Control to Q Logic State	$C_L=50$ pF, $R_L=10k$ (Figure 10)		125	250	ns
$t_{1H}, t_{0H}$	OE Control to Hi-Z	$C_L=10$ pF, $R_L=10k$ (Figure 10)		125	250	ns
$t_c$	Conversion Time	$f_c=640$ kHz, (Figure 7) <sup>(1)</sup>	90	100	116	$\mu s$
$f_c$	Clock Frequency		10	640	1280	kHz
$t_{EOC}$	EOC Delay Time	(Figure 7)	0		$8 + 2 \mu s$	Clock Periods
$C_{IN}$	Input Capacitance	At Control Inputs		10	15	pF
$C_{OUT}$	TRI-STATE Output Capacitance	At TRI-STATE Outputs		10	15	pF

(1) The outputs of the data register are updated one clock cycle before the rising edge of EOC.

## Functional Description

### MULTIPLEXER

The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. [Table 1](#) shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

**Table 1. Analog Channel Selection**

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

### CONVERTER CHARACTERISTICS

#### The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach ([Figure 3](#)) was chosen over the conventional R/2R ladder because of its inherent monotonicity, which ensures no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in [Figure 3](#) are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached  $+\frac{1}{2}$  LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. [Figure 4](#) shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion start pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 6 shows a typical error curve for the ADC0808.

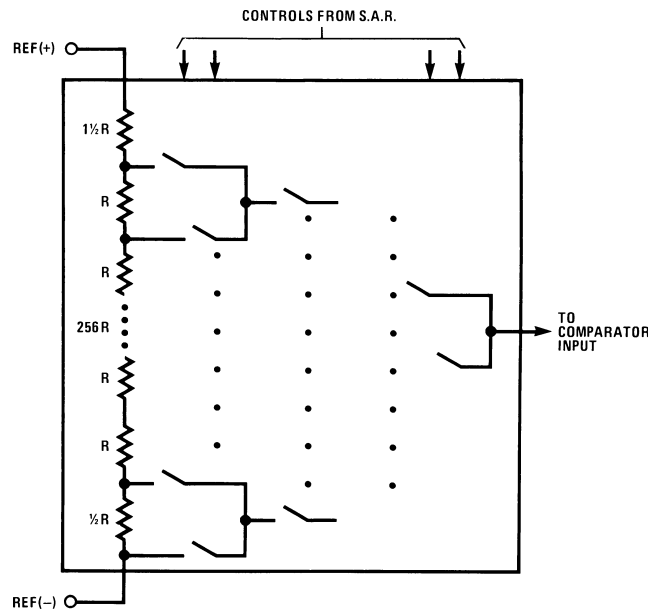


Figure 3. Resistor Ladder and Switch Tree

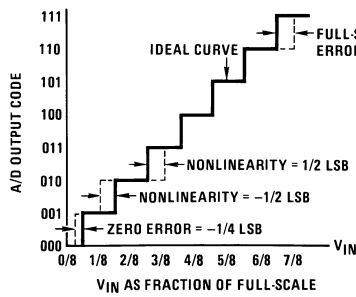


Figure 4. 3-Bit A/D Transfer Curve

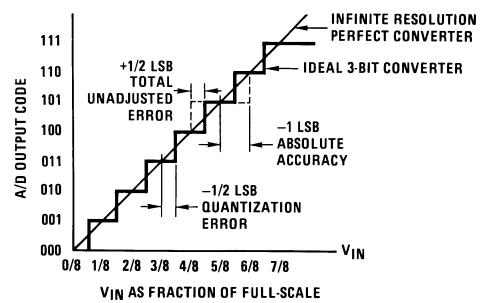


Figure 5. 3-Bit A/D Absolute Accuracy Curve

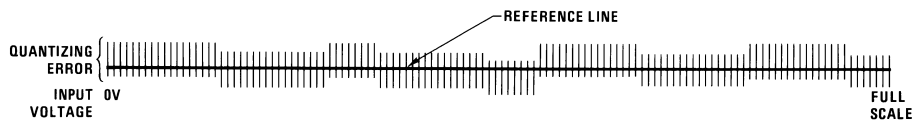


Figure 6. Typical Error Curve

Timing Diagram

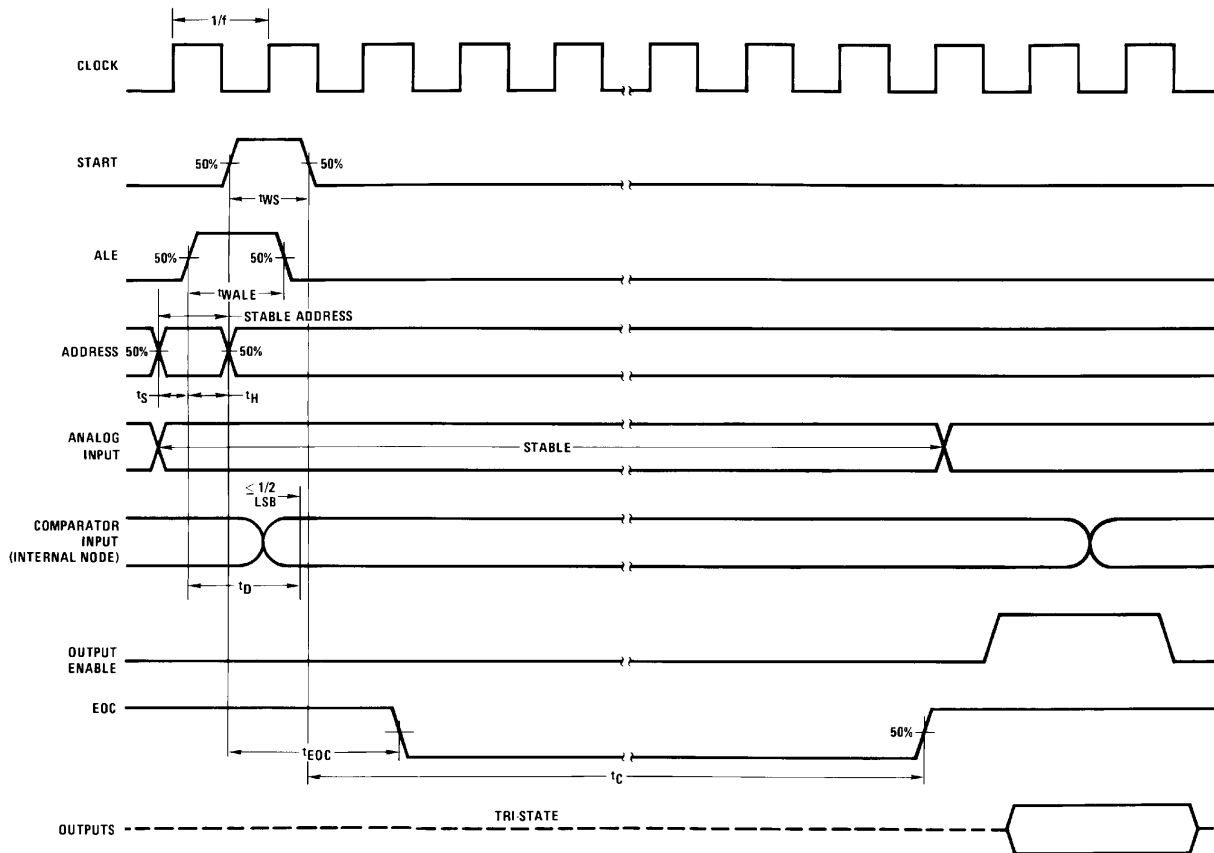
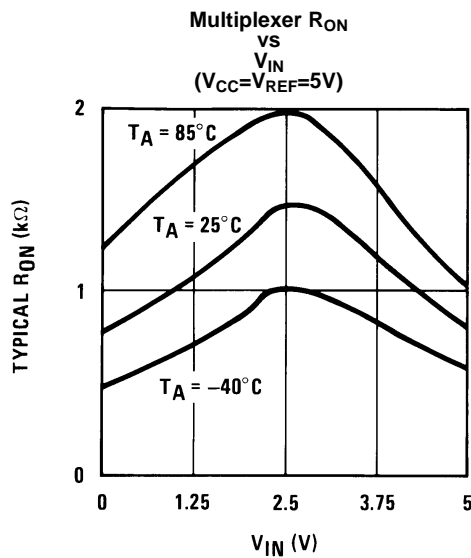
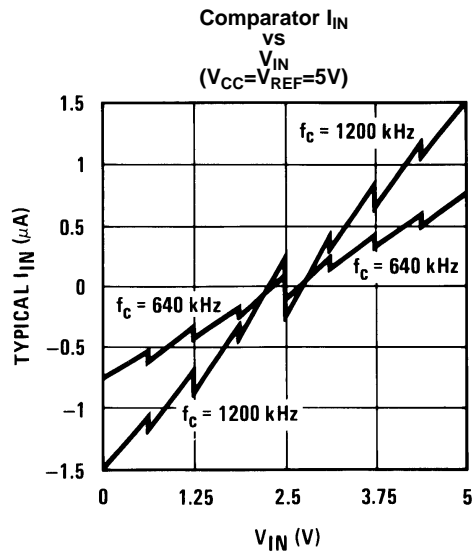


Figure 7.

Typical Performance Characteristics





TRI-STATE Test Circuits and Timing Diagrams

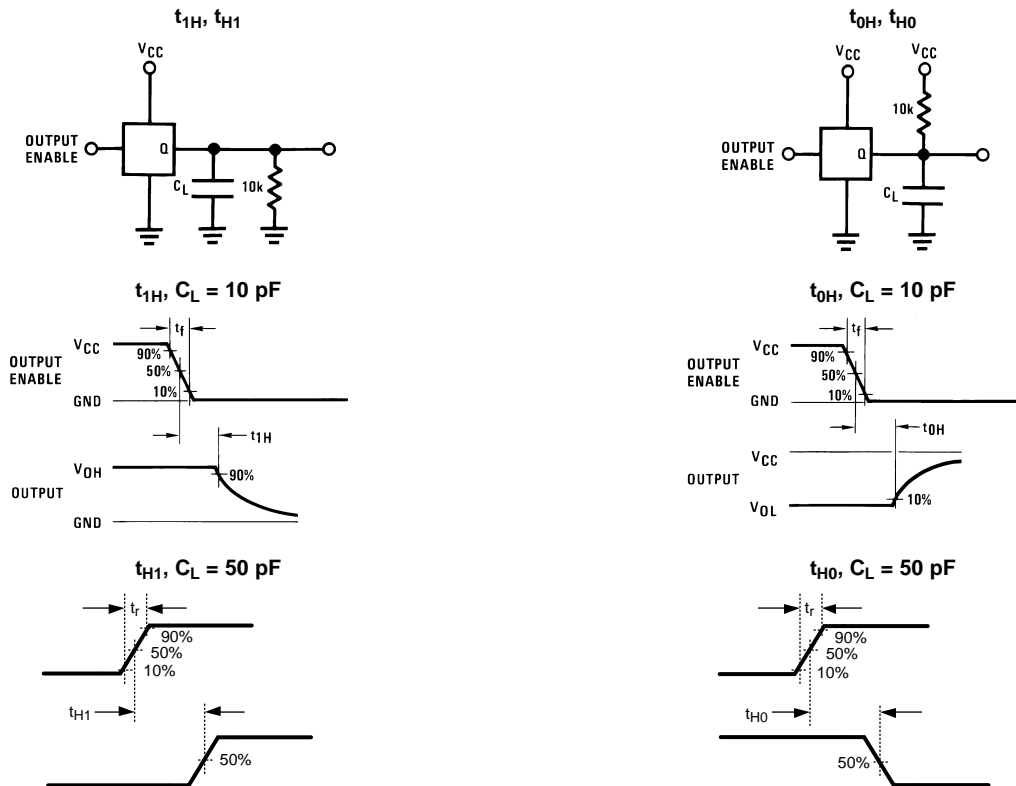


Figure 10. TRI-STATE Test Circuits and Timing Diagrams

## APPLICATIONS INFORMATION

### OPERATION

#### RATIOMETRIC CONVERSION

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs}-V_Z} = \frac{D_X}{D_{MAX}-D_{MIN}}$$

- $V_{IN}$ = Input voltage into the ADC0808
- $V_{fs}$ = Full-scale voltage
- $V_Z$ = Zero voltage
- $D_X$ = Data point being measured
- $D_{MAX}$ = Maximum data limit
- $D_{MIN}$ = Minimum data limit

(1)

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, (Figure 11).

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if  $V_{CC}=V_{REF}=5.12V$ , then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

#### RESISTOR LADDER LIMITATIONS

The voltages from the resistor ladder are compared to the selected into 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(-), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 12 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

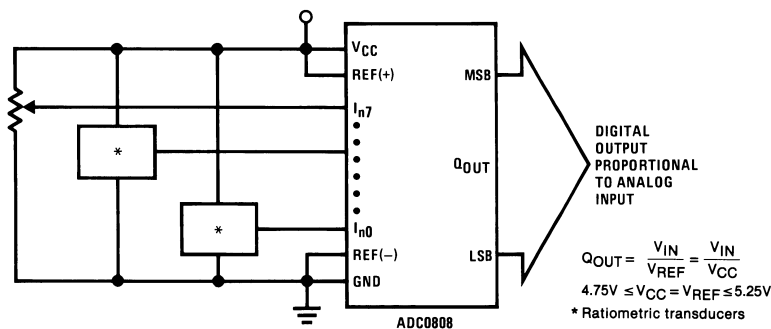
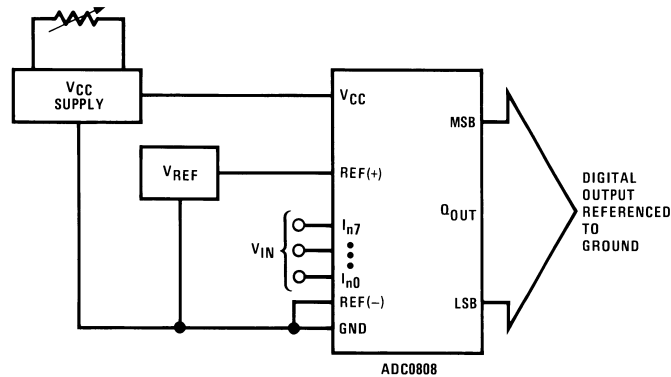


Figure 11. Ratiometric Conversion System

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In Figure 13 a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in Figure 14. The LM301 is overcompensated to insure stability when loaded by the 10  $\mu$ F output capacitor.

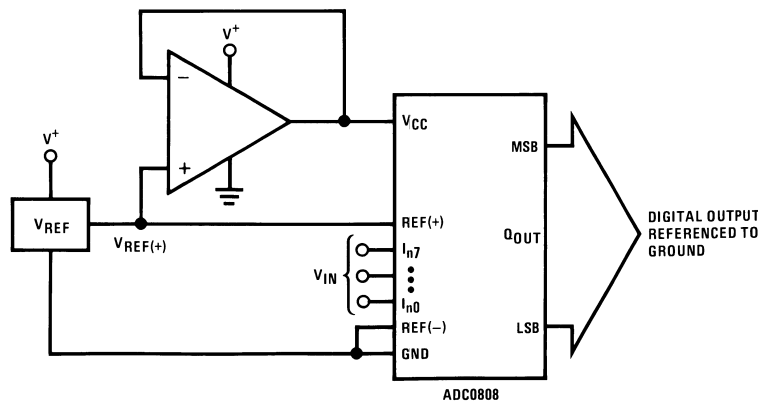
The top and bottom ladder voltages cannot exceed  $V_{CC}$  and ground, respectively, but they can be symmetrically less than  $V_{CC}$  and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In Figure 15, a 2.5V reference is symmetrically centered about  $V_{CC}/2$  since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.



$$Q_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$$

Figure 12. Ground Referenced Conversion System Using Trimmed Supply



$$Q_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$$

Figure 13. Ground Referenced Conversion System with Reference Generating  $V_{CC}$  Supply

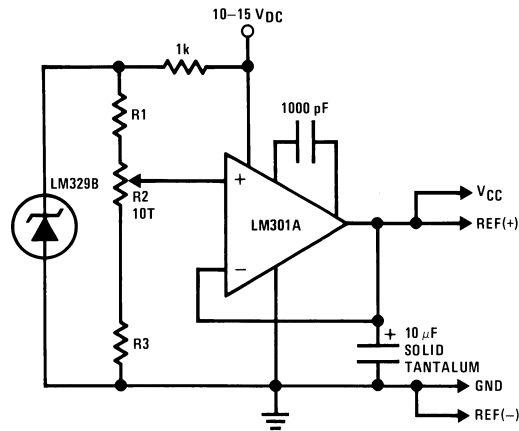
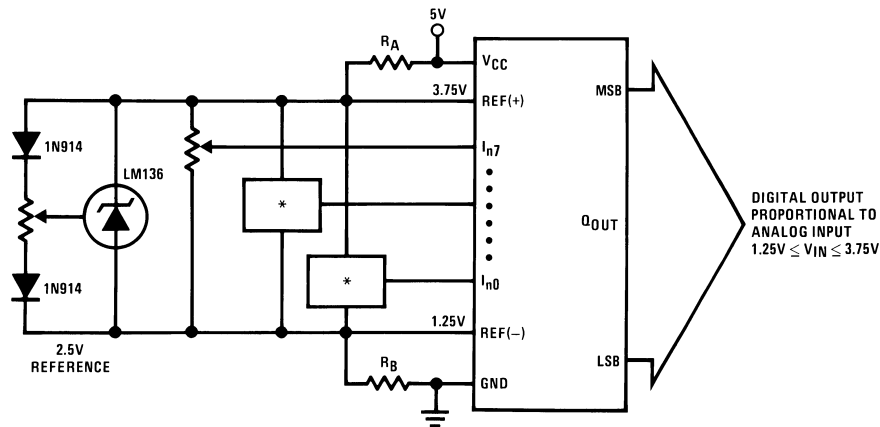


Figure 14. Typical Reference and Supply Circuit



$R_A = R_B$   
 \*Ratiometric transducers

Figure 15. Symmetrically Centered Reference

**CONVERTER EQUATIONS**

The transition between adjacent codes N and N+1 is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[ \frac{N}{256} + \frac{1}{512} \right] \pm V_{TUE} \right\} + V_{REF(-)} \tag{2}$$

The center of an output code N is given by:

$$V_{IN} \left\{ (V_{REF(+)} - V_{REF(-)}) \left[ \frac{N}{256} \right] \pm V_{TUE} \right\} + V_{REF(-)} \tag{3}$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy}$$

Where:

- $V_{IN}$  = Voltage at comparator input
- $V_{REF(+)}$  = Voltage at Ref(+)
- $V_{REF(-)}$  = Voltage at Ref(-)
- $V_{TUE}$  = Total unadjusted error voltage (typically
- $V_{REF(+)} \div 512$

(4)

### ANALOG COMPARATOR INPUTS

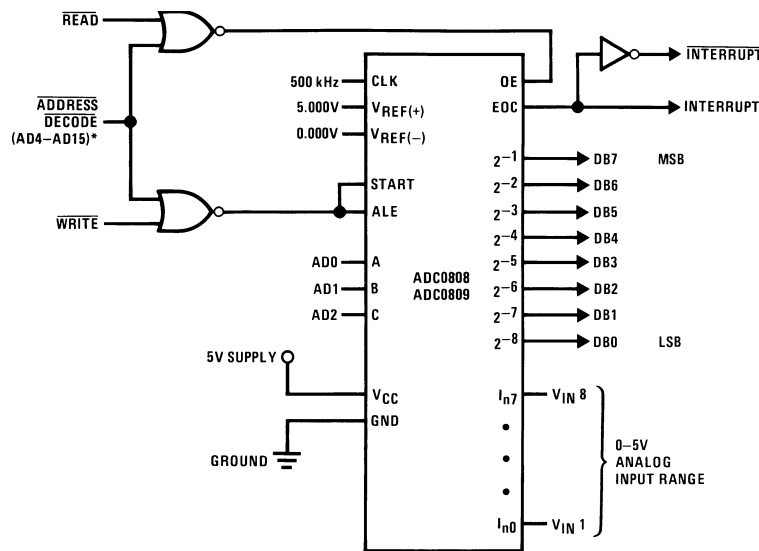
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with  $V_{IN}$  as shown in Figure 8.

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

### Typical Application



\*Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

Table 2. Microprocessor Interface Table

PROCESSOR	READ	WRITE	INTERRUPT (COMMENT)
8080	$\overline{MEMR}$	$\overline{MEMW}$	INTR (Thru RST Circuit)
8085	$\overline{RD}$	$\overline{WR}$	INTR (Thru RST Circuit)
Z-80	$\overline{RD}$	$\overline{WR}$	$\overline{INT}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	$VMA \cdot \phi 2 \cdot R/W$	$VMA \cdot \phi \cdot R/W$	$\overline{IRQA}$ or $\overline{IRQB}$ (Thru PIA)

## REVISION HISTORY

### Changes from Revision G (March 2013) to Revision H

Page

- 
- Changed layout of National Data Sheet to TI format ..... [13](#)
-

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC0808CCN	NRND	PDIP	N	28	13	TBD	Call TI	Call TI	-40 to 85	ADC0808CCN	
ADC0808CCN/NOPB	ACTIVE	PDIP	N	28	13	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	ADC0808CCN	<b>Samples</b>
ADC0808CCV	NRND	PLCC	FN	28	35	TBD	Call TI	Call TI	-40 to 85	ADC0808CCV	
ADC0808CCV/NOPB	ACTIVE	PLCC	FN	28	35	Green (RoHS & no Sb/Br)	CU SN	Level-2A-245C-4 WEEK	-40 to 85	ADC0808CCV	<b>Samples</b>
ADC0808CCVX	NRND	PLCC	FN	28	750	TBD	Call TI	Call TI	-40 to 85	ADC0808CCV	
ADC0808CCVX/NOPB	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU SN	Level-2A-245C-4 WEEK	-40 to 85	ADC0808CCV	<b>Samples</b>
ADC0809CCN	NRND	PDIP	N	28	13	TBD	Call TI	Call TI	-40 to 85	ADC0809CCN	
ADC0809CCN/NOPB	ACTIVE	PDIP	N	28	13	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	ADC0809CCN	<b>Samples</b>
ADC0809CCV	NRND	PLCC	FN	28	35	TBD	Call TI	Call TI	-40 to 85	ADC0809CCV	
ADC0809CCV/NOPB	ACTIVE	PLCC	FN	28	35	Green (RoHS & no Sb/Br)	CU SN	Level-2A-245C-4 WEEK	-40 to 85	ADC0809CCV	<b>Samples</b>
ADC0809CCVX	NRND	PLCC	FN	28	750	TBD	Call TI	Call TI	-40 to 85	ADC0809CCV	
ADC0809CCVX/NOPB	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU SN	Level-2A-245C-4 WEEK	-40 to 85	ADC0809CCV	<b>Samples</b>
MM74C949N	NRND	PDIP	N	28	13	TBD	Call TI	Call TI	-40 to 85	ADC0808CCN	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

---

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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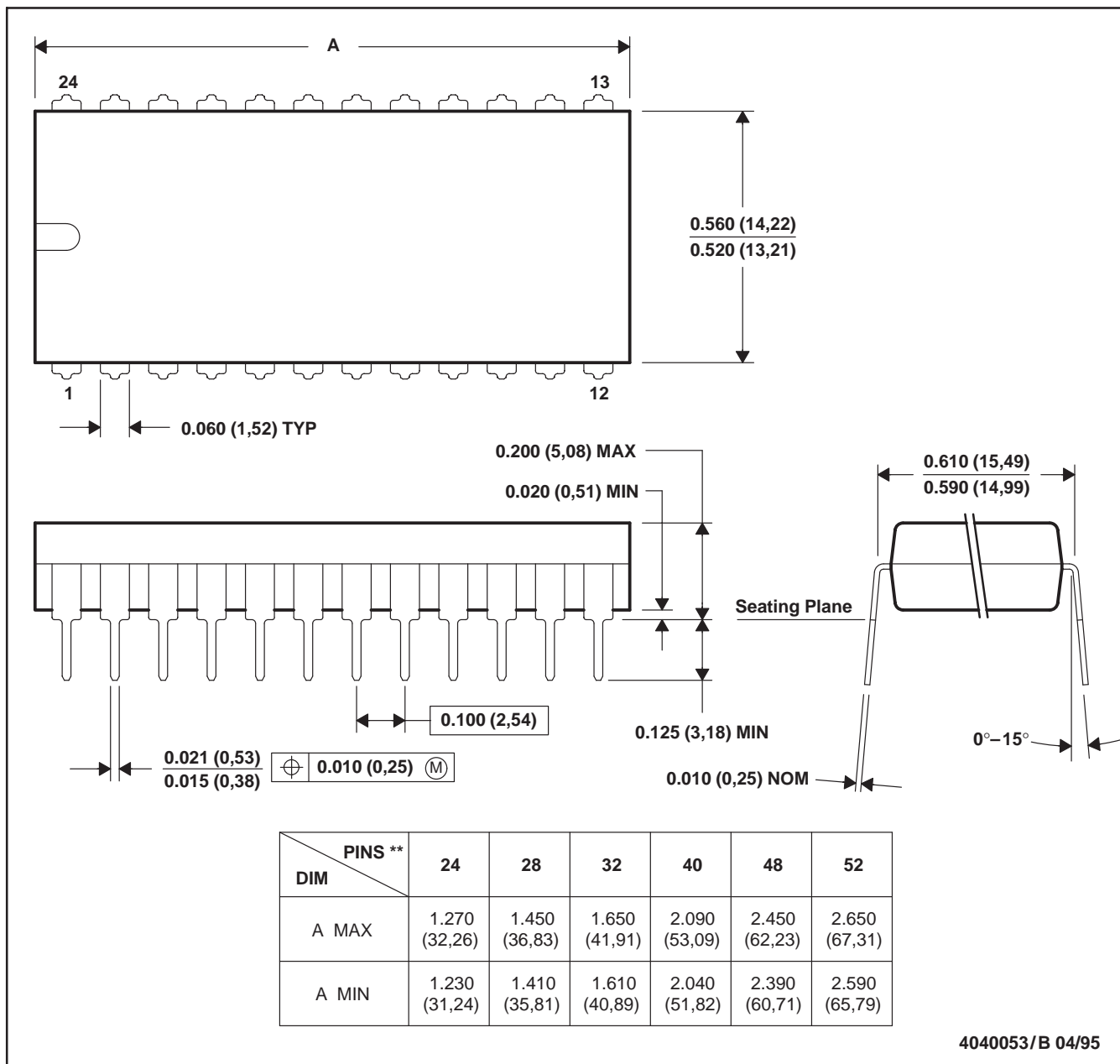
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**N (R-PDIP-T\*\*)**

**PLASTIC DUAL-IN-LINE PACKAGE**

24 PIN SHOWN

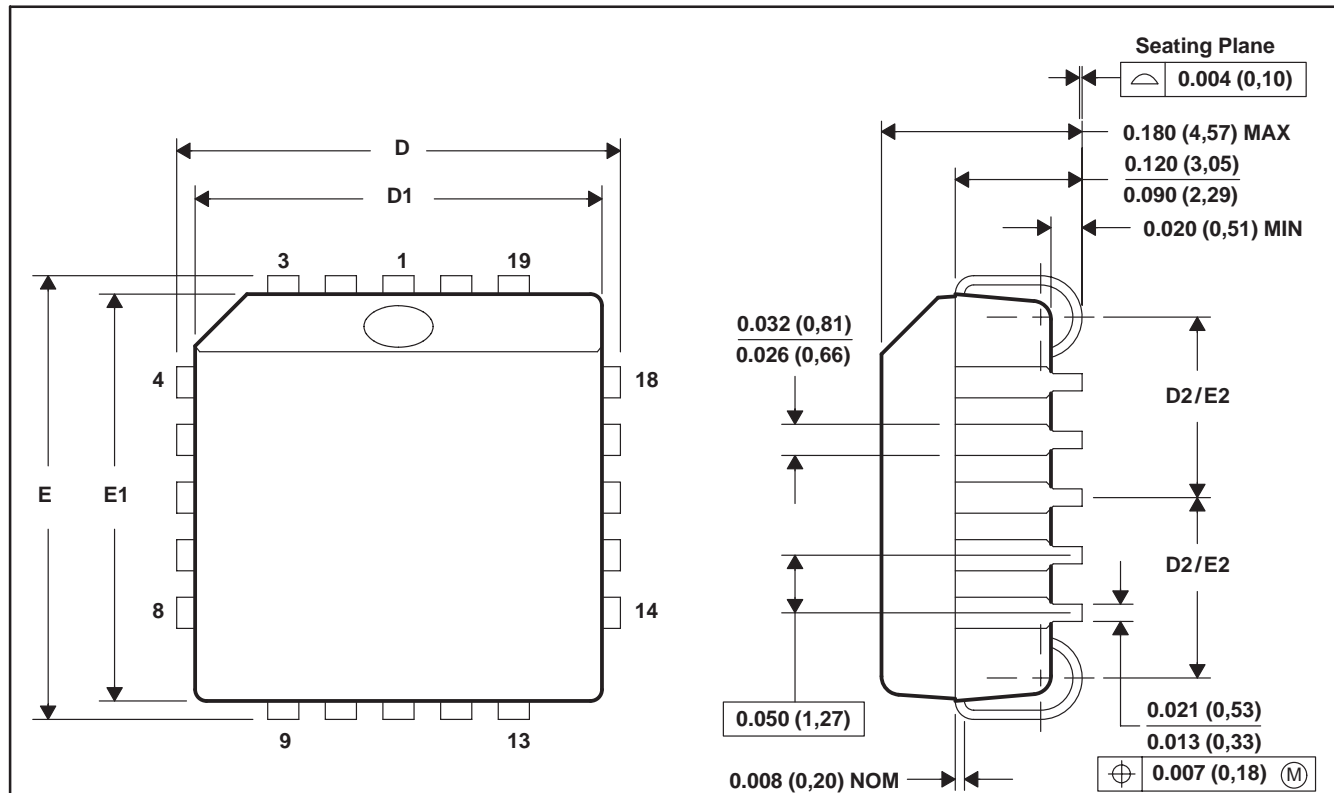


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-011  
 D. Falls within JEDEC MS-015 (32 pin only)

FN (S-PQCC-J\*\*)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-018

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