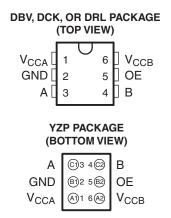


1-BIT BIDIRECTIONAL VOLTAGE-LEVEL TRANSLATOR FOR OPEN-DRAIN AND PUSH-PULL APPLICATIONS

FEATURES

- No Direction-Control Signal Needed
- Maximum Data Rates
 - 24 Mbps (Push Pull)
 - 2 Mbps (Open Drain)
- Available in the Texas Instruments NanoFree[™] Package
- 1.65 V to 3.6 V on A port and 2.3 V to 5.5 V on B port (V_{CCA} ≤ V_{CCB})
- V_{CC} Isolation Feature If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- No Power-Supply Sequencing Required Either V_{CCA} or V_{CCB} Can be Ramped First
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

- ESD Protection Exceeds JESD 22
 - A Port
 - 2500-V Human-Body Model (A114-B)
 - 200-V Machine Model (A115-A)
 - 1500-V Charged-Device Model (C101)
 - B Port
 - 8-kV Human-Body Model (A114-B)
 - 200-V Machine Model (A115-A)
 - 1500-V Charged-Device Model (C101)



DESCRIPTION/ORDERING INFORMATION

This one-bit noninverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.65 V to 3.6 V. The B port is designed to track V_{CCB} . V_{CCA} must be less than or equal to V_{CCB} . V_{CCB} accepts any supply voltage from 2.3 V to 5.5 V. This allows for low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

M

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.



ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
	NanoFree [™] – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	TXS0101YZPR	2G_
	SOT (SOT 22) DBV	Reel of 3000	TXS0101DBVR	NEE
	SOT (SOT-23) – DBV	Reel of 250	TXS0101DBVT	NFF_
–40°C to 85°C	00T (00 70) DOV	Reel of 3000	TXS0101DCKR	20
	SOT (SC-70) – DCK	Reel of 250	TXS0101DCKT	2G
	SOT (SOT-563) – DRL	Reel of 3000	TXS0101DRLR	20
	301 (301-303) - DRL	Reel of 250	TXS0101DRLT	2G

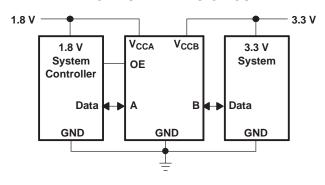
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

 DBV/DCK/DRL: The actual top-side marking has one additional character that designates the wafer fab/assembly site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

PIN DESCRIPTION

NO.	NAME	FUNCTION
1	V_{CCA}	A-port supply voltage. 1.65 V \leq V _{CCA} \leq 3.6 V and V _{CCA} \leq V _{CCB}
2	GND	Ground
3	Α	Input/output A. Referenced to V _{CCA} .
4	В	Input/output B. Referenced to V _{CCB} .
5	OE	Output enable. Pull OE low to place all outputs in 3-state mode. Referenced to V _{CCA} .
6	V _{CCB}	B-port supply voltage. 2.3 V ≤ V _{CCB} ≤ 5.5 V

TYPICAL OPERATING CIRCUIT





ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		-0.5	4.6	V
V_{CCB}	Supply voltage range		-0.5	6.5	V
V	Input voltage range (2)	A port	-0.5	4.6	V
VI	Input voltage range ⁽²⁾	B port, OE	-0.5	6.5	V
V	Voltage range applied to any output	A port	-0.5	4.6	V
Vo	in the high-impedance or power-off state (2)	B port	-0.5	6.5	V
.,	Valta and an analysis of the bight and an array (2)(3)	A port	-0.5	$V_{CCA} + 0.5$	V
Vo	Voltage range applied to any output in the high or low state (2)(3)	B port	-0.5	$V_{CCB} + 0.5$	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
lok	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current	·		±50	mA
	Continuous current through V _{CCA} , V _{CCB} , or GND			±100	mA
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE RATINGS

				UNIT
		DBV package	165	
	Dealine at the arm of importance (1)	DCK package	259	90.444
θ_{JA}	Package thermal impedance ⁽¹⁾	DRL package	142	°C/W
		YZP package	123	

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.



RECOMMENDED OPERATING CONDITIONS (1)(2)

			V _{CCA}	V _{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage (3)				1.65	3.6	V
V_{CCB}	Supply voltage .				2.3	5.5	V
		A-port I/Os	1.65 V to 1.95 V	2.3 V to 5.5 V	$V_{CCI} - 0.2$	V _{CCI}	
	Lligh lovel input voltage	A-port 1/OS	2.3 V to 3.6 V	2.5 V 10 5.5 V	$V_{CCI} - 0.4$	V _{CCI}	V
V _{IH}	High-level input voltage	B-port I/Os	1 65 V to 2 6 V	2.2.\/ to F.F.\/	V _{CCI} - 0.4	V _{CCI}	V
		OE input	1.65 V to 3.6 V	2.3 V to 5.5 V	V _{CCA} × 0.65	5.5	
		A-port I/Os			0	0.15	
V _{IL}	Low-level input voltage	B-port I/Os	1.65 V to 3.6 V	2.3 V to 5.5 V	0	0.15	V
		OE input			0	V _{CCA} × 0.35	
		A-port I/Os, push-pull driving				10	
Δt/Δv	Input transition rise or fall rate	B-port I/Os, push-pull driving	1.65 V to 3.6 V	2.3 V to 5.5 V		10	ns/V
		Control Input				10	
T _A	Operating free-air tempera	ture			-40	85	°C

- V_{CCI} is the supply associated with the input port.
- V_{CCO} is the supply associated with the output port. V_{CCA} must be less than or equal to V_{CCB} , and V_{CCA} must not exceed 3.6 V.

ELECTRICAL CHARACTERISTICS (1)(2)(3)

over recommended operating free-air temperature range (unless otherwise noted)

D.	DAMETED	TEST	V	V	T,	λ = 25°	С	-40°C to 85	5°C	UNIT
P	ARAMETER	CONDITIONS	V _{CCA}	V _{CCB}	MIN	TYP	MAX	MIN	MAX	UNII
V _{OHA}		$I_{OH} = -20 \mu A,$ $V_{IB} \ge V_{CCB} - 0.4 V$	1.65 V to 3.6 V	2.3 V to 5.5 V				V _{CCA} × 0.67		V
V _{OLA}		$I_{OL} = 1 \text{ mA},$ $V_{IB} \le 0.15 \text{ V}$	1.65 V to 3.6 V	2.3 V to 5.5 V					0.4	V
V _{OHB}		$I_{OH} = -20 \mu A,$ $V_{IA} \ge V_{CCA} - 0.2 V$	1.65 V to 3.6 V	2.3 V to 5.5 V				V _{CCB} × 0.67		V
V _{OLB}		$I_{OL} = 1 \text{ mA},$ $V_{IA} \le 0.15 \text{ V}$	1.65 V to 3.6 V	2.3 V to 5.5 V					0.4	V
I	OE		1.65 V to 3.6 V	1.65 V to 5.5 V			±1		±2	μΑ
	A port		0 V	0 to 5.5 V			±1		±2	μΑ
I _{off}	B port		0 to 3.6 V	0 V			±1		±2	μΑ
I _{OZ}	A or B port		1.65 V to 3.6 V	2.3 V to 5.5 V			±1		±2	μΑ
			1.65 V to V _{CCB}	2.3 V to 5.5 V					2.4	
I_{CCA}		$V_I = V_O = \text{open},$ $I_O = 0$	3.6 V	0 V					2.2	μΑ
		10 - 0	0 V	5.5 V					-1	
			1.65 V to V _{CCB}	2.3 V to 5.5 V					12	
I_{CCB}		$V_I = V_O = open,$ $I_O = 0$	3.6 V	0 V					-1	μΑ
		10 - 0	0 V	5.5 V					1	
I _{CCA} +	- I _{CCB}	$V_{I} = V_{CCI},$ $I_{O} = 0$	1.65 V to V _{CCB}	2.3 V to 5.5 V					14.4	μΑ
Cı	OE		3.3 V	3.3 V		2.5			3.5	pF
_	A port		221/	221/		5		6		
C _{io}	B port		3.3 V	3.3 V		6		7.5		pF

- V_{CCI} is the V_{CC} associated with the input port.
- (2)
- V_{CCO} is the V_{CC} associated with the output port. V_{CCA} must be less than or equal to V_{CCB} , and V_{CCA} must not exceed 3.6 V.

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TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

				V _{CCB} = 2 ± 0.2 \		V _{CCB} = 3 ± 0.3		V _{CCB} = ± 0.5		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate	Push-pull driving			21		22		24	Mhaa
	Data fate	Open-drain driving			2		2		2	Mbps
	Dulas duration	Push-pull driving	Data inputs	47		45		41		no
ι _W	t _w Pulse duration	Open-drain driving	Data iriputs	500		500		500		ns

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

				V _{CCB} = 2 ± 0.2		V _{CCB} = 3 ± 0.3		V _{CCB} = ± 0.5		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate	Push-pull driving			20		22		24	Mbps
	Dala Tale	Open-drain driving			2		2		1	MDPS
	Dulas duration	Push-pull driving	Data innuta	50		45		41		9
ı _w	t _w Pulse duration	Open-drain driving	Data inputs	500		500		500		ns

TIMING REQUIREMENTS

over recommended operating free-air temperature range, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted)

				V _{CCB} = 3 ± 0.3	3.3 V V	V _{CCB} = ± 0.5	= 5 V 5 V	UNIT
				MIN	MAX	MIN	MAX	
	Data rate	Push-pull driving			23		24	Mbps
	Data Tate	Open-drain driving			2		2	ivibps
	Pulse duration	Push-pull driving	Data inputa	43		41		20
t _w	Puise duration	Open-drain driving	Data inputs	500		500		ns

Product Folder Link(s): TXS0101



SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$ (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	V _{CCB} = ± 0.	= 2.5 V .2 V	V _{CCB} = ± 0.	= 3.3 V 3 V	V _{CCB} ± 0.	= 5 V 5 V	UNIT
	(INPUT)	(OUTPUT)	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	
			Push-pull driving		5.3		5.4		6.8	
t _{PHL}	А	В	Open-drain driving	2.3	8.8	2.4	9.6	2.6	10	ns
+	A	Ь	Push-pull driving		6.8		7.1		7.5	115
t _{PLH}			Open-drain driving	45	260	36	208	27	198	
•			Push-pull driving		4.4		4.5		4.7	
t _{PHL}	ь	А	Open-drain driving	1.9	5.3	1.1	4.4	1.2	4	ns
4	В		Push-pull driving		5.3		4.5		0.5	115
t _{PLH}			Open-drain driving	45	175	36	140	27	102	
t _{en}	OE	A or B			200		200		200	ns
t _{dis}	OE	A or B			50		40		35	ns
4	A-port r	iaa tima	Push-pull driving	3.2	9.5	2.3	9.3	2	7.6	no
t _{rA}	A-port i	ise ume	Open-drain driving	38	165	30	132	22	95	ns
4	P nort r	iaa tima	Push-pull driving	1.1	10.8	1	9.1	1	7.6	no
t _{rB}	B-port r	ise ume	Open-drain driving	34	145	23	106	10	76	ns
	A north	iall time	Push-pull driving	1.9	5.9	1.9	6	1.4	13.3	
t _{fA}	A-port f	all time	Open-drain driving	4.4	6.9	4.3	6.4	4.2	6.1	
	Doort	iall time	Push-pull driving	2.2	13.8	2.2	16.2	2.6	16.2	ns
t _{fB}	B-port f	an unie	Open-drain driving	6.9	13.8	7.5	16.2	7	16.2	
May data rata			Push-pull driving	21		22		24		Mhna
wax data fate	Max data rate		Open-drain driving	2		2		2		Mbps



SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CCB} = ± 0.			= 3.3 V 3 V	V _{CCB}	= 5 V 5 V	UNIT	
	(INPUT)	(OUTPUT)	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX		
			Push-pull driving		3.2		3.7		3.8		
t _{PHL}	Α	В	Open-drain driving	1.7	6.3	2	6	2.1	5.8	ns	
	A	D	D	Push-pull driving		3.5		4.1		4.4	115
t _{PLH}			Open-drain driving	43	250	36	206	27	190		
			Push-pull driving		3		3.6		4.3		
t _{PHL}	В	Δ	Open-drain driving	1.8	4.7	1.6	4.2	1.2	4		
	Б	Α	Push-pull driving		2.5		1.6		1	ns	
t _{PLH}			Open-drain driving	44	170	37	140	27	103		
t _{en}	OE	A or B			200		200		200	ns	
t _{dis}	OE	A or B			50		40		35	ns	
	A nort r	ion time	Push-pull driving	2.8	7.4	2.1	6.6	0.9	5.6	20	
t _{rA}	A-port r	ise ume	Open-drain driving	34	149	28	121	24	89	ns	
	Doorte	ion time	Push-pull driving	1.3	8.3	0.9	7.2	0.4	6.1	20	
t _{rB}	B-port r	ise ume	Open-drain driving	35	151	24	112	12	81	ns	
	A	all times	Push-pull driving	1.9	5.7	1.4	5.5	0.8	5.3		
t _{fA}	A-port f	all time	Open-drain driving	4.4	6.9	4.3	6.2	4.2	5.8	ns	
4	D nort f	all time	Push-pull driving	2.2	7.8	2.4	6.7	2.6	6.6	20	
t _{fB}	B-port f	all liffle	Open-drain driving	5.1	8.8	5.4	9.4	5.4	10.4	ns	
May data rata				20		22		24		Mhna	
Max data rate			Open-drain driving	2		2		2		Mbps	



SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	FROM	TO (OUTPUT)	TEST CONDITIONS	V _{CCB} = ± 0.3	3.3 V 3 V	V _{CCB} ± 0.		UNIT
	(INPUT)	(OUTPUT)	CONDITIONS	MIN	MAX	MIN	MAX	
			Push-pull driving		2.4		3.1	
t _{PHL}	Α	В	Open-drain driving	1.3	4.2	1.4	4.6	no
4	t _{PLH}		Push-pull driving		4.2		4.4	ns
\PLH			Open-drain driving	36	204	28	165	
			Push-pull driving		2.5		3.3	
t _{PHL}	В	^	Open-drain driving	1	124	1	97	
	D	A	Push-pull driving		2.5		2.6	ns
t _{PLH}			Open-drain driving	3	139	3	105	
t _{en}	OE	A or B			200		200	ns
t _{dis}	OE	A or B			40		35	ns
	A nort r	iaa tima	Push-pull driving	2.3	5.6	1.9	4.8	
t _{rA}	A-port i	ise time	Open-drain driving	25	116	19	85	ns
	Doort	iaa tima	Push-pull driving	1.6	6.4	0.6	7.4	
t _{rB}	Б-роп г	ise time	Open-drain driving	26	116	14	72	ns
	A	fall time -	Push-pull driving	1.4	5.4	1	5	
t _{fA}	A-port	fall time	Open-drain driving	4.3	6.1	4.2	5.7	ns
	Donati	fall 4:	Push-pull driving	2.3	7.4	2.4	7.6	
t _{fB}	B-port	fall time	Open-drain driving	5	7.6	4.8	8.3	ns
May data nata			Push-pull driving	23		24		Mhair
Max data rate			Open-drain driving	2		2		Mbps

PRINCIPLES OF OPERATION

Applications

The TXS0101 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The TXS0101 is ideal for use in applications where an open-drain driver is connected to the data I/Os. The TXB0101 can also be used in applications where a push-pull driver is connected to the data I/Os, but the TXB0102 might be a better option for such push-pull applications.

Architecture

The TXS0101 architecture (see Figure 1) does not require a direction-control signal to control the direction of data flow from A to B or from B to A.



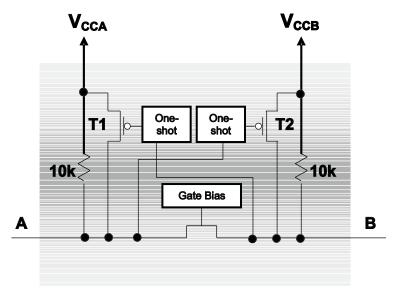


Figure 1. Architecture of a TXS01xx Cell

Each A-port I/O has an internal $10-k\Omega$ pullup resistor to V_{CCA} , and each B-port I/O has an internal $10-k\Omega$ pullup resistor to V_{CCB} . The output one-shots detect rising edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1,T2) for a short duration, which speeds up the low-to-high transition.

Input Driver Requirements

The fall time (t_{fA} , t_{fB}) of a signal depends on the output impedance of the external device driving the data I/Os of the TXS0101. Similarly, the t_{PHL} and max data rates also depend on the output impedance of the external driver. The values for t_{fA} , t_{fB} , t_{PHL} , and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50 Ω .

Power Up

During operation, ensure that $V_{CCA} \le V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \ge V_{CCB}$ does not damage the device, so any power supply can be ramped up first.

Enable and Disable

The TXS0101 has an OE input that is used to disable the device by setting OE low, which places all I/Os in the Hi-Z state. The disable time (t_{dis}) indicates the delay between the time when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

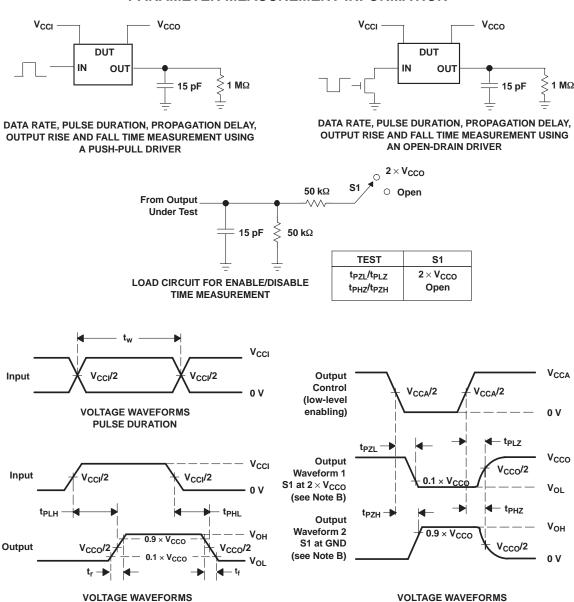
Pullup or Pulldown Resistors on I/O Lines

Each A-port I/O has an internal 10-k Ω pullup resistor to V_{CCA}, and each B-port I/O has an internal 10-k Ω pullup resistor to V_{CCB}. If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal 10-k Ω resistors).

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PARAMETER MEASUREMENT INFORMATION



A. C_L includes probe and jig capacitance.

PROPAGATION DELAY TIMES

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{Ω} = 50 Ω , $dv/dt \geq$ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.
- J. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

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ENABLE AND DISABLE TIMES





20-May-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TXS0101DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFFF ~ NFFR)	Samples
TXS0101DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFFF ~ NFFR)	Samples
TXS0101DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	NFFR	Samples
TXS0101DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFFR	Samples
TXS0101DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2GO	Samples
TXS0101DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2GO	Samples
TXS0101DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2GO	Samples
TXS0101DCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2GO	Samples
TXS0101DRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2GR	Samples
TXS0101DRLRG4	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2GR	Samples
TXS0101YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	2G7	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

20-May-2013

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above. **Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight

in homogeneous material)

- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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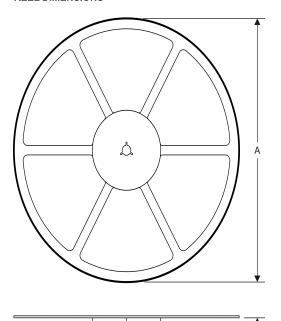
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PACKAGE MATERIALS INFORMATION

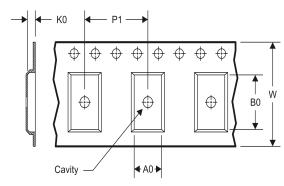
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TAPE AND REEL INFORMATION

REEL DIMENSIONS







A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0101DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TXS0101DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TXS0101DCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TXS0101DCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TXS0101DRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TXS0101YZPR	DSBGA	YZP	6	3000	180.0	8.4	1.02	1.52	0.63	4.0	8.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0101DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
TXS0101DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
TXS0101DCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TXS0101DCKT	SC70	DCK	6	250	203.0	203.0	35.0
TXS0101DRLR	SOT	DRL	6	4000	202.0	201.0	28.0
TXS0101YZPR	DSBGA	YZP	6	3000	220.0	220.0	34.0

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- Falls within JEDEC MO-178 Variation AB, except minimum lead width.



DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AB.



DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DRL (R-PDSO-N6)

PLASTIC SMALL OUTLINE



NOTES:

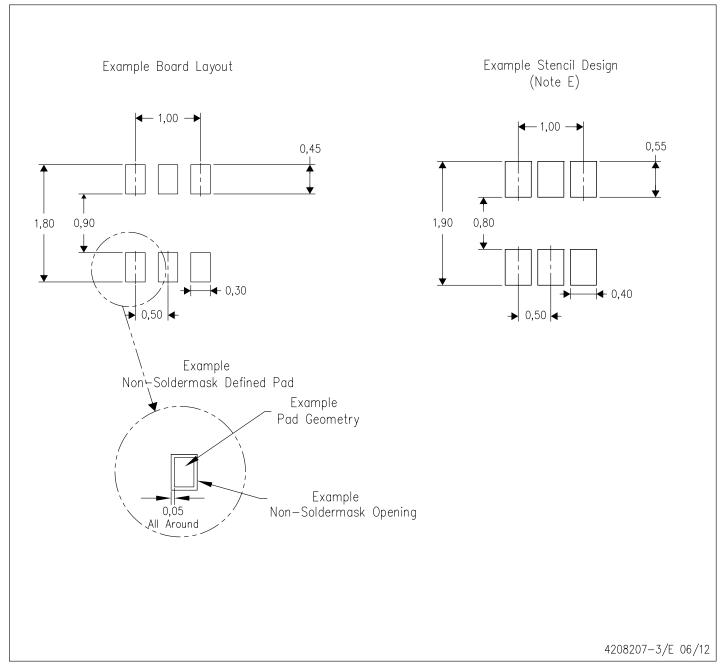
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs.

 Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
- D. JEDEC package registration is pending.



DRL (R-PDSO-N6)

PLASTIC SMALL OUTLINE



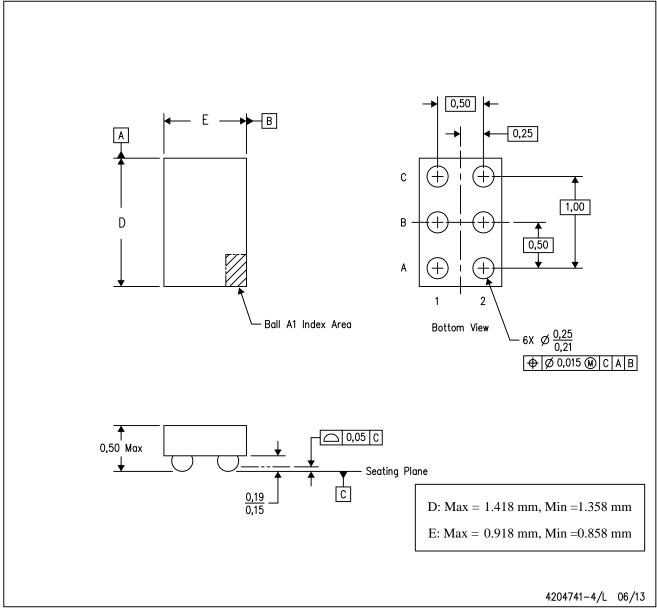
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over—print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. NanoFree \mathbf{M} package configuration.

NanoFree is a trademark of Texas Instruments.



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