DUAL CHANNEL, 12-BITS, 125/105/80/65 MSPS ADC WITH DDR LVDS/CMOS OUTPUTS

Check for Samples: ADS62P24, ADS62P25, ADS62P22, ADS62P23

FEATURES

- **Maximum Sample Rate: 125 MSPS**
- **12-Bit Resolution with No Missing Codes**
- **95 dB Crosstalk**
- **Parallel CMOS and DDR LVDS Output Options**
- **3.5 dB Coarse Gain and Programmable Fine Gain up to 6 dB for SNR/SFDR Trade-Off**
- ***Digital Processing Block* with:**
  - **Offset Correction**
  - **Fine Gain Correction, in Steps of 0.05 dB**
  - **Decimation by 2/4/8**
  - **Built-in and Custom Programmable 24-Tap Low-/High-/Band-Pass Filters**
- **Supports Sine, LVPECL, LVDS, and LVCMOS Clocks and Amplitude Down to 400 mV_{PP}**
- **Clock Duty Cycle Stabilizer**
- **Internal Reference; Supports External Reference also**
- **64-QFN Package (9mm × 9mm)**
- **Pin Compatible 14-Bit Family (ADS62P4X)**

APPLICATIONS

- **Wireless Communications Infrastructure**
- **Software Defined Radio**
- **Power Amplifier Linearization**
- **802.16d/e**
- **Test and Measurement Instrumentation**
- **High Definition Video**
- **Medical Imaging**
- **Radar Systems**

DESCRIPTION

ADS62P2X is a dual channel 12-bit A/D converter family with maximum sample rates up to 125 MSPS. It combines high performance and low power consumption in a compact 64 QFN package. Using an internal sample and hold and low jitter clock buffer, the ADC supports high SNR and high SFDR at high input frequencies. It has coarse and fine gain options that can be used to improve SFDR performance at lower full-scale input ranges.

ADS62P2X includes a digital processing block that consists of several useful and commonly used digital functions such as ADC offset correction, fine gain correction (in steps of 0.05 dB), decimation by 2,4,8 and in-built and custom programmable filters. By default, the digital processing block is bypassed, and its functions are disabled.

Two output interface options exist – parallel CMOS and DDR LVDS (Double Data Rate). ADS62P2X includes internal references while traditional reference pins and associated decoupling capacitors have been eliminated. Nevertheless, the device can also be driven with an external reference. The device is specified over the industrial temperature range (–40°C to 85°C).

Table 1. ADS62P2X Performance Summary

		ADS62P25	ADS62P24	ADS62P23	ADS62P22
SFDR, dBc	F_{in} = 10 MHz (0 dB gain)	88	92	93	94
	F_{in} = 190 MHz (3.5 dB gain)	84	86	87	85
SINAD, dBFS	F_{in} = 10 MHz (0 dB gain)	71	71.3	71.5	71.5
	F_{in} = 190 MHz (3.5 dB gain)	69.5	69.5	69.7	69.2
Analog power, mW		799	710	594	515

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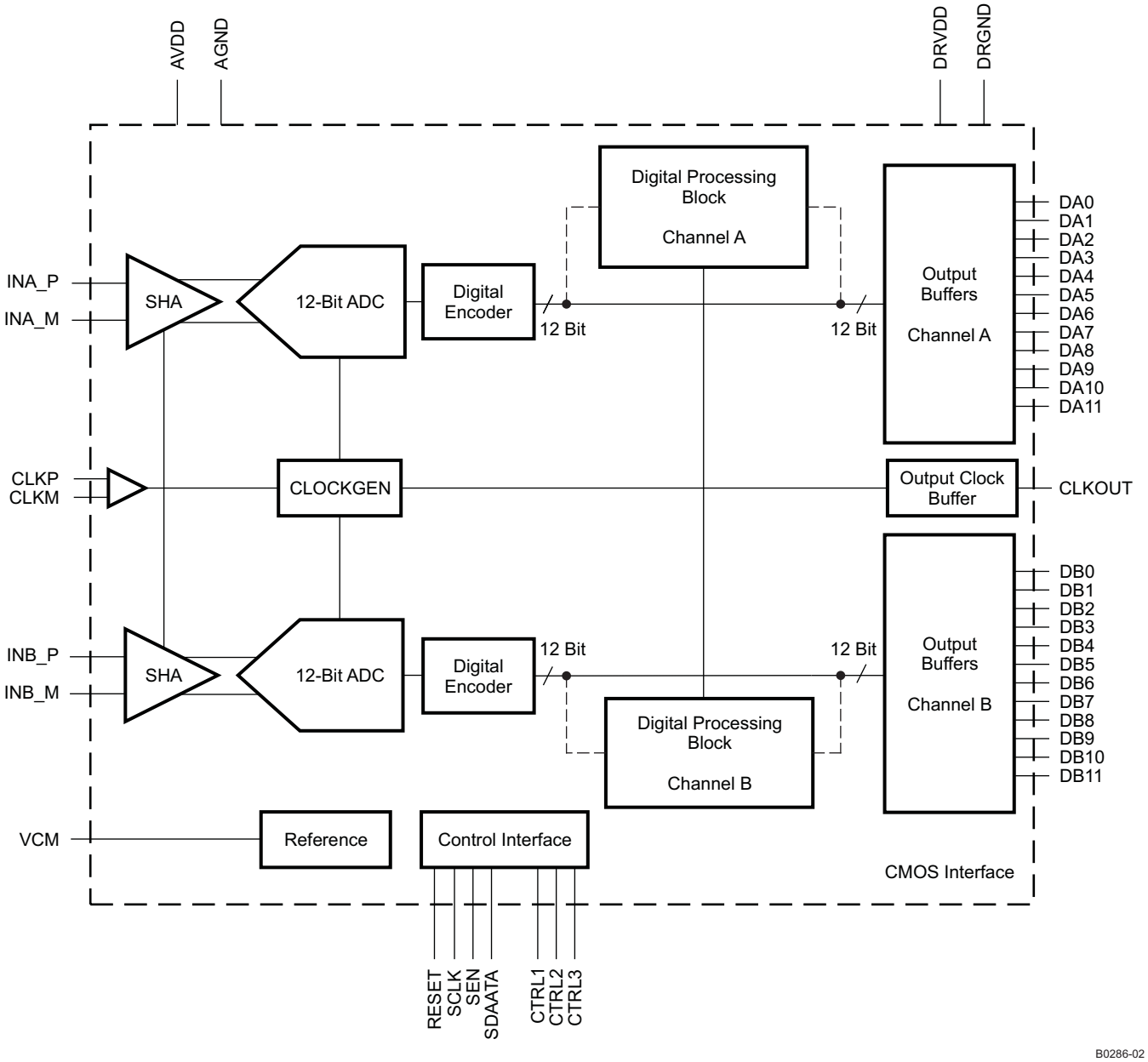
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



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ADS62PXX Family

	125 MSPS	105 MSPS	80 MSPS	65 MSPS
ADS62P4X 14 Bits	ADS62P45	ADS62P44	ADS62P43	ADS62P42
ADS62P2X 12 Bits	ADS62P25	ADS62P24	ADS62P23	ADS62P22

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PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS62P25	QFN-64(2)	RGC	–40°C to 85°C	AZ62P25	ADS62P25IRGCT	Tape and Reel, 250
					ADS62P25IRGCR	Tape and Reel, 2500
ADS62P24	QFN-64(2)	RGC	–40°C to 85°C	AZ62P24	ADS62P24IRGCT	Tape and Reel, 250
					ADS62P24IRGCR	Tape and Reel, 2500
ADS62P23	QFN-64(2)	RGC	–40°C to 85°C	AZ62P23	ADS62P23IRGCT	Tape and Reel, 250
					ADS62P23IRGCR	Tape and Reel, 2500
ADS62P22	QFN-64(2)	RGC	–40°C to 85°C	AZ62P22	ADS62P22IRGCT	Tape and Reel, 250
					ADS62P22IRGCR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) For thermal pad size on the package, see the mechanical drawings at the end of this data sheet. θ_{JA} = 23.17 °C/W (0 LFM air flow), θ_{JC} = 22.1 °C/W when used with 2 oz. copper trace and pad soldered directly to a JEDEC standard four layer 3 in × 3 in (7.62 cm × 7.62 cm) PCB.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
V_I	Supply voltage range, AVDD	–0.3 to 3.9	V
	Supply voltage range, DRVDD	–0.3 to 3.9	V
	Voltage between AGND and DRGND	–0.3 to 0.3	V
	Voltage between AVDD to DRVDD	–0.3 to 3.3	V
	Voltage applied to VCM pin (in external reference mode)	–0.3 to 2	V
	Voltage applied to analog input pins, INP and INM	–0.3 to minimum (3.6, AVDD + 0.3)	V
	Voltage applied to analog input pins, CLKP and CLKM	–0.3 to (AVDD + 0.3)	V
T_A	Operating free-air temperature range	–40 to 85	°C
T_J	Operating junction temperature range	125	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		3	3.3	3.6	V
DRVDD	Output buffer supply voltage (1)	CMOS interface	1.65	1.8 to 3.3	3.6	V
		LVDS interface	3	3.3	3.6	V
ANALOG INPUTS						
	Differential input voltage range			2		V_{pp}
V_{IC}	Input common-mode voltage			1.5 ± 0.1		V
	Voltage applied on VCM in external reference mode		1.45	1.5	1.55	V
CLOCK INPUT						
	Input clock sample rate, F_S	ADS62P25	1		125	MSPS
		ADS62P24	1		105	
		ADS62P23	1		80	
		ADS62P22	1		65	
	Input clock amplitude differential ($V_{CLKP} – V_{CLKM}$)	Sine wave, ac-coupled	0.4	1.5		V_{pp}
		LVPECL, ac-coupled		± 0.8		
		LVDS, ac-coupled		± 0.35		
		LVCMOS, ac-coupled		3.3		
	Input Clock duty cycle		35%	50%	65%	
DIGITAL OUTPUTS						
	Output buffer drive strength (2)	for C_{LOAD} ≤ 5 pF and DRVDD ≥ 2.2 V		DEFAULT strength		
		for C_{LOAD} > 5 pF and DRVDD ≥ 2.2 V		MAXIMUM strength		
		for DRVDD < 2.2 V		MAXIMUM strength		
C_{LOAD}	Maximum external load capacitance from each output pin to DRGND	CMOS interface, maximum buffer strength		10		pF
		LVDS interface, without internal termination		5		
		LVDS interface, with internal termination		10		
R_{LOAD}	Differential load resistance (external) between the LVDS output pairs			100		Ω
T_A	Operating free-air temperature		-40		85	°C

(1) For easy migration to the next generation, higher sampling speed devices (> 125 MSPS), use 1.8 V DRVDD supply.
(2) See *Output Buffer Strength Programmability* in application section

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ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V to 3.3 V, maximum rated sampling frequency, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, applies to CMOS and LVDS interfaces, unless otherwise noted.

Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3 V, DRVDD = 3.3 V, unless otherwise noted.

PARAMETER			ADS62P25 F_S = 125 MSPS			ADS62P24 F_S = 105 MSPS			ADS62P23 F_S = 80 MSPS			ADS62P22 F_S = 65 MSPS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			12			12			12		Bits
ANALOG INPUT															
	Differential input voltage range			2			2			2			2		V_{PP}
	Differential input resistance (dc) see Figure 83			> 1			> 1			> 1			> 1		MΩ
	Differential input capacitance see Figure 84			7			7			7			7		pF
	Analog input bandwidth			450			450			450			450		MHz
	Analog input common mode current (per input pin of each ADC)			1.3			1.3			1.3			1.3		µA/MSPS
REFERENCE VOLTAGES															
VREFB	Internal reference bottom voltage			1			1			1			1		V
VREFT	Internal reference top voltage			2			2			2			2		V
V_{CM}	Common mode output voltage			1.5			1.5			1.5			1.5		V
	V_{CM} output current capability			4			4			4			4		mA
DC ACCURACY															
	No missing codes			Specified			Specified			Specified			Specified		
E_O	Offset error		-10	± 2	10	-10	± 2	10	-10	± 2	10	-10	± 2	10	mV
	Offset error temperature coefficient			0.05			0.05			0.05			0.05		mV/°C
	There are two sources of gain error – internal reference inaccuracy and channel gain error														
E_{GREF}	Gain error due to internal reference inaccuracy alone, (ΔV_{REF} /2) %		-2	±0.25	2	-2	±0.25	2	-2	±0.25	2	-2	±0.25	2	% FS
E_{GCHAN}	Gain error of channel alone[1] across devices & across channels within a device		-1	±0.3	1	-1	±0.3	1	-1	±0.3	1	-1	±0.3	1	% FS
	Channel gain error temperature coefficient			0.005			0.005			0.005			0.005		Δ%/°C
DNL	Differential nonlinearity		-0.75	±0.3		-0.75	±0.3		-0.75	±0.3		-0.75	±0.3		LSB
INL	Integral nonlinearity		-2	±0.6	2	-2	±0.6	2	-2	±0.6	2	-2	±0.6	2	LSB
POWER SUPPLY															
I_{AVDD}	Analog supply current			240	275		212	240		177	200		153	175	mA
I_{DRVDD}	Digital supply current, **CMOS** interface DRVDD = 1.8 V F_{IN}= 2 MHZ [2]	No external load capacitance		15			13			11.5			10		mA
		10 pF external load capacitance		28			25			21			18		mA
I_{DRVDD}	Digital supply current, **LVDS** interface DRVDD = 3.3 V with 100 Ω external termination			73			73			73			73		mA
P_{AVDD}	Analog power dissipation			799	908		710	792		594	660		515	578	mW
P_{DRVDD}	Digital power dissipation CMOS interface DRVDD = 1.8 V [3]	No external load capacitance		27			24			21			18		mW
		10 pF external load capacitance		51			45			38			32		mW
	Global powerdown			50	75		50	75		50	75		50	75	mW

(1) This is specified by design and characterization; it is not tested in production.
(2) In CMOS mode, the DRVDD current scales with the sampling frequency, load capacitance on output pins, input frequency and supply voltage (see **Figure 80** and CMOS power dissipation in the application section).
(3) The maximum DRVDD current depends on the actual load capacitance on the digital output lines. Note that the maximum recommended load capacitance is 10 pF.

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ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V to 3.3 V, maximum rated sampling frequency, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, applies to CMOS and LVDS interfaces, unless otherwise noted.

Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3 V, DRVDD = 3.3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS		ADS62P25 F_S = 125 MSPS			ADS62P24 F_S = 105 MSPS			ADS62P23 F_S = 80 MSPS			ADS62P22 F_S = 65 MSPS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC AC CHARACTERISTICS															
SNR Signal to Noise Ratio	Fin = 10 MHz			71.3			71.5			71.6			71.6		dBFS
	Fin = 50 MHz		68.5	71.1			71.3		69	71.4			71.4		
	Fin = 70 MHz			71		68.5	71.2			71.3		69	71.3		
	Fin = 190 MHz	0 dB gain		70.2			70.2			70.3			69.9		
		3.5 dB coarse gain		69.5			69.5			69.7			69.2		
RMS Output Noise	Inputs tied to common-mode														LSB
SINAD Signal to Noise and Distortion Ratio	Fin = 10 MHz			71			71.3			71.5			71.5		dBFS
	Fin = 50 MHz		68	70.5			70.9		68.5	71.3			71.3		
	Fin = 70 MHz			70.7		68	70.9			71.1		68.5	71.1		
	Fin = 190 MHz	0 dB gain		69.6			69.9			69.8			69.7		
		3.5 dB coarse gain		69.2			69.3			69.5			69.4		
ENOB Effective Number of Bits	Fin = 50 MHz		11.0	11.4					11.1	11.6					Bits
	Fin = 70 MHz					11.0	11.5					11.1	11.5		
SFDR Spurious Free Dynamic Range	Fin = 10 MHz			88			92			93			94		dBc
	Fin = 50 MHz		76	80			83		79	87			87		
	Fin = 70 MHz			86		76	85			89		79	89		
	Fin = 190 MHz	0 dB gain		81			83			83			81		
		3.5 dB coarse gain		84			86			87			85		
THD Total Harmonic Distortion	Fin = 10 MHz			88			90			92			93		dBc
	Fin = 50 MHz		74	79			82		76	86			86		
	Fin = 70 MHz			84.5		75	84			88		77	88		
	Fin = 190 MHz	0 dB gain		79			80			80			79		
		3.5 dB coarse gain		81			82			82			82		
HD2 Second Harmonic Distortion	Fin = 10 MHz			94			93			95			98		dBc
	Fin = 50 MHz		76	92			93		79	94			97		
	Fin = 70 MHz			92		76	93			94		79	96		
	Fin = 190 MHz	0 dB gain		86			86			85			86		
		3.5 dB coarse gain		88			88			88			89		
HD3 Third Harmonic Distortion	Fin = 10 MHz			88			92			93			94		dBc
	Fin = 50 MHz		76	80			83		79	87			87		
	Fin = 70 MHz			86		76	85			89		79	89		
	Fin = 190 MHz	0 dB gain		81			83			83			81		
		3.5 dB coarse gain		84			86			87			85		
Worst Spur (Other than HD2, HD3)	Fin = 10 MHz			95			96			97			99		dBc
	Fin = 50 MHz			94			95			96			98		
	Fin = 70 MHz			94			95			96			97		
	Fin = 190 MHz			90			93			95			92		

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ELECTRICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V to 3.3 V, maximum rated sampling frequency, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, applies to CMOS and LVDS interfaces, unless otherwise noted.

Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3 V, DRVDD = 3.3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS62P25 F_S = 125 MSPS			ADS62P24 F_S = 105 MSPS			ADS62P23 F_S = 80 MSPS			ADS62P22 F_S = 65 MSPS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
IMD 2-Tone Intermodulation Distortion	F1 = 185 MHz, F2 = 190 MHz each tone at -7 dBFS		88			87			92			92		dBFS
Crosstalk	Up to 100 MHz		95			95			95			95		dB
Input Overload Recovery	Recovery to within 1% (of final value) for 6-dB overload with sine wave input		1			1			1			1		clock cycles
PSRR AC Power Supply Rejection Ratio	for 100 mVpp signal on AVDD supply		35			35			35			35		dBc

DIGITAL CHARACTERISTICS(1)

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1 AVDD = 3.0 V to 3.6 V.

PARAMETER	TEST CONDITIONS	ADS62P25/ADS62P24 ADS62P23/ADS62P22			UNIT
		MIN	TYP	MAX	
DIGITAL INPUTS RESET, CTRL1, CTRL2, CTRL3, SCLK, SDATA, SEN (2) (3)					
High-level input voltage		2.4			V
Low-level input voltage				0.8	V
High-level input current			33		µA
Low-level input current			–33		µA
Input capacitance			4		pF
DIGITAL OUTPUTS CMOS INTERFACE, DRVDD = 1.65 V to 3.6 V					
High-level output voltage			DRVDD		V
Low-level output voltage			0		V
Output capacitance	Output capacitance inside the device, from each output to ground		2		pF
DIGITAL OUTPUTS LVDS INTERFACE, DRVDD = 3.0 V to 3.6 V, I_O = 3.5 mA, R_L = 100 Ω (4)					
High-level output voltage			1375		mV
Low-level output voltage			1025		mV
Output differential voltage, $\|V_{OD}\|$		225	350		mV
V_{OS} Output offset voltage, single-ended	Common-mode voltage of OUTP, OUTM		1200		mV
Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

(1) All LVDS and CMOS specifications are characterized, but not tested at production.
(2) SCLK and SEN function as digital input pins when they are used for serial interface programming. When used as parallel control pins, analog voltage needs to be applied as per Table 4 and Table 5.
(3) All digital input pins are referred to AVDD supply.
(4) I_O refers to the LVDS buffer current setting, R_L is the differential load resistance between the LVDS output pair.

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TIMING CHARACTERISTICS – LVDS AND CMOS MODES(1)

Typical values are specified at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} clock amplitude, C_L = 5 pF(2), I_O = 3.5 mA, R_L = 100 Ω (3), no internal termination, unless otherwise noted.
Min and max values are specified across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.0 V to 3.6 V, unless otherwise specified.

PARAMETER		TEST CONDITIONS		ADS62P25 F_S = 125 MSPS			ADS62P24 F_S = 105 MSPS			ADS62P23 F_S = 80 MSPS			ADS62P22 F_S = 65 MSPS			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_a	Aperture delay			0.7	1.5	2.5	0.7	1.5	2.5	0.7	1.5	2.5	0.7	1.5	2.5	ns
	Aperture delay variation	channel-to-channel within a device			±80			±80			±80			±80		ps
t_j	Aperture jitter				150			150			150			150		fs rms
	Wake-up time (to valid data)	from global powerdown			15	50		15	50		15	50		15	50	µs
		from standby			15	50		15	50		15	50		15	50	µs
		from output buffer disable	**CMOS**		100	200		100	200		100	200		100	200	ns
			LVDS		200	500		200	500		200	500		200	500	ns
	Latency	Default, after reset			14			14			14			14		clock cycles
		with low latency mode enabled			10			10			10			10		clock cycles
		with digital filter enabled			15			15			15			15		clock cycles
DDR LVDS MODE(4), DRVDD = 3.0 V to 3.6V																
t_{su}	Data setup time(5)	Data valid (6) to zero-cross of CLKOUTP		0.6	1.5		1.0	2.3		2.4	3.8		3.8	5.2		ns
t_h	Data hold time(5)	Zero-cross of CLKOUTP to data becoming invalid(6)		1.0	2.3		1.0	2.3		1.0	2.3		1.0	2.3		ns
t_{PDI}	Clock propagation delay	Input clock rising edge zero-cross to output clock rising edge zero-cross		3.5	5.5	7.5	3.5	5.5	7.5	3.5	5.5	7.5	3.5	5.5	7.5	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP-CLKOUTM) 10 ≤ Fs ≤ 125 MSPS		46%	50%	53%	46%	50%	53%	46%	50%	53%	46%	50%	53%	
t_r t_f	Data rise time, Data fall time	Rise time measured from –50 mV to 50 mV Fall time measured from 50 mV to –50 mV 1 ≤ Fs ≤ 125 MSPS		70	100	170	70	100	170	70	100	170	70	100	170	ps
$t_{CLKRISE}$ $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –50 mV to 50 mV Fall time measured from 50 mV to –50 mV 1 ≤ Fs ≤ 125 MSPS		70	100	170	70	100	170	70	100	170	70	100	170	ps

(1) Timing parameters are specified by design and characterization and not tested in production.
(2) C_L is the effective external single-ended load capacitance between each output pin and ground.
(3) I_O refers to the LVDS buffer current setting; R_L is the differential load resistance between the LVDS output pair.
(4) Measurements are done with a transmission line of 100 Ω characteristic impedance between the device and the load.
(5) Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(6) Data valid refers to logic high of +100 mV and logic low of –100 mV.

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TIMING CHARACTERISTICS – LVDS AND CMOS MODES(1) (continued)

Typical values are specified at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} clock amplitude, C_L = 5 pF(2), I_O = 3.5 mA, R_L = 100 Ω (3), no internal termination, unless otherwise noted.
Min and max values are specified across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.0 V to 3.6 V, unless otherwise specified.

PARAMETER		TEST CONDITIONS	ADS62P25 F_S = 125 MSPS			ADS62P24 F_S = 105 MSPS			ADS62P23 F_S = 80 MSPS			ADS62P22 F_S = 65 MSPS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
PARALLEL CMOS MODE, DRVDD = 2.5 V to 3.6 V, default output buffer drive strength (7)															
t_{su}	Data setup time(8)	Data valid(9) to 50% of CLKOUT rising edge	2.0	3.5		2.8	4.3		4.3	5.8		5.7	7.2		ns
t_h	Data hold time(8)	50% of CLKOUT rising edge to data becoming invalid(9)	2.0	3.5		2.7	4.2		4.2	5.7		5.6	7.1		ns
t_{PDI}	Clock propagation delay	Input clock rising edge zero-cross to 50% of CLKOUT rising edge	5.8	7.3	8.8	5.8	7.3	8.8	5.8	7.3	8.8	5.8	7.3	8.8	ns
	Output clock duty cycle	Duty cycle of output clock (CLKOUT) 10 ≤ Fs ≤ 125 MSPS	45%	53%	60%	45%	53%	60%	45%	53%	60%	45%	53%	60%	
t_r t_f	Data rise time Data fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD 1 ≤ Fs ≤ 125 MSPS	1.0	1.8	2.5	1.0	1.8	2.5	1.0	1.8	2.5	1.0	1.8	2.5	ns
$t_{CLKRISE}$ $t_{CLKFALL}$	Output clock rise time Output clock fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD 1 ≤ Fs ≤ 125 MSPS	1.0	1.8	2.5	1.0	1.8	2.5	1.0	1.8	2.5	1.0	1.8	2.5	ns
PARALLEL CMOS INTERFACE, DRVDD = 1.8 V, maximum buffer drive strength (10)															
t_{START}	Input clock rising edge to data valid (11) (12)				8.5			7.5			5.5			3.6	ns
t_{DV}	Width of valid data window		3.3	6.0		5.0	7.5		8.0	10.5		10.5	13.5		ns

(7) For DRVDD < 2.2 V, it is recommended to use external clock for data capture and NOT the device output clock signal (CLKOUT). See *Parallel CMOS interface* in application section.
(8) Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(9) Data valid refers to logic high of 2 V (1.7 V) and logic low of 0.8 V (0.7 V) for DRVDD = 3.3 V (2.5 V).
(10) For DRVDD < 2.2 V, output clock cannot be used for data capture. A delayed version of the input clock can be used, that gives the desired setup and hold times at the receiving chip.
(11) Data valid refers to logic high of 1.26V and logic low of 0.54V for DRVDD = 1.8V.
(12) Measured from zero-crossing of input clock having 50% duty cycle.

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TIMING CHARACTERISTICS – LVDS AND CMOS MODES(1)

Typical values are specified at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} clock amplitude, C_L = 5 pF(2), I_O = 3.5 mA, R_L = 100 Ω (3), no internal termination, unless otherwise noted.
Min and max values are specified across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.0 V to 3.6 V, unless otherwise specified.

PARAMETER		TEST CONDITIONS	F_S = 65 MSPS			F_S = 40 MSPS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
PARALLEL CMOS INTERFACE, DRVDD = 1.8 V, MULTIPLEXED MODE, maximum buffer drive strength (4)									
t_{START_CHA}	Input clock falling edge to channel A data getting valid (5) (6)			0.8	2.3		8	9.5	ns
t_{DV_CHA}	Width of valid data window		5.4	6.4		10.3	11.3		ns
t_{START_CHB}	Input clock falling edge to channel A data getting valid (5) (6)			1.1	2.4		8.4	9.7	ns
t_{DV_CHB}	Width of valid data window		5	6		9.7	10.7		ns

(1) Timing parameters are specified by design and characterization and not tested in production.
(2) C_L is the effective external single-ended load capacitance between each output pin and ground.
(3) I_O refers to the LVDS buffer current setting; R_L is the differential load resistance between the LVDS output pair.
(4) For DRVDD < 2.2 V, output clock cannot be used for data capture. A delayed version of the input clock can be used, that gives the desired setup and hold times at the receiving chip
(5) Data valid refers to logic high of 1.26V and logic low of 0.54V for DRVDD = 1.8V.
(6) Measured from zero-crossing of input clock having 50% duty cycle.

Table 2. Timing Characteristics at Lower Sampling Frequencies

SAMPLING FREQUENCY, MSPS	t_{su} DATA SETUP TIME, ns			t_h DATA HOLD TIME, ns			t_{PDI} CLOCK PROPAGATION DELAY, ns		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
CMOS INTERFACE, DRVDD = 2.5 V TO 3.6 V									
40	10.5	12		10.3	11.8		5.8	7.3	8.8
20	23	24.5		23	24.5				
LVDS INTERFACE, DRVDD = 3.0 V to 3.6 V									
40	8.5	10		1	2.3		3.5	5.5	7.5
20	21	22.5		1	2.3				

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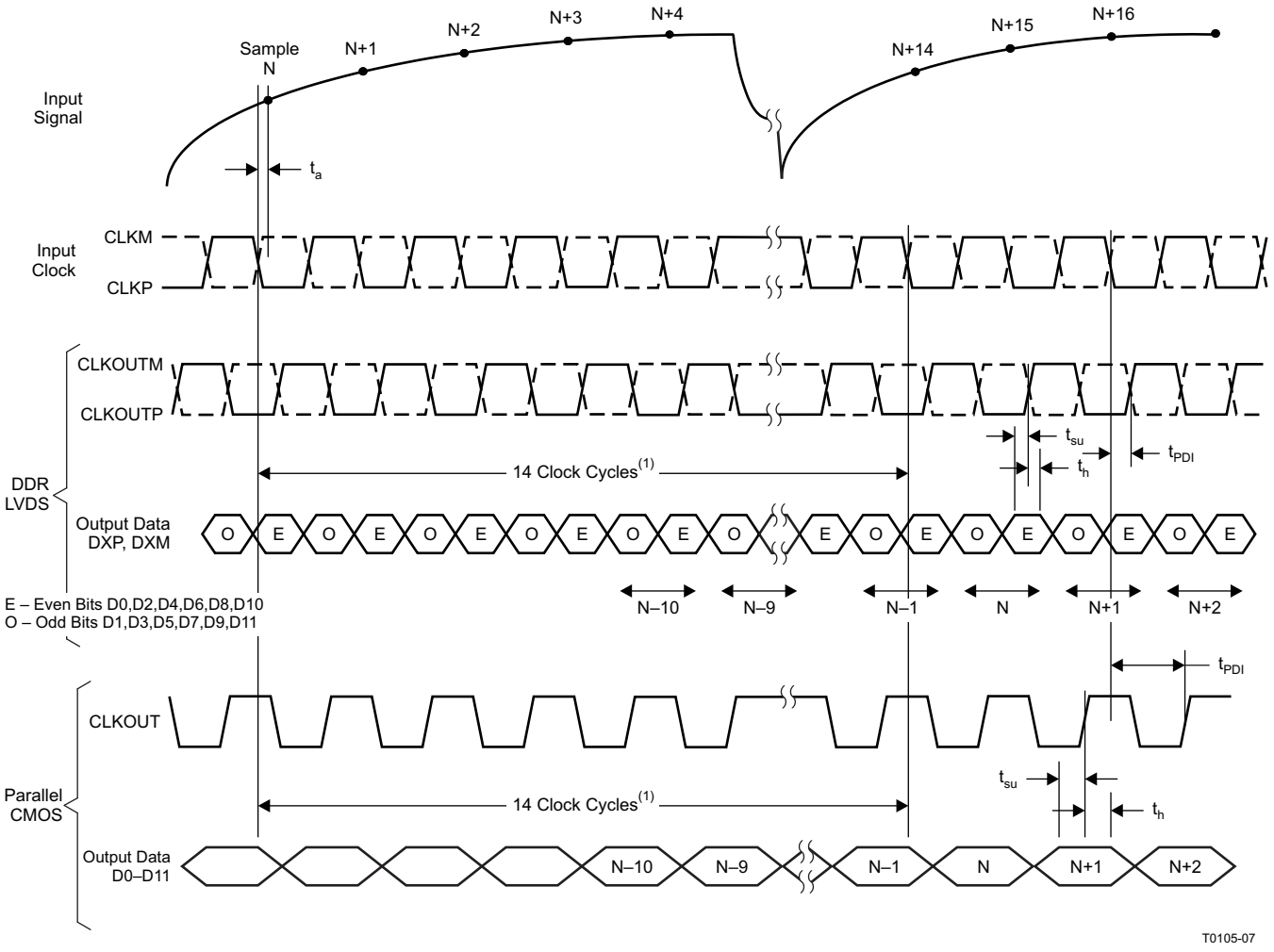
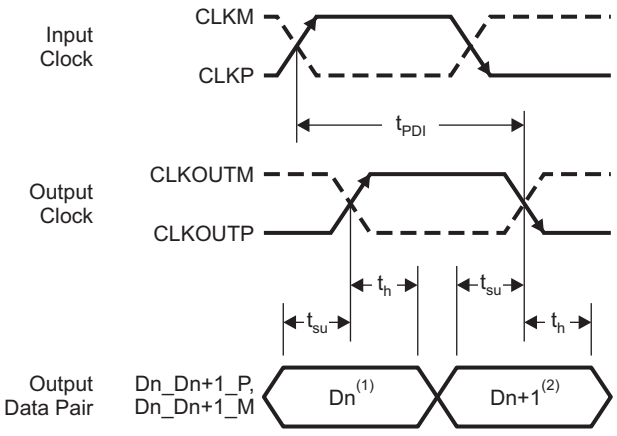


(1) Latency is 10 clock cycles in low-latency mode.

Figure 1. Latency



(1) Dn – Bits D0, D2, D4, D6, D8, D10
(2) Dn+1 – Bits D1, D3, D5, D7, D9, D11

T0106-05

Figure 2. LVDS Mode Timing

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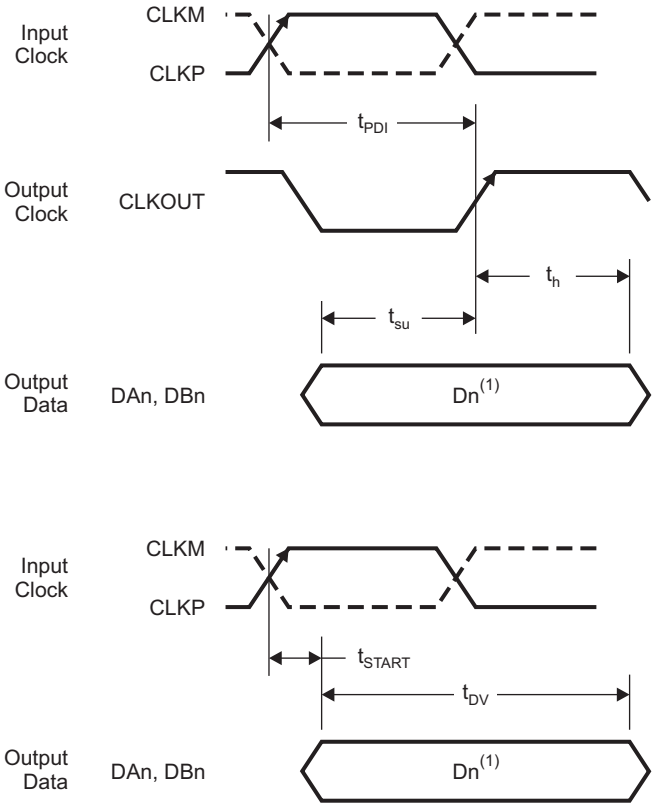
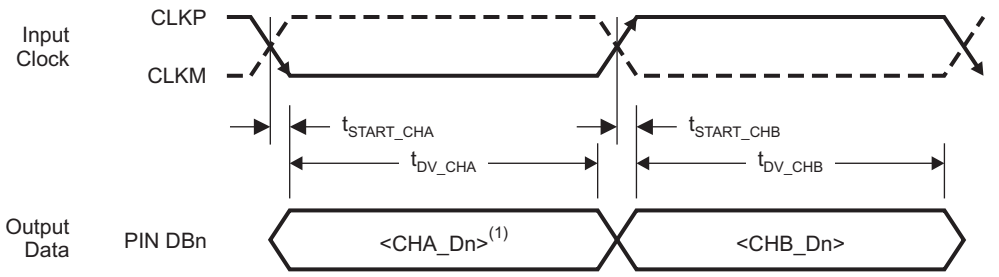


(1) Dn – Bits D0, D1, D2, ... of Channels A and B

T0107-03

Figure 3. CMOS Mode Timing



(1) Dn – Bits D0, D1, D2, ...

T0107-06

Figure 4. Multiplexed Mode Timing (CMOS Only)

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DEVICE CONFIGURATION

ADS62P2X can be configured independently using either parallel interface control or serial interface programming.

USING PARALLEL INTERFACE CONTROL ONLY

To control the device using the parallel interface, keep RESET tied to ***high*** (AVDD). Pins SEN, SCLK, CTRL1, CTRL2 and CTRL3 can be used to directly control certain modes of the ADC. After power-up, the device will automatically get configured as per the parallel pin voltage settings (Table 4 to Table 6).

In this mode, SEN and SCLK function as parallel *analog* control pins, which can be configured using a simple resistor divider (Figure 5). Table 3 has a brief description of the modes controlled by the parallel pins.

Table 3. Parallel Pin Definition

PIN	TYPE OF PIN	CONTROLS MODES
SCLK	Analog control pins (controlled by analog voltage levels, see)	Coarse gain and internal/external reference
SEN		LVDS/CMOS interface and output data format
CTRL1	Digital control pins (controlled by digital logic levels)	Together control various power down modes and MUX mode.
CTRL2		
CTRL3		

USING SERIAL INTERFACE PROGRAMMING ONLY

To program the device using the serial interface, keep RESET low. Pins SEN, SDATA, and SCLK function as serial interface *digital* pins and are used to access the internal registers of ADC. The registers must first be reset to their default values either by applying a pulse on RESET pin or by setting bit <RST> = 1. After reset, the RESET pin must be kept low.

The serial interface section describes the register programming and register reset in more detail. Since the parallel pins (CTRL1, CTRL2, CTRL3) are not used in this mode, they must be tied to ground.

USING BOTH SERIAL INTERFACE and PARALLEL CONTROLS

For increased flexibility, a combination of serial interface registers and parallel pin controls (CTRL1 to CTRL3) can also be used to configure the device. To allow this, keep RESET ***low***.

The parallel interface control pins CTRL1 to CTRL3 are available. After power-up, the device will automatically get configured as per the voltage settings on these pins (Table 6).

SEN, SDATA, and SCLK function as serial interface *digital* pins and are used to access the internal registers of ADC. The registers must first be reset to their default values either by applying a pulse on RESET pin or by setting bit <RST> = 1. After reset, the RESET pin must be kept low. The serial interface section describes the register programming and register reset in more detail.

Since the power down modes can be controlled using both the parallel pins and serial registers, the priority between the two is determined by **<OVRD>** bit. When **<OVRD>** bit = 0, pins CTRL1 to CTRL3 control the power down modes. With **<OVRD>** = 1, register bits **<POWER DOWN>** control these modes, over-riding the pin settings.

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DETAILS OF PARALLEL CONFIGURATION ONLY

The functions controlled by each parallel pin are described below. A simple way of configuring the parallel pins is shown in Figure 5.

Table 4. SCLK (Analog Control Pin)

SCLK	DESCRIPTION
0	0dB gain and internal reference
(3/8)AVDD	0dB gain and external reference
(5/8)2AVDD	3.5dB coarse gain and external reference
AVDD	3.5dB coarse gain and internal reference

Table 5. SEN (Analog Control Pin)

SEN	DESCRIPTION
0	2s complement format and DDR LVDS output
(3/8)AVDD	Straight binary and DDR LVDS output
(5/8)AVDD	Straight binary and parallel CMOS output
AVDD	2s complement format and parallel CMOS output

Table 6. CTRL1, CTRL2 and CTRL3 (Digital Control Pins)

CTRL1	CTRL2	CTRL3	DESCRIPTION
LOW	LOW	LOW	Normal operation
LOW	LOW	HIGH	Channel A output buffer disabled
LOW	HIGH	LOW	Channel B output buffer disabled
LOW	HIGH	HIGH	Channel A and B output buffer disabled
HIGH	LOW	LOW	Channel A and B powered down
HIGH	LOW	HIGH	Channel A standby
HIGH	HIGH	LOW	Channel B standby
HIGH	HIGH	HIGH	MUX mode of operation (only with CMOS interface Channel A and B data is multiplexed and output on DB11 to DB0 pins . See multiplexed output mode for detailed description.

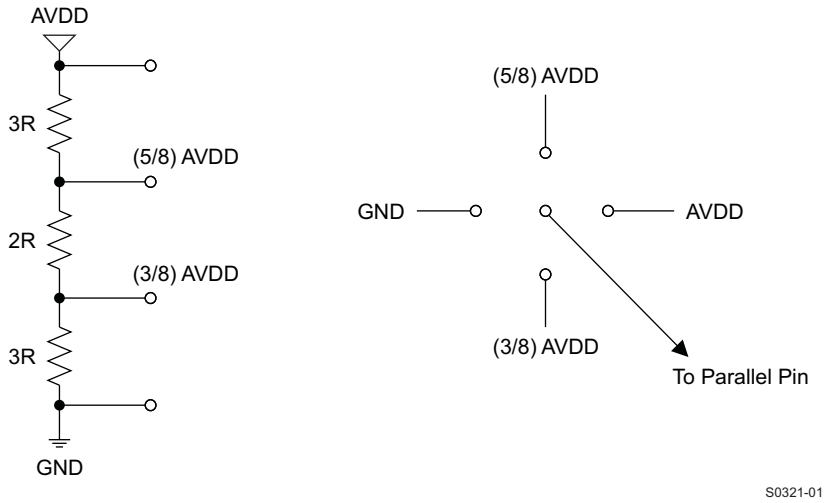

Figure 5. Simple Scheme to Configure Parallel Pins

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SERIAL INTERFACE

The ADC has a set of internal registers, which can be accessed by the serial interface formed by pins SEN (Serial interface Enable), SCLK (Serial Interface Clock) and SDATA (Serial Interface Data).

Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every falling edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 16th SCLK falling edge when SEN is low. In case the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiple of 16-bit words within a single active SEN pulse.

The first 8 bits form the register address and the remaining 8 bits the register data. The interface can work with SCLK frequency from 20 MHz down to low speeds (few Hertz), and also with a non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers ***must*** be initialized to their default values. This can be done in one of two ways:

1. Either through hardware reset by applying a high-going pulse on RESET pin (of width greater than 10 ns) as shown in Figure 6.

   OR

2. By applying software reset. Using the serial interface, set the **<RST>** bit to ***high***. This initializes internal registers to their default values and then self-resets the **<RST>** bit to ***low***. In this case the RESET pin is kept ***low***.

SERIAL INTERFACE TIMING CHARACTERISTICS

Typical values at 25°C, min and max values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3 V, DRVDD = 1.8 V to 3.3 V, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency	> DC		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

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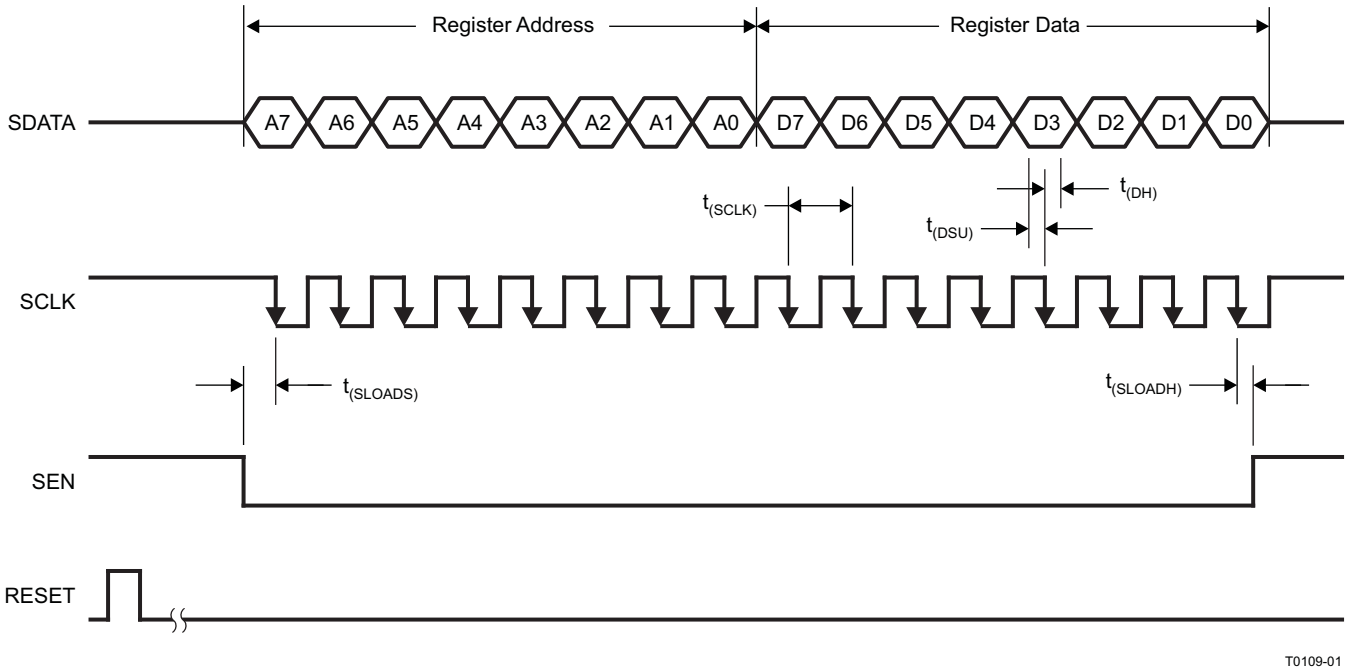
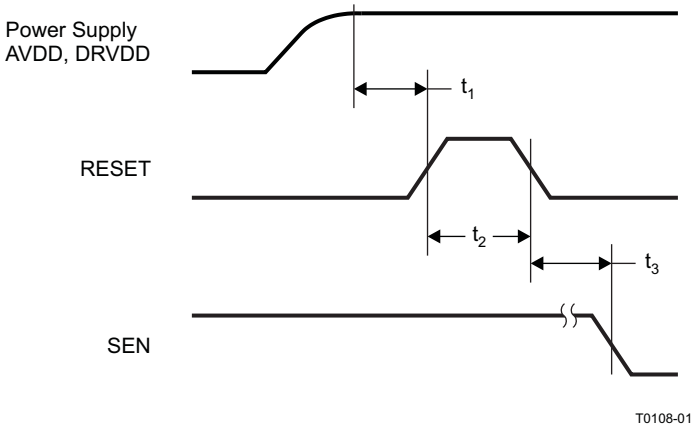


Figure 6. Serial Interface Timing

RESET TIMING

Typical values at 25°C, min and max values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power-up of AVDD and DRVDD to RESET pulse active	5			ms
t_2	Reset pulse width	Pulse width of active RESET signal	10			ns
t_3	Register write delay	Delay from RESET disable to SEN active	25			ns
t_{PO}	Power-up time	Delay from power-up of AVDD and DRVDD to output stable		7		ms



NOTE: A high-going pulse on RESET pin is required in serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET has to be tied permanently HIGH.

Figure 7. Reset Timing Diagram

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SERIAL REGISTER MAP

Table 7. Summary of Functions Supported by Serial Interface(1)

REGISTER ADDRESS	REGISTER FUNCTIONS							
A7–A0 IN HEX	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
00	0	0	0	0	0	0	<RST> *Software Reset*	0
10	<CLKOUT STRENGTH>		0	0	0	0	0	0
11	0	0	<CURRENT DOUBLE> LVDS *buffer current double*		<LVDS CURRENT> *LVDS buffer current programmability*		<DATAOUT STRENGTH>	
12	0	0	<LVDS TERMINATION> *Internal termination programmability*					
13	0	0	0	<OFFSET FREEZE>	0	0	0	0
14	<OVRD> *Over-ride bit*	0	<OUTPUT INTERFACE> *LVDS or CMOS interface*	<COARSE GAIN> 3.5 dB gain	<REF> *Internal/External reference*	<POWER DOWN MODES> and MUX mode		
16	0	0	0	<DATA FORMAT> 2s complement or straight binary	Bit/Byte wise (LVDS only)	<TEST PATTERNS>		
17	0	0	0	0	<FINE GAIN> *0 to 6 dB gain in 0.5 dB steps*			
18	<CUSTOM LOW> *Lower 6 bits*							
19	0	0	<CUSTOM HIGH> *Upper 6 bits*					
1A	<LOW LATENCY>	<OFFSET TC> *Offset correction time constant*			<GAIN CORRECTION> *0 to 0.5 dB, steps of 0.05 dB*			
1B	<OFFSET EN> *Other correction enable*	0	<FILTER COEFF SELECT> *In-built or custom coefficients*	<FILTER ENABLE> *Enable digital filtering*	<ODD TAP ENABLE>	<DECIMATION RATE> *Decimate by 2, 4, 8*		
1D	0	0	0	0	0	0	<DECIMATION FILTER FREQ BANDS>	
1E to 2F	<FILTER COEFFICIENTS> *12 coefficients, each 12 bit signed*							

(1) Multiple functions in a register can be programmed in a single write operation.

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DESCRIPTION OF SERIAL REGISTERS

Table 8.

A7–A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
00	0	0	0	0	0	0	<RST> *Software Reset*	0

D1 **<RST>**
1 Software reset applied – resets all internal registers and self-clears to 0.

Table 9.

A7–A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
10	<CLKOUT STRENGTH>		0	0	0	0	0	0

D7–D6 **<CLKOUT STRENGTH> Output clock buffer drive strength control**
01 WEAKER than default drive
00 DEFAULT drive strength
11 STRONGER than default drive strength (recommended for load capacitances > 5 pF)
10 MAXIMUM drive strength (recommended for load capacitances > 5 pF)

Table 10.

A7–A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
11	0	0	<CURRENT DOUBLE> LVDS buffer current double		LVDS CURRENT> LVDS buffer current programmability		DATAOUT STRENGTH>	

D1–D0 **<DATAOUT STRENGTH> Output data buffer drive strength control**
01 WEAKER than default drive
00 DEFAULT drive strength
11 STRONGER than default drive strength (recommended for load capacitances > 5 pF)
10 MAXIMUM drive strength (recommended for load capacitances > 5 pF)

D3–D2 **<LVDS CURRENT> LVDS Current programmability**
00 3.5 mA
01 2.5 mA
10 4.5 mA
11 1.75 mA

D5–D4 **CURRENT DOUBLE> LVDS Current double control**
00 default current, set by <LVDS CURR>
01 LVDS clock buffer current is doubled, 2x <LVDS CURR>
10 LVDS data and clock buffers current are doubled, 2x <LVDS CURR>
11 unused

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Table 11.

A7–A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
12	0	0	<LVDS TERMINATION> *Internal termination programmability*					

D5–D3 **<LVDS DATA TERM> Internal termination control for data outputs**

000	No internal termination
001	300 Ω
010	180 Ω
011	110 Ω
100	150 Ω
101	100 Ω
110	81 Ω
111	60 Ω

D2–D0 **<LVDS CLK TERM> Internal termination control for clock output**

000	No internal termination
001	300 Ω
010	180 Ω
011	110 Ω
100	150 Ω
101	100 Ω
110	81 Ω
111	60 Ω

Table 12.

A7–A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
13	0	0	0	<OFFSET FREEZE>	0	0	0	0

D4 **<OFFSET FREEZE> Offset correction becomes inactive and the last estimated offset value is used to cancel the offset**

0	Offset correction active
1	Offset correction inactive

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Table 13.

A7–A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
14	<OVRD> *Over-ride bit*	0	<OUTPUT INTERFACE> *LVDS or CMOS interface*	<COARSE GAIN> *3.5 dB gain*	<REF> *Internal / External reference*	<POWER DOWN MODES>		

D2-D0 **<POWER DOWN MODES>**

000 Normal operation

001 Channel A output buffer disabled

010 Channel B output buffer disabled

011 Channel A and B output buffers disabled

100 Global power down

101 Channel A standby

110 Channel B standby

111 Multiplexed mode, **MUX–** (only with CMOS interface)
Channel A and B data is multiplexed and output on DB11 to DB0 pins.

D3 **<REF> Reference mode**

0 Internal reference enabled

1 External reference enabled

D4 **<COARSE GAIN> Coarse gain control**

0 0 dB coarse gain

1 3.5 dB coarse gain

D5 **<OUTPUT INTERFACE> Output interface selection**

0 Parallel CMOS data outputs

1 DDR LVDS data outputs

D7 **<OVRD> Over-ride bit** – the LVDS/CMOS selection, power down and MUX modes can also be controlled using parallel pins. By setting <OVRD> = 1, register bits LVDS <CMOS> and <POWER DOWN MODES> will over-ride the settings of the parallel pins.

0 Disable over-ride

1 Enable over-ride

Table 14.

A7–A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
16	0	0	0	DATA FORMAT> *2s complement or straight binary*	Bit / Byte wise (LVDS only)	<TEST PATTERNS>		

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D2–D0	**<TEST PATTERNS> Test Patterns to verify capture**
000	Normal ADC operation
001	Outputs all zeros
010	Outputs all ones
011	Outputs toggle pattern
100	Outputs digital ramp
101	Outputs custom pattern
110	Unused
111	Unused
D3	**Bit-wise/Byte-wise selection (DDR LVDS mode ONLY)**
0	Bit wise – Odd bits (D1, D3, D5, D7, D9) on CLKOUT rising edge and even bits (D0, D2, D4, D6, D8, D10) on CLKOUT falling edge
1	Byte wise – Lower 7 bits (D0-D6) at CLKOUT rising edge and upper 4 bits (D7-D10) at CLKOUT falling edge
D4	**<DATA FORMAT> Data format selection**
0	2s complement
1	Straight binary

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Table 15.

A7–A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
17	0	0	0	0	<FINE GAIN> *0 to 6 dB gain in 0.5 dB steps*			

D2–D0	<FINE GAIN> Gain programmability in 0.5 dB steps
0000	0 dB gain, default after reset
0001	0.5 dB gain
0010	1.0 dB gain
0011	1.5 dB gain
0100	2.0 dB gain
0101	2.5 dB gain
0110	3.0 dB gain
0111	3.5 dB gain
1000	4.0 dB gain
1001	4.5 dB gain
1010	5.0 dB gain
1011	5.5 dB gain
1100	6.0 dB gain
Others	Unused

Table 16.

A7–A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
18	<CUSTOM LOW> *Lower 6 bits*							
19	0	0	<CUSTOM HIGH> *Upper 6 bits*					

D7-D2 **<CUSTOM LOW>**

6 lower bits of custom pattern available at the output instead of ADC data.

D5-D0 **<CUSTOM HIGH>**

6 upper bits of custom pattern available at the output instead of ADC data.

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Table 17.

A7–A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
1A	<LOW LATENCY>	<OFFSET TC> *Offset correction time constant*			<GAIN CORRECTION> *0 to 0.5 dB, steps of 0.05 dB*			

D2–D0	**<GAIN CORRECTION> Enables fine gain correction in steps of 0.05 dB (same correction applies to both channels)**
0000	0 dB gain, default after reset
0001	+0.5 dB gain
0010	+0.10 dB gain
0011	+0.15 dB gain
0100	+0.20 dB gain
0101	+0.25 dB gain
0110	+0.30 dB gain
0111	+0.35 dB gain
1000	+0.40 dB gain
1001	+0.45 dB gain
1010	+0.5 dB gain

D6-D4	**<OFFSET TC> Time constant of offset correction in number of clock cycles (seconds, for sampling frequency = 125 MSPS)**
000	2^{27} (1.1 s)
001	2^{26} (0.55 s)
010	2^{25} (0.27 s)
011	2^{24} (0.13 s)
100	2^{28} (2.15 s)
101	2^{29} (4.3 s)
110	2^{27} (1.1 s)
111	2^{27} (1.1 s)

D7	**<LOW LATENCY>**
0	Default latency, 14 clock cycles
1	Low latency enabled, 10 clock cycles – Digital Processing Block is bypassed.

Table 18.

A7–A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
1B	<OFFSET Enable> *Offset correction enable*	0	<FILTER COEFF SELECT> *In-built or custom coefficients*	<FILTER Enable> *Enable digital filtering*	<ODD TAP Enable>	<DECIMATION RATE> *Decimate by 2,4,8*		

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D2-D0	**<DECIMATION RATE>** Decimation filters
000	Decimate by 2 (pre-defined or user coefficients can be used)
001	Decimate by 4 (pre-defined or user coefficients can be used)
011	No decimation (pre-defined coefficients are disabled, only custom coefficients are available)
100	Decimate by 8 (only custom coefficients are available)
D3	**<ODD TAP ENABLE>**
0	Even taps enabled (24 coefficients)
1	0 Odd taps enabled (23 coefficients)
D4	**<FILTER ENABLE>**
0	Digital filter bypassed
1	Digital filtering enabled
D5	**<FILTER COEFF SELECT>**
0	Pre-defined coefficients are loaded in the filter
1	User-defined coefficients are loaded in the filter (coefficients have to be loaded in registers – to -)
D7	**<OFFSET Enable>**
0	Offset correction disabled
1	Offset correction enabled

Table 19.

A7–A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
1D	0	0	0	0	0	0	<DECIMATION FILTER FREQ BANDS>	

D1-D0	**<DECIMATION FILTER FREQ BAND>** Decimation filters
	With decimate by 2, **<DECIMATION RATE>** = 000:
00	Low-pass filter (–6 dB frequency at Fs/4)
01	High-pass filter (–6 dB frequency at Fs/4)
10, 11	Unused
	With decimate by 4, **<DECIMATION RATE>** = 001:
00	Low-pass filter (-3 dB frequency at Fs/8)
01	Band-pass filter (center frequency at 3Fs/16)
10	Band-pass filter (center frequency at 5Fs/16)
11	High-pass filter (-3 dB frequency at 3Fs/8)

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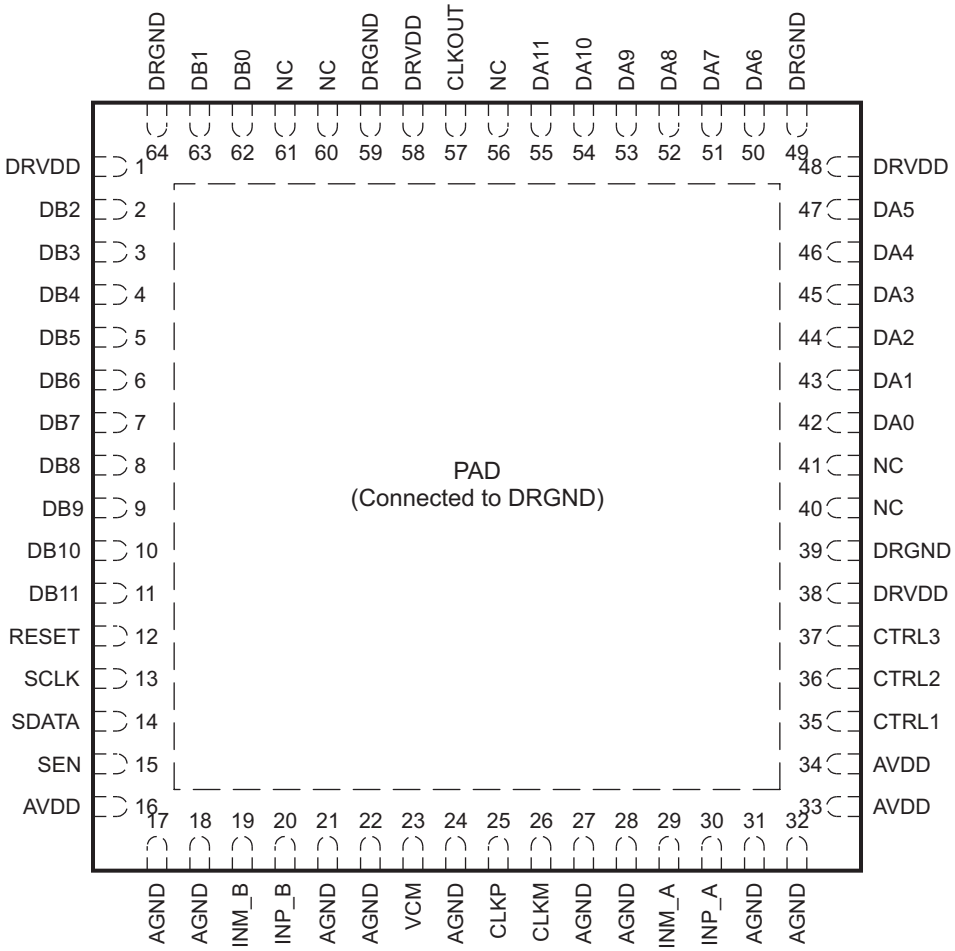
PIN CONFIGURATION (CMOS MODE)

RGC PACKAGE
(TOP VIEW)



P0056-11

Pin Assignments (CMOS INTERFACE)

PIN NAME	DESCRIPTION	PIN NUMBER	NUMBER OF PINS
AVDD	Analog power supply	16, 33, 34	3
AGND	Analog ground	17, 18, 21, 22, 24, 27, 28, 31, 32	9
CLKP, CLKM	Differential input clock	25, 26	2
INM_A, INP_A	Differential input signal – channel A. When not used, the analog input pins (INP_A, INM_A) MUST be tied to VCM and CANNOT be floated.	29, 30	2
INM_B, INP_B	Differential input signal – channel B. When not used, the analog input pins (INP_A, INM_A) MUST be tied to VCM and CANNOT be floated.	19, 20	2
VCM	Internal reference mode – Common-mode voltage output. External reference mode – Reference input. The voltage forced on this pin sets the ADC internal references.	23	1
RESET	Serial interface RESET input. In serial interface mode, the user ***must*** initialize internal registers through hardware RESET by applying a high-going pulse on this pin or by using software reset (refer to Serial Interface section). In parallel interface mode, the user has to tie RESET pin permanently ***high***. (SCLK, SDATA and SEN are used as parallel pin controls in this mode) The pin has an internal 100 kΩ pull-down resistor.	12	1
SCLK	This pin functions as serial interface clock input when RESET is ***low***. It functions as analog control pin when RESET is tied ***high*** and controls coarse gain and internal/external reference selection. See Table 4 for details. The pin has an internal pull-down resistor to ground.	13	1
SDATA	This pin functions as serial interface data input when RESET is low. The pin has an internal pull-down resistor to ground.	14	1

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Pin Assignments (CMOS INTERFACE) (continued)

PIN NAME	DESCRIPTION	PIN NUMBER	NUMBER OF PINS
SEN	This pin functions as serial interface enable input when RESET is ***low***. It functions as analog control pin when RESET is tied ***high*** and controls the output interface (LVDS/CMOS) and data format selection. See Table 5 for details. The pin has an internal pull-up resistor to AVDD.	15	1
CTRL1	These are digital logic input pins. Together they control various power down and multiplexed mode. see Table 6 for details	35	1
CTRL2		36	1
CTRL3		37	1
DA11 to DA0	Channel A 12-bit data outputs, CMOS	42-47, 50-55	12
DB11 to DB0	Channel B 12-bit data outputs, CMOS	62-63, 2-11	12
CLKOUT	CMOS output clock	57	1
DRVDD	Digital supply	1, 38, 48, 58	4
DRGND	Digital ground	39, 49, 59, 64 and PAD	4
PAD	Digital ground. Solder the pad to the digital ground on the board using multiple vias for good electrical and thermal performance.	–	1
NC	Do not connect	40,41,60,61,56	5

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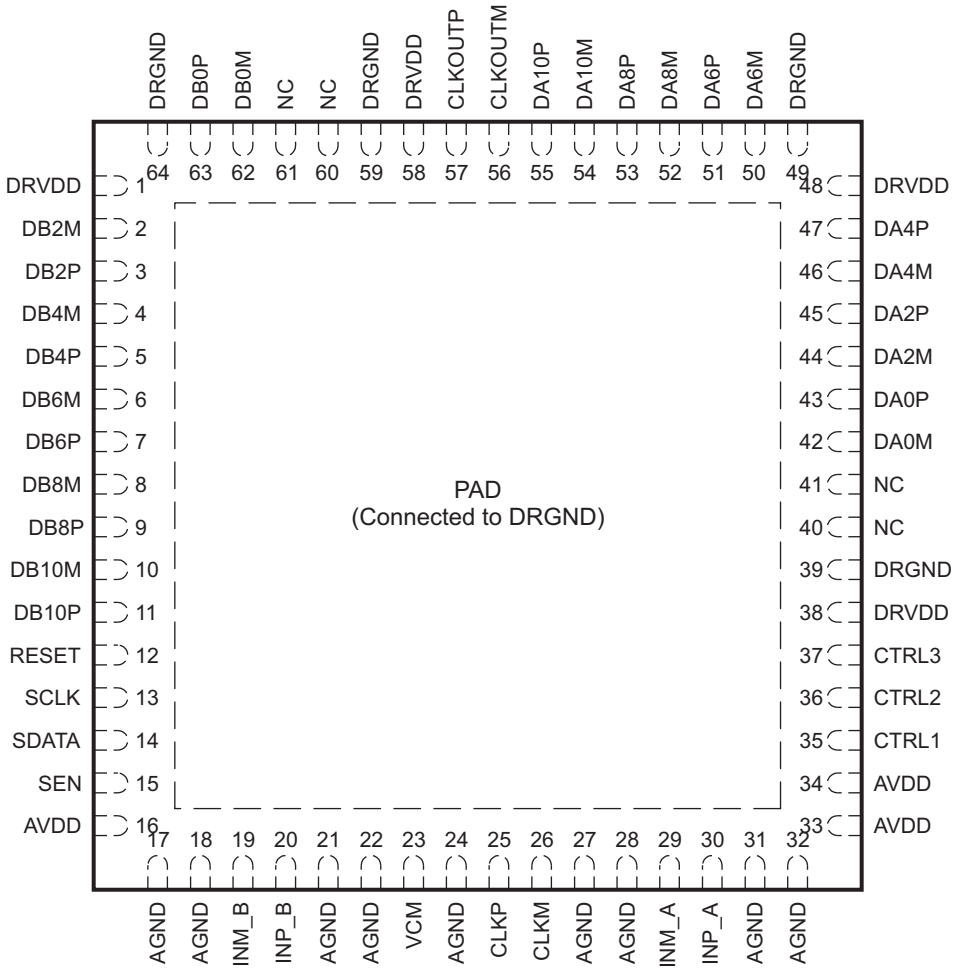
PIN CONFIGURATION (LVDS MODE)

RGC PACKAGE
(TOP VIEW)



P0056-12

Pin Assignments (LVDS INTERFACE)

PIN NAME	DESCRIPTION	PIN NUMBER	NUMBER OF PINS
AVDD	Analog power supply	16, 33, 34	3
AGND	Analog ground	17, 18, 21, 22, 24, 27, 28, 31,32	9
CLKP, CLKM	Differential input clock	25, 26	2
INM_A, INP_A	Differential input signal – Channel A. When not used, the analog input pins (INP_A, INM_A) MUST be tied to VCM and CANNOT be floated.	29, 30	2
INM_B, INP_B	Differential input signal – Channel B. When not used, the analog input pins (INP_B, INM_B) MUST be tied to VCM and CANNOT be floated	19, 20	2
VCM	Internal reference mode – Common-mode voltage output. External reference mode – Reference input. The voltage forced on this pin sets the ADC internal references.	23	1
RESET	Serial interface RESET input. In serial interface mode, the user ***must*** initialize internal registers through hardware RESET by applying a high-going pulse on this pin or by using software reset (refer to Serial Interface section). In parallel interface mode, the user has to tie RESET pin permanently ***high***. (SCLK, SDATA and SEN are used as parallel pin controls in this mode) The pin has an internal 100 kΩ pull-down resistor.	12	1

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Pin Assignments (LVDS INTERFACE) (continued)

PIN NAME	DESCRIPTION	PIN NUMBER	NUMBER OF PINS
SCLK	This pin functions as serial interface clock input when RESET is ***low***. It functions as analog control pin when RESET is tied ***high*** and controls coarse gain and internal/external reference selection. See Table 4 for details. The pin has an internal pull-down resistor to ground.	13	1
SDATA	This pin functions as serial interface data input when RESET is low. The pin has an internal pull-down resistor to ground.	14	1
SEN	This pin functions as serial interface enable input when RESET is ***low***. It functions as analog control pin when RESET is tied ***high*** and controls the output interface (LVDS/CMOS) and data format selection. See Table 5 for details. The pin has an internal pull-up resistor to AVDD.	15	1
CTRL1	These are digital logic input pins. Together they control various power down and multiplexed mode. See Table 6 for details.	35	1
CTRL2		36	1
CTRL3		37	1
DA0P	Channel A Differential output data D0 and D1 multiplexed, true	43	1
DA0M	Channel A Differential output data D0 and D1 multiplexed, complement	42	1
DA2P	Channel A Differential output data D2 and D3 multiplexed, true	45	1
DA2M	Channel A Differential output data D2 and D3 multiplexed, complement	44	1
DA4P	Channel A Differential output data D4 and D5 multiplexed, true	47	1
DA4M	Channel A Differential output data D4 and D5 multiplexed, complement	46	1
DA6P	Channel A Differential output data D6 and D7 multiplexed, true	51	1
DA6M	Channel A Differential output data D6 and D7 multiplexed, complement	50	1
DA8P	Channel A Differential output data D8 and D9 multiplexed, true	53	1
DA8M	Channel A Differential output data D8 and D9 multiplexed, complement	52	1
DA10P	Channel A Differential output data D10 and D11 multiplexed, true	55	1
DA10M	Channel A Differential output data D10 and D11 multiplexed, complement	54	1
CLKOUTP	Differential output clock, true	57	1
CLKOUTM	Differential output clock, complement	56	1
DB0P	Channel B Differential output data D0 and D1 multiplexed, true	63	1
DB0M	Channel B Differential output data D0 and D1 multiplexed, complement	62	1
DB2P	Channel B Differential output data D2 and D3 multiplexed, true	3	1
DB2M	Channel B Differential output data D2 and D3 multiplexed, complement	2	1
DB4P	Channel B Differential output data D4 and D5 multiplexed, true	5	1
DB4M	Channel B Differential output data D4 and D5 multiplexed, complement	4	1
DB6P	Channel B Differential output data D6 and D7 multiplexed, true	7	1
DB6M	Channel B Differential output data D6 and D7 multiplexed, complement	6	1
DB8P	Channel B Differential output data D8 and D9 multiplexed, true	9	1
DB8M	Channel B Differential output data D8 and D9 multiplexed, complement	8	1
DB10P	Channel B Differential output data D10 and D11 multiplexed, true	11	1
DB10M	Channel B Differential output data D10 and D11 multiplexed, complement	10	1
DRVDD	Digital supply	1, 38, 48, 58	4
DRGND	Digital ground	39, 49, 59, 64 and PAD	4
PAD	Digital ground. Solder the pad to the digital ground on the board using multiple vias for good electrical and thermal performance.	–	1
NC	Do not connect	40, 41, 60, 61	4

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TYPICAL CHARACTERISTICS - ADS62P25 (F_S= 125 MSPS)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

FFT for 20 MHz INPUT SIGNAL

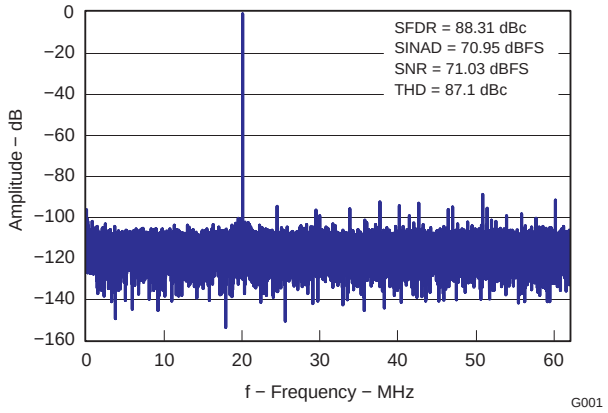

Figure 8.

FFT for 70 MHz INPUT SIGNAL

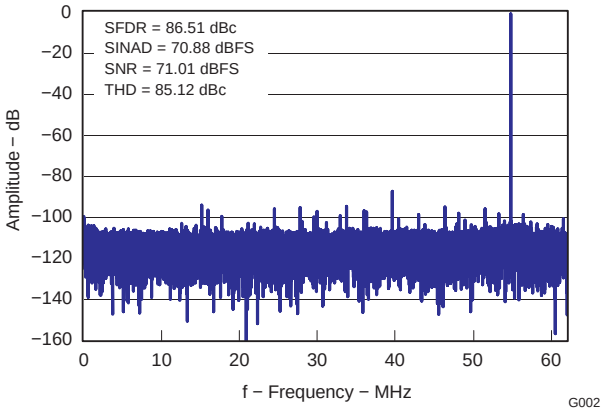

Figure 9.

FFT for 190 MHz INPUT SIGNAL

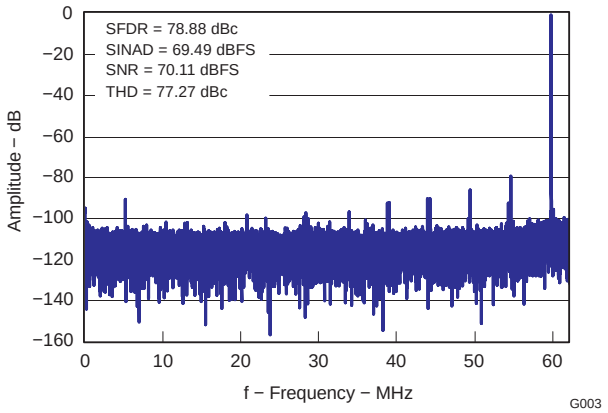

Figure 10.

INTERMODULATION DISTORTION (IMD) vs FREQUENCY

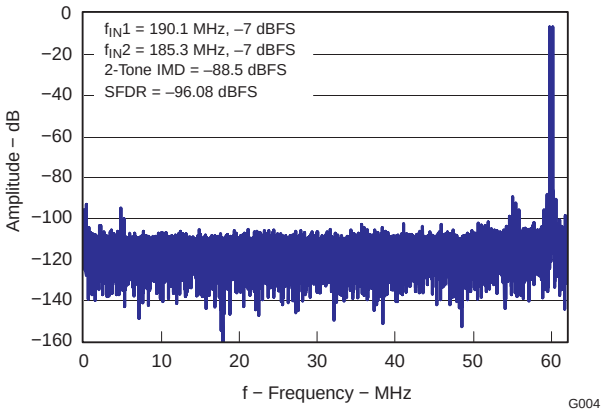

Figure 11.

SFDR vs INPUT FREQUENCY

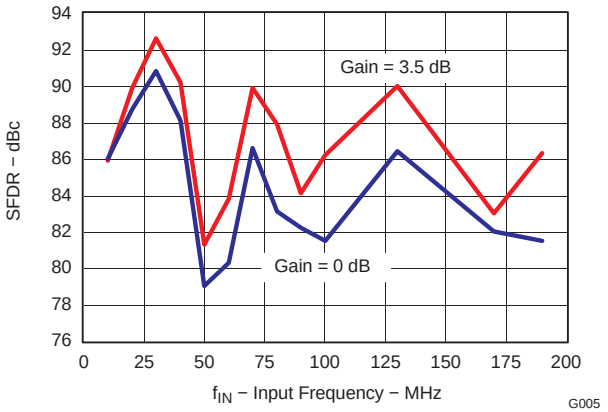

Figure 12.

SNR vs INPUT FREQUENCY

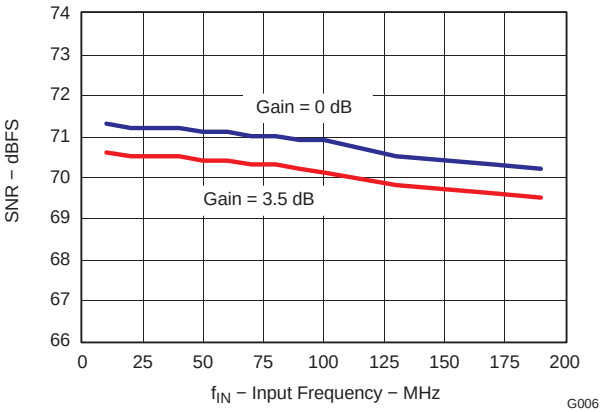

Figure 13.

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TYPICAL CHARACTERISTICS - ADS62P25 (F_S= 125 MSPS) (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

SFDR vs INPUT FREQUENCY (LVDS interface)

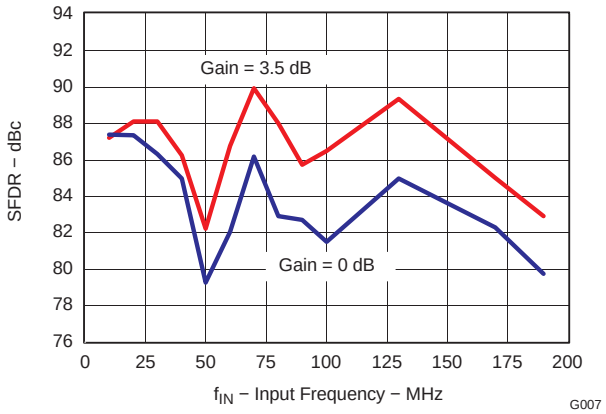

Figure 14.

SFDR vs INPUT FREQUENCY ACROSS GAIN

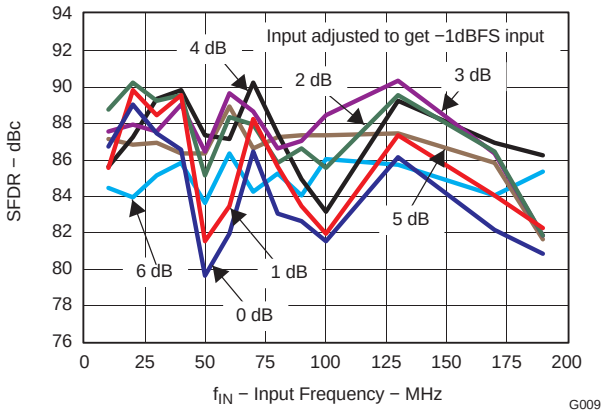

Figure 15.

SINAD vs INPUT FREQUENCY ACROSS GAIN

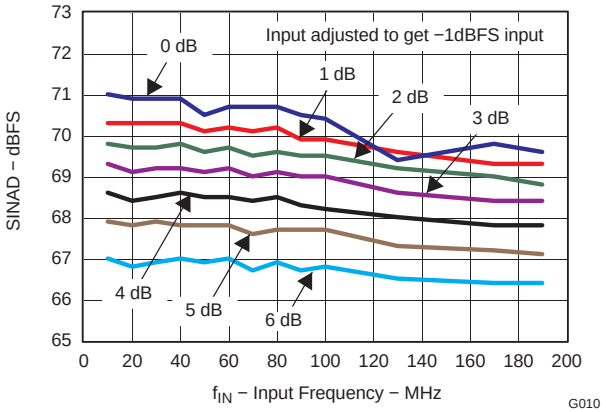

Figure 16.

PERFORMANCE vs AVDD

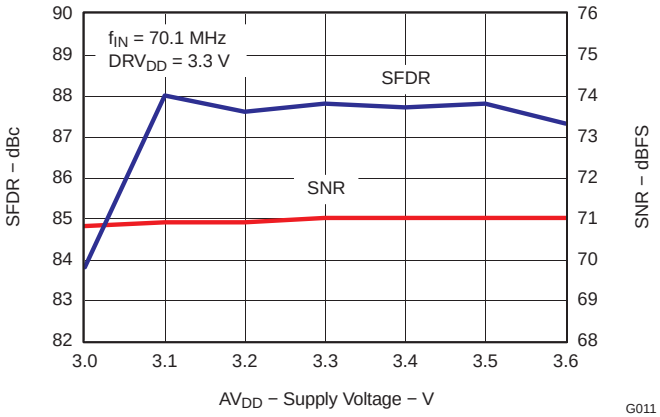

Figure 17.

PERFORMANCE vs DRVDD

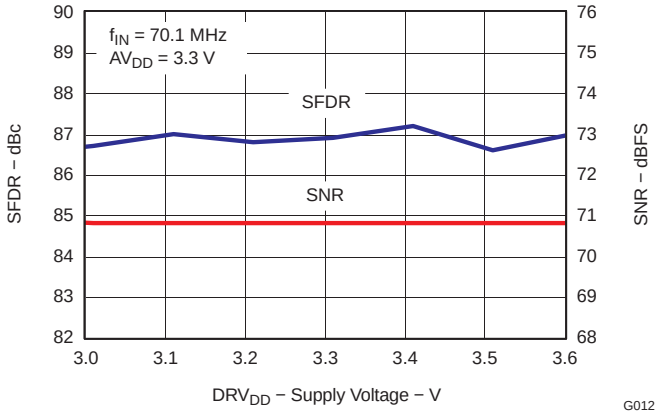

Figure 18.

PERFORMANCE vs TEMPERATURE

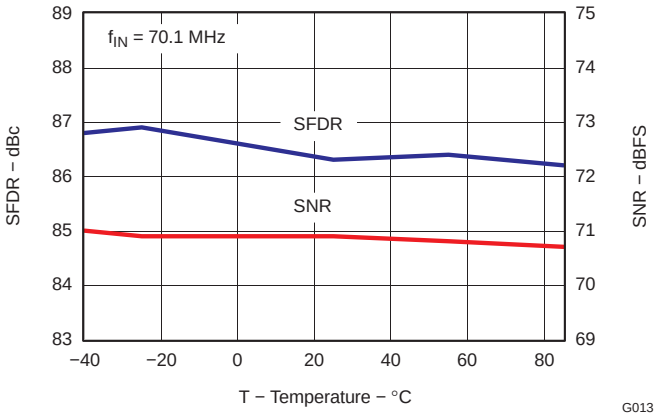

Figure 19.

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TYPICAL CHARACTERISTICS - ADS62P25 (F_S= 125 MSPS) (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

PERFORMANCE vs INPUT AMPLITUDE

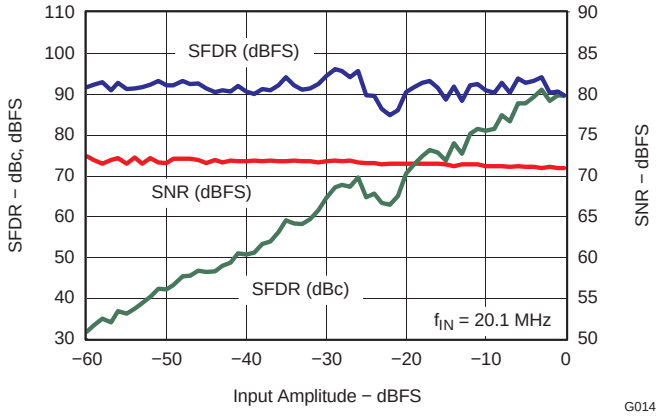

Figure 20.

PERFORMANCE vs CLOCK AMPLITUDE

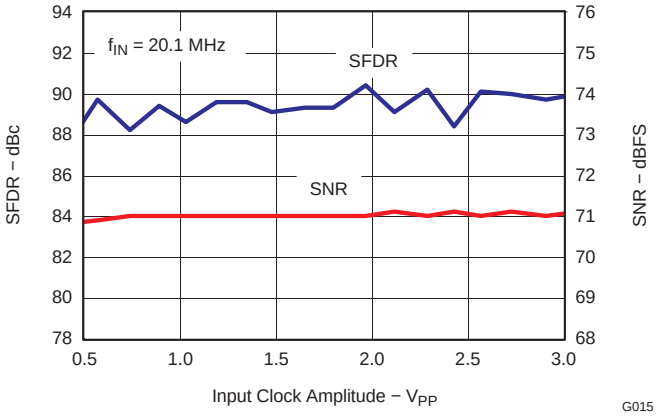

Figure 21.

PERFORMANCE vs INPUT CLOCK DUTY CYCLE

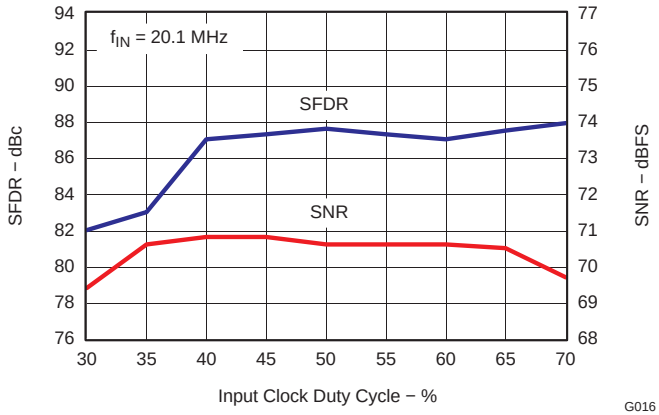

Figure 22.

OUTPUT NOIL HISTOGRAM (INPUTS TIED TO COMMON-MODE)

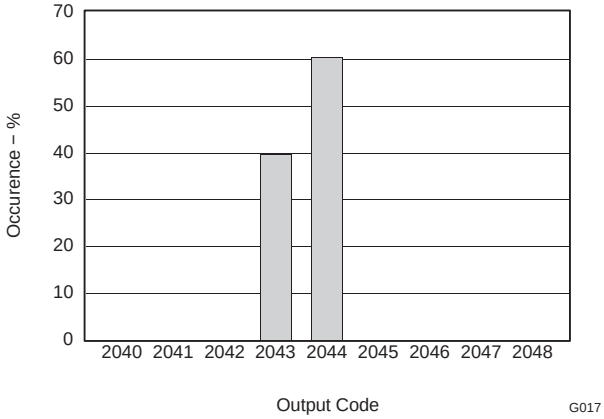

Figure 23.

PERFORMANCE IN EXTERNAL REFERENCE MODE

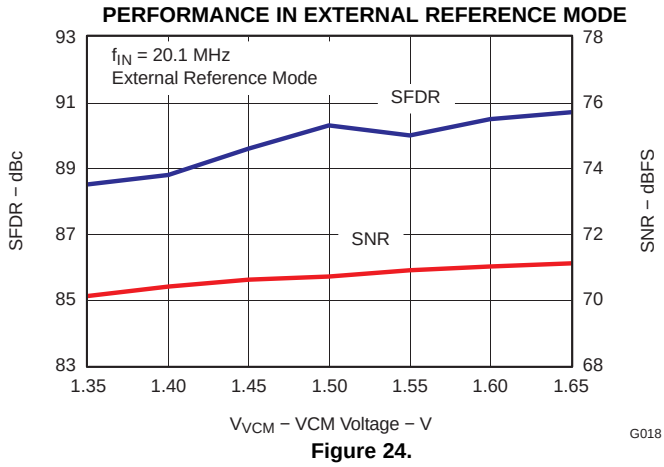

Figure 24.

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TYPICAL CHARACTERISTICS - ADS62P24 (F_S= 105 MSPS)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

FFT for 20 MHz INPUT SIGNAL

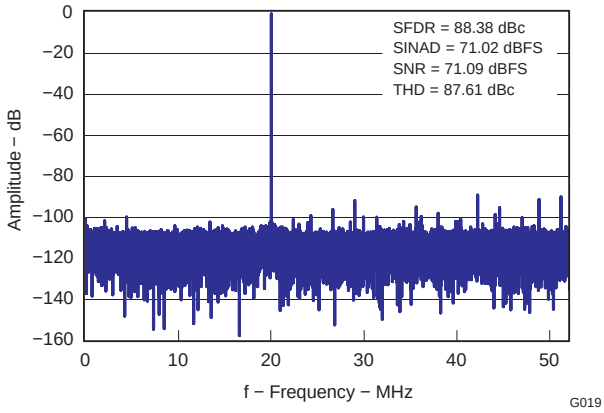

Figure 25.

FFT for 70 MHz INPUT SIGNAL

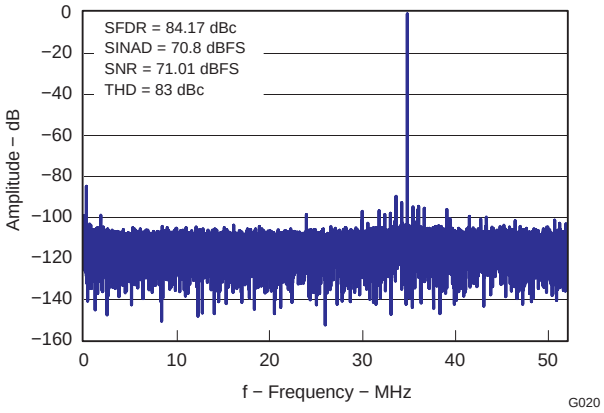

Figure 26.

FFT for 190 MHz INPUT SIGNAL

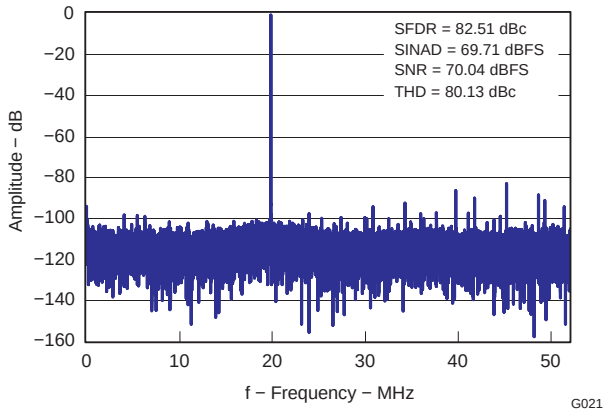

Figure 27.

INTERMODULATION DISTORTION (IMD) vs FREQUENCY

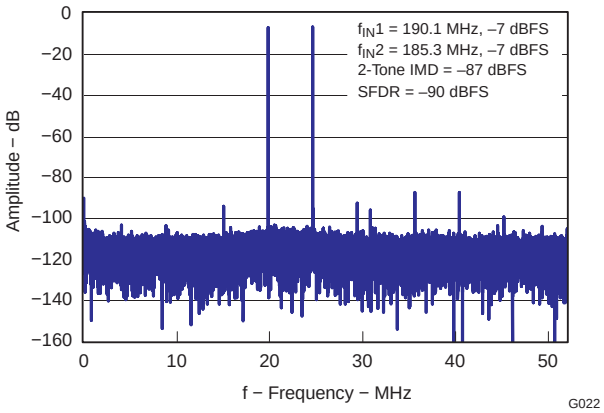

Figure 28.

SFDR vs INPUT FREQUENCY

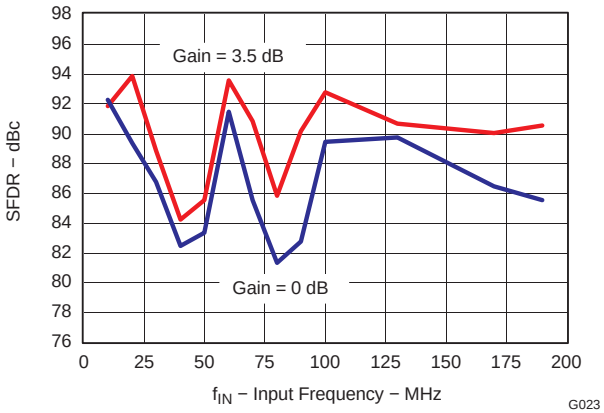

Figure 29.

SNR vs INPUT FREQUENCY

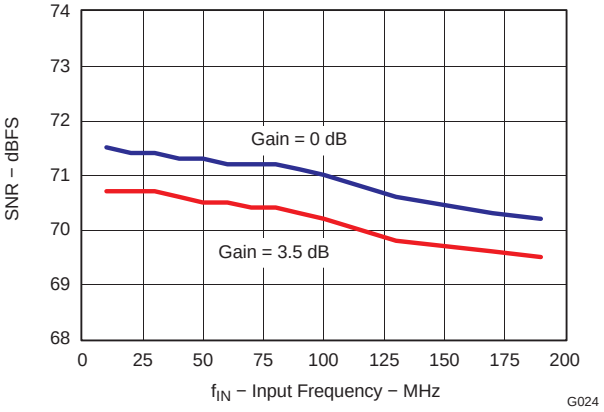

Figure 30.

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TYPICAL CHARACTERISTICS - ADS62P24 (F_S= 105 MSPS) (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

SFDR vs INPUT FREQUENCY (LVDS interface)

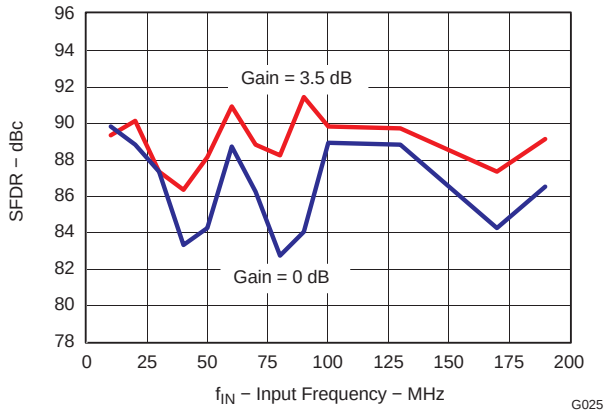

Figure 31.

SFDR vs INPUT FREQUENCY ACROSS GAIN

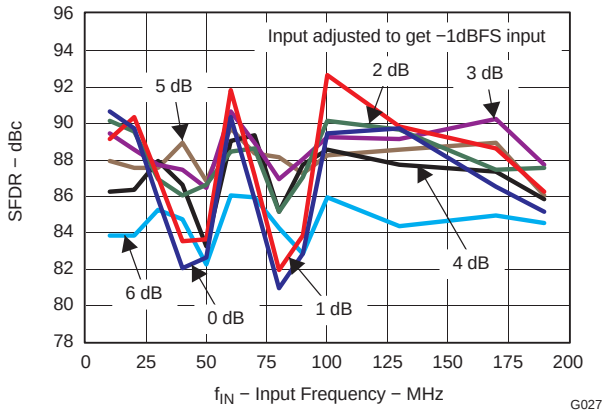

Figure 32.

SINAD vs INPUT FREQUENCY ACROSS GAIN

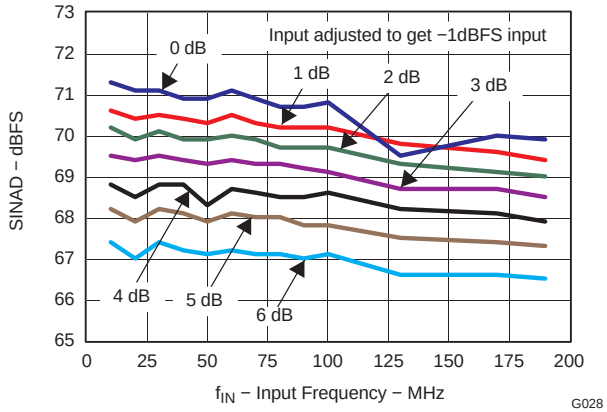

Figure 33.

PERFORMANCE vs AVDD

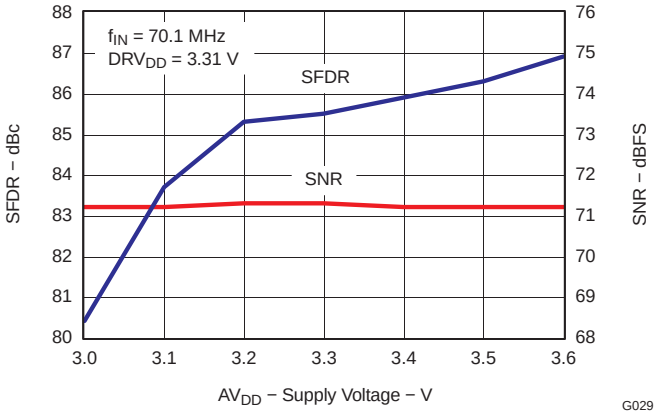

Figure 34.

PERFORMANCE vs DRVDD

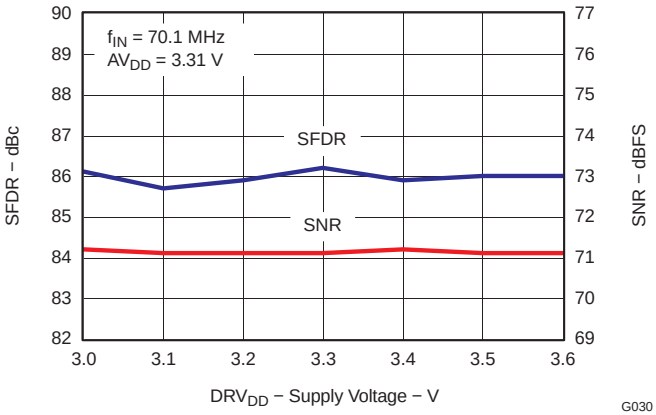

Figure 35.

PERFORMANCE vs TEMPERATURE

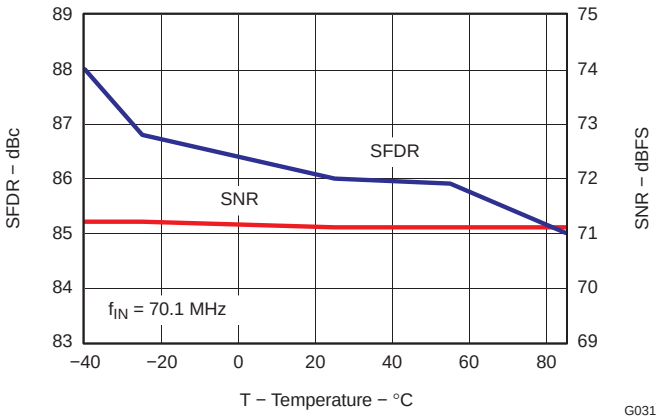

Figure 36.

TYPICAL CHARACTERISTICS - ADS62P24 (F_S= 105 MSPS) (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

PERFORMANCE vs INPUT AMPLITUDE

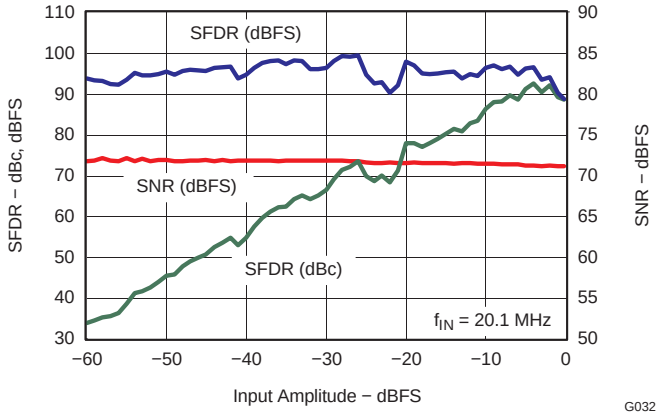

Figure 37.

PERFORMANCE vs CLOCK AMPLITUDE

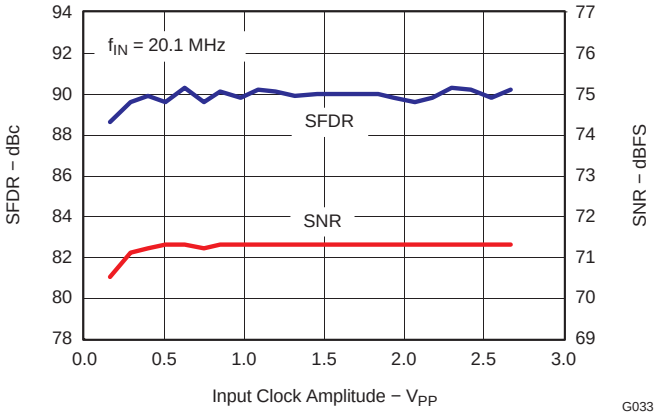

Figure 38.

PERFORMANCE vs INPUT CLOCK DUTY CYCLE

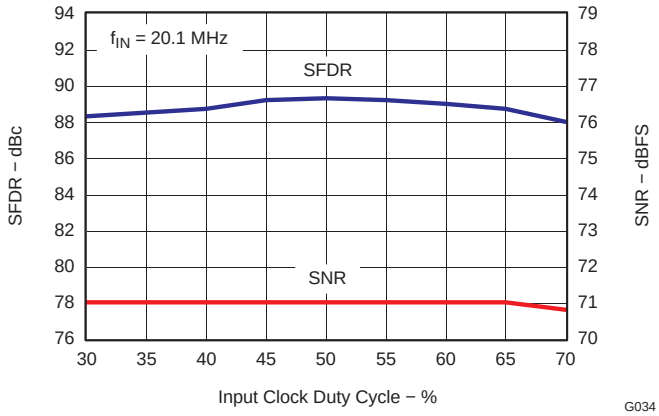

Figure 39.

OUTPUT NOISE HISTOGRAM WITH INPUTS TIED TO COMMON-MODE

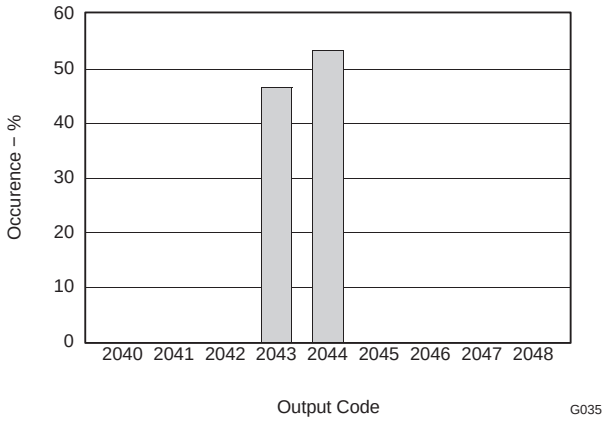

Figure 40.

PERFORMANCE IN EXTERNAL REFERENCE MODE

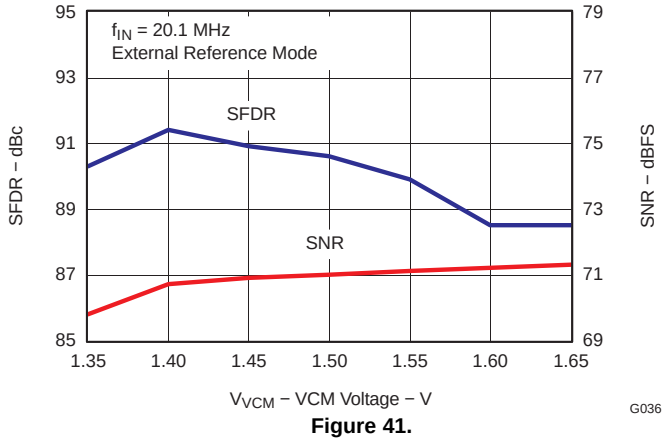

Figure 41.

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TYPICAL CHARACTERISTICS - ADS62P23 (F_S= 80 MSPS)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

FFT for 20 MHz INPUT SIGNAL

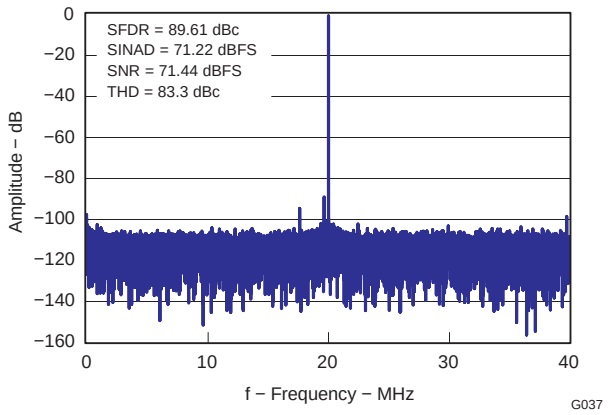

Figure 42.

FFT for 70 MHz INPUT SIGNAL

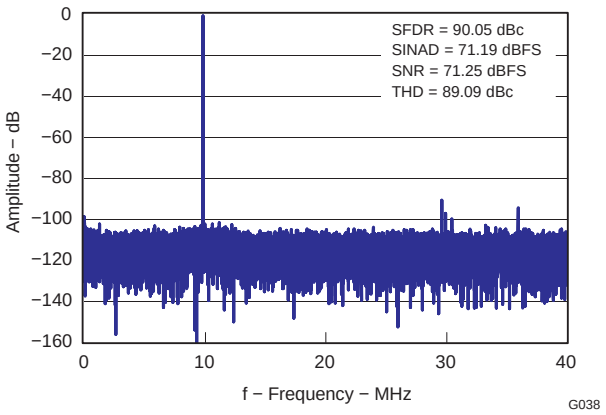

Figure 43.

FFT for 190 MHz INPUT SIGNAL

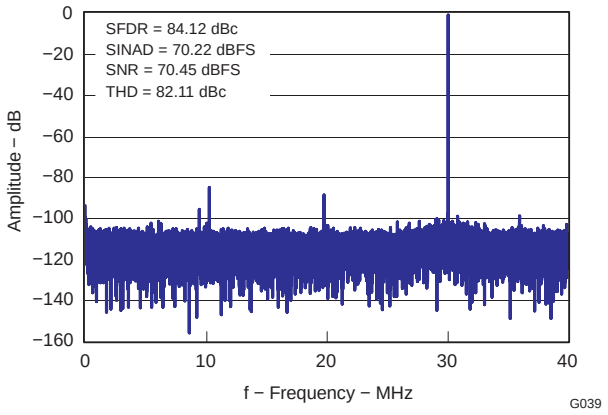

Figure 44.

INTERMODULATION DISTORTION (IMD) vs FREQUENCY

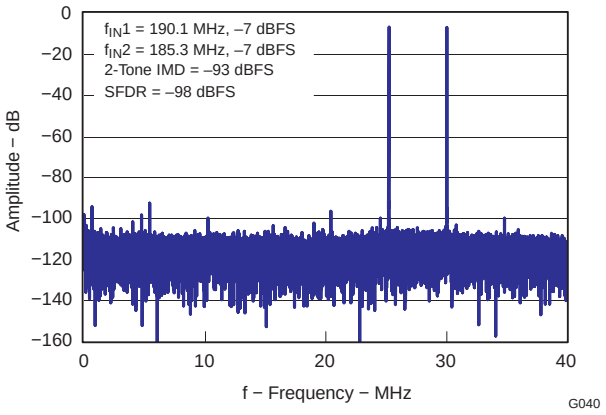

Figure 45.

SFDR vs INPUT FREQUENCY

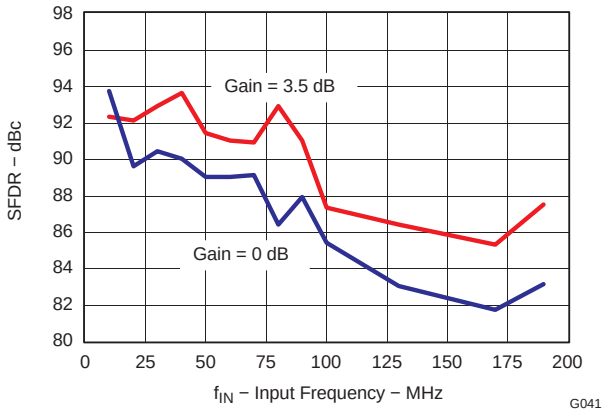

Figure 46.

SNR vs INPUT FREQUENCY

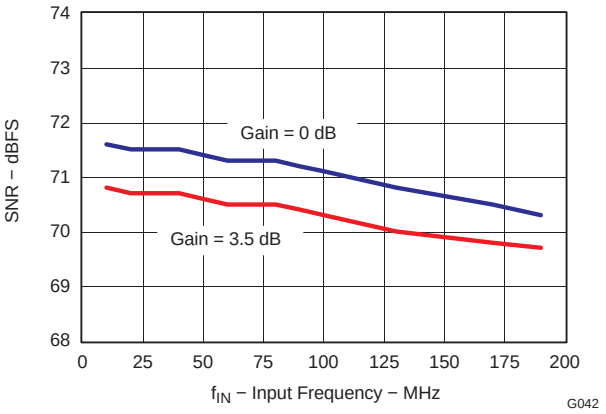

Figure 47.

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TYPICAL CHARACTERISTICS - ADS62P23 (F_S= 80 MSPS) (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

SFDR vs INPUT FREQUENCY (LVDS interface)

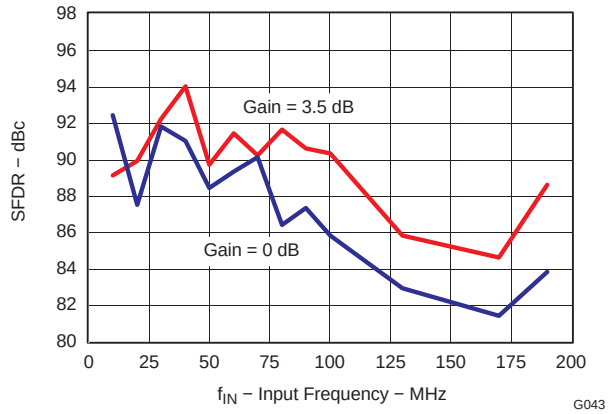

Figure 48.

SFDR vs INPUT FREQUENCY ACROSS GAIN

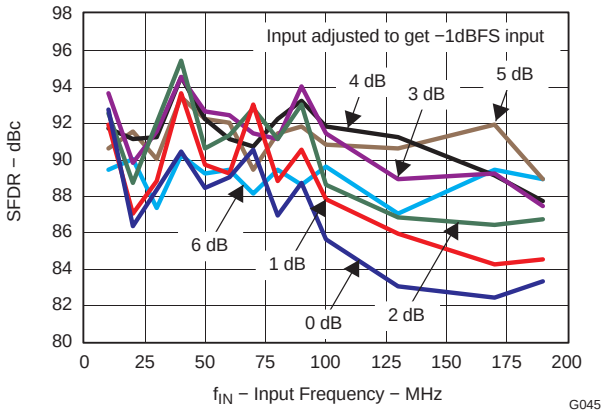

Figure 49.

SINAD vs INPUT FREQUENCY ACROSS GAIN

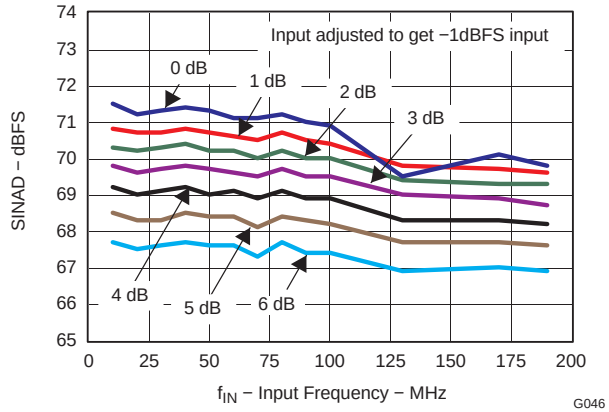

Figure 50.

PERFORMANCE vs AVDD

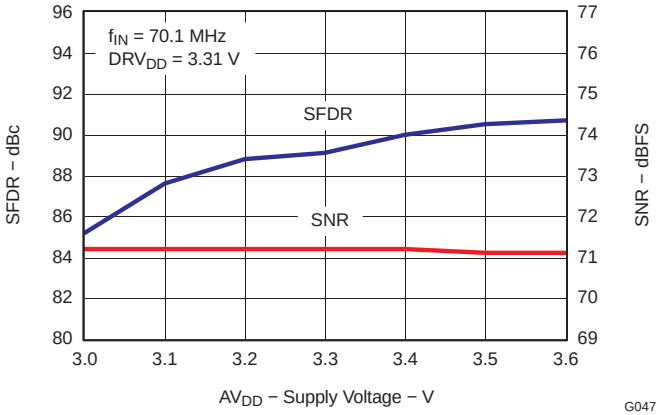

Figure 51.

PERFORMANCE vs DRVDD

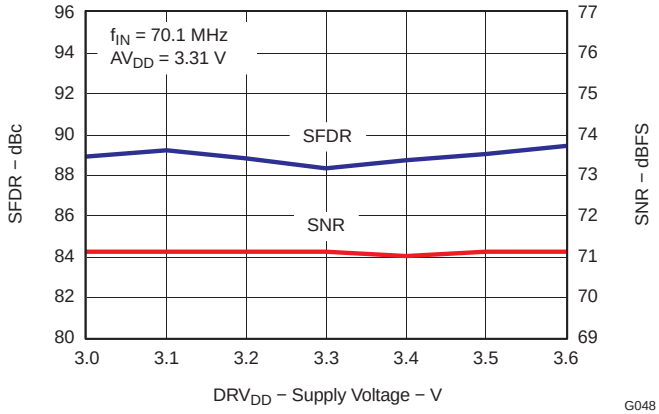

Figure 52.

PERFORMANCE vs TEMPERATURE

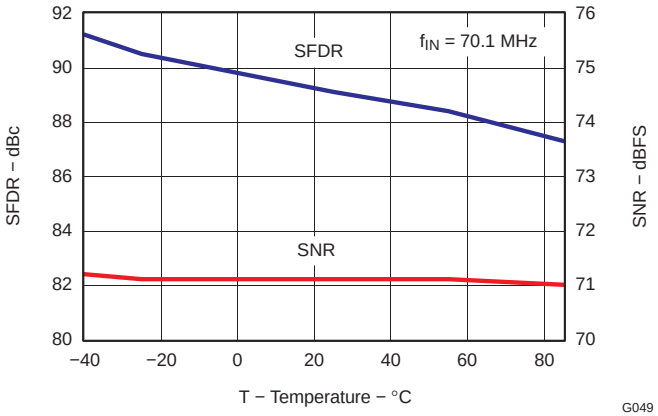

Figure 53.

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TYPICAL CHARACTERISTICS - ADS62P23 (F_S= 80 MSPS) (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

PERFORMANCE vs INPUT AMPLITUDE

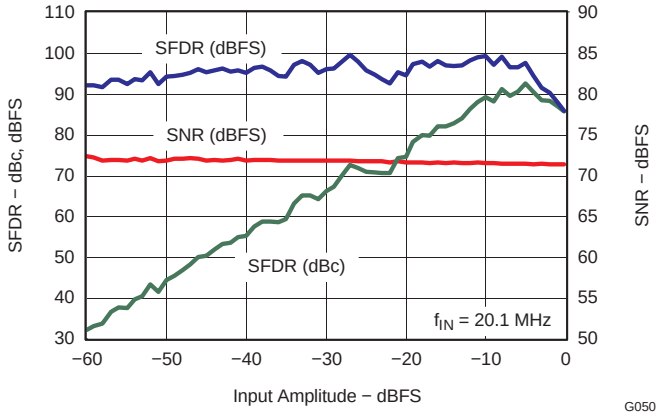

Figure 54.

PERFORMANCE vs CLOCK AMPLITUDE

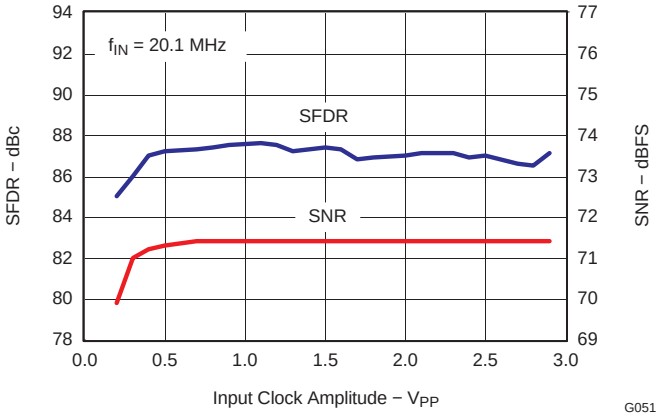

Figure 55.

PERFORMANCE vs INPUT CLOCK DUTY CYCLE

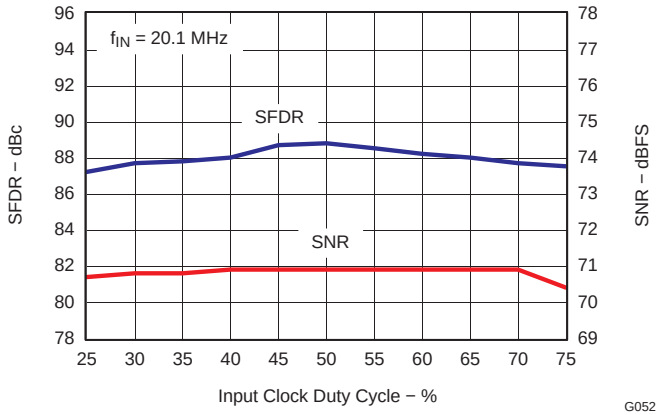

Figure 56.

OUTPUT NOISE HISTOGRAM WITH INPUTS TIED TO COMMON-MODE

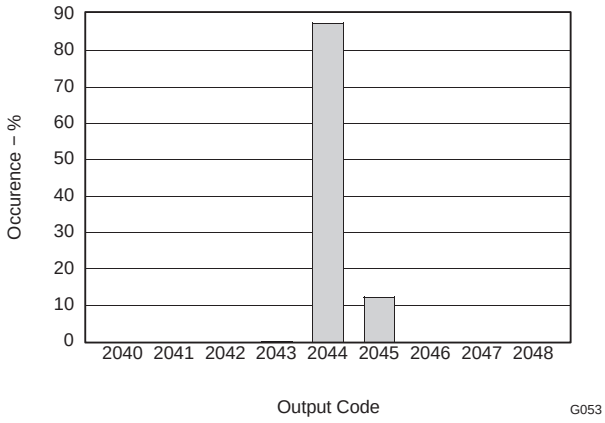

Figure 57.

PERFORMANCE IN EXTERNAL REFERENCE MODE

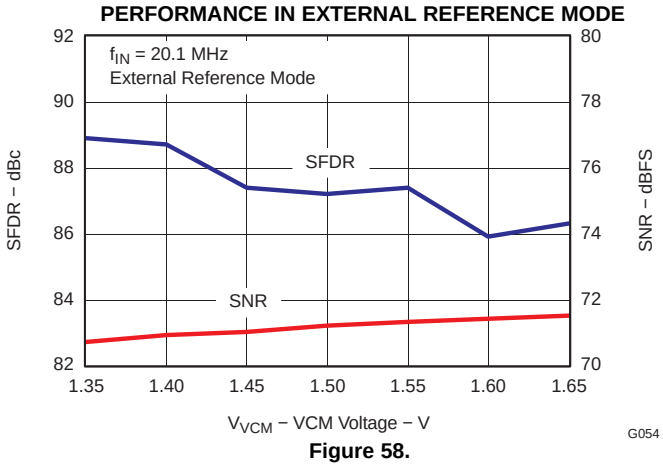

Figure 58.

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TYPICAL CHARACTERISTICS - ADS62P22 (F_S= 65 MSPS)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

FFT for 20 MHz INPUT SIGNAL

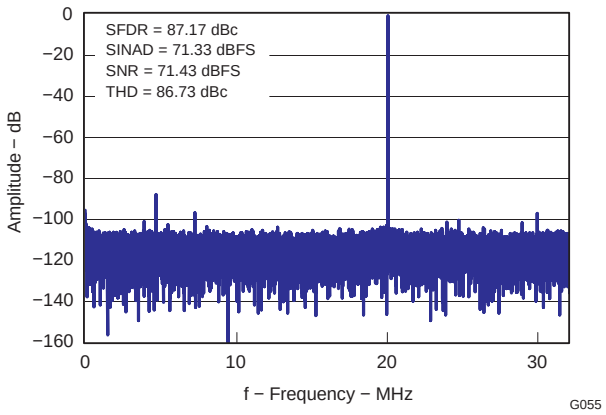

Figure 59.

FFT for 70 MHz INPUT SIGNAL

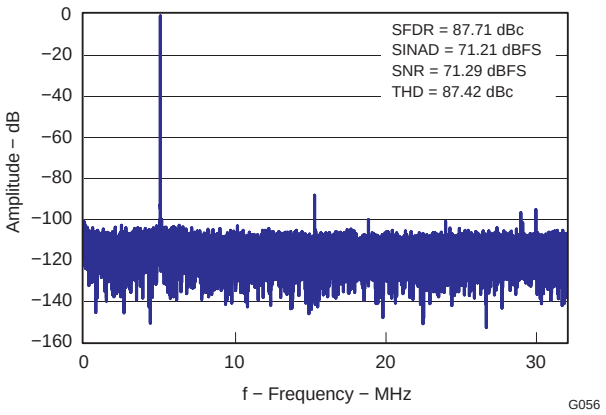

Figure 60.

FFT for 190 MHz INPUT SIGNAL

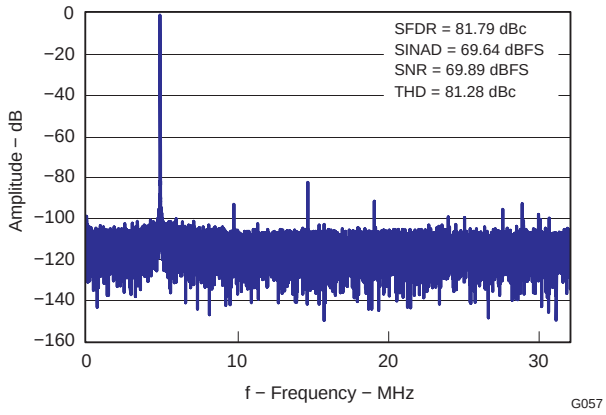

Figure 61.

INTERMODULATION DISTORTION (IMD) vs FREQUENCY

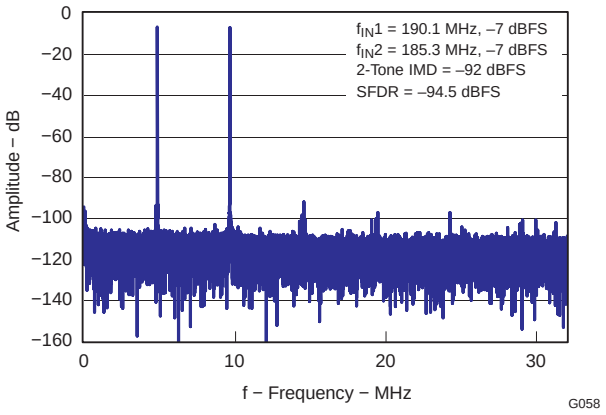

Figure 62.

SFDR vs INPUT FREQUENCY

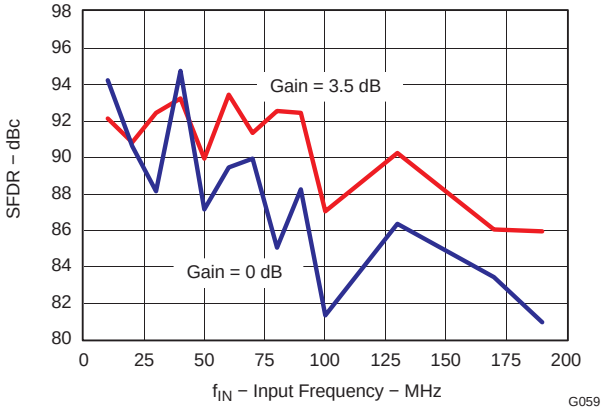

Figure 63.

SNR vs INPUT FREQUENCY

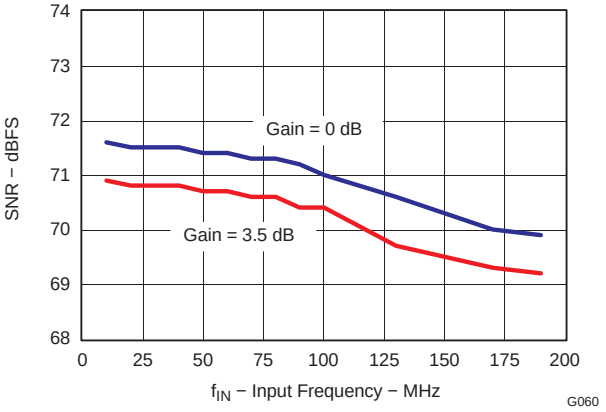

Figure 64.

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TYPICAL CHARACTERISTICS - ADS62P22 (F_S= 65 MSPS) (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

SFDR vs INPUT FREQUENCY (LVDS interface)

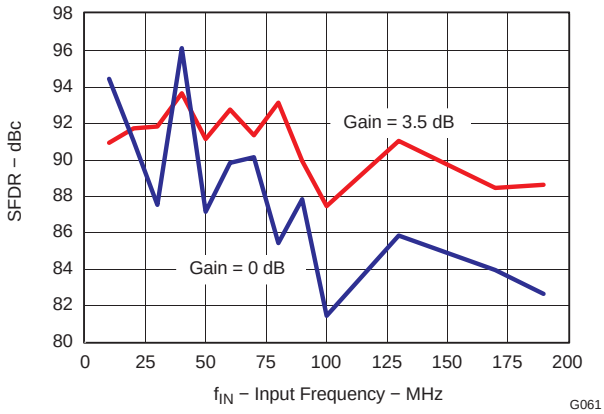

Figure 65.

SFDR vs INPUT FREQUENCY ACROSS GAIN

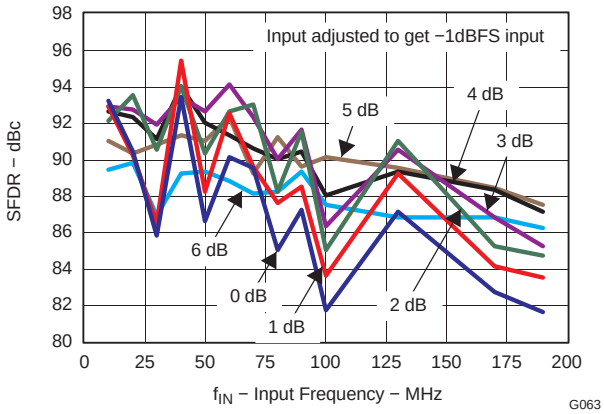

Figure 66.

SINAD vs INPUT FREQUENCY ACROSS GAIN

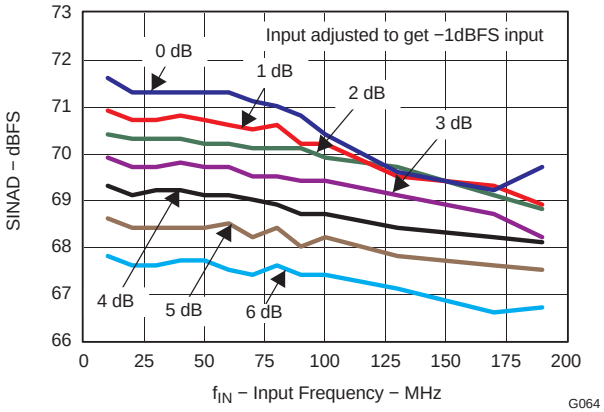

Figure 67.

PERFORMANCE vs AVDD

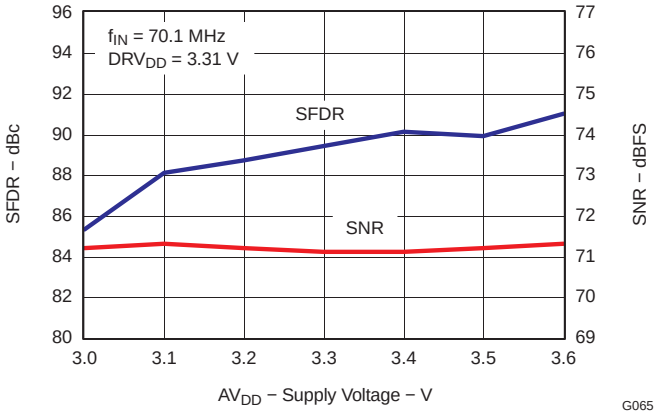

Figure 68.

PERFORMANCE vs DRVDD

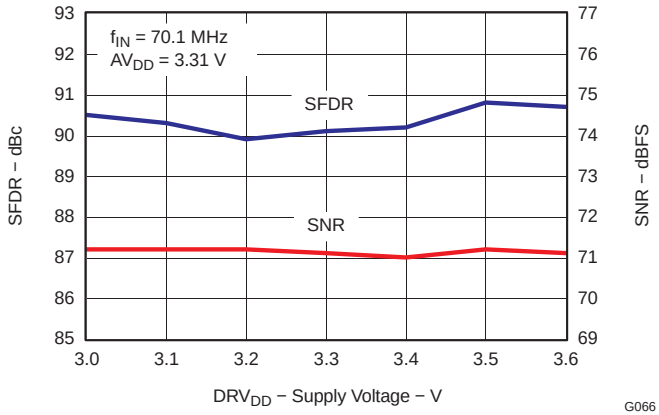

Figure 69.

PERFORMANCE vs TEMPERATURE

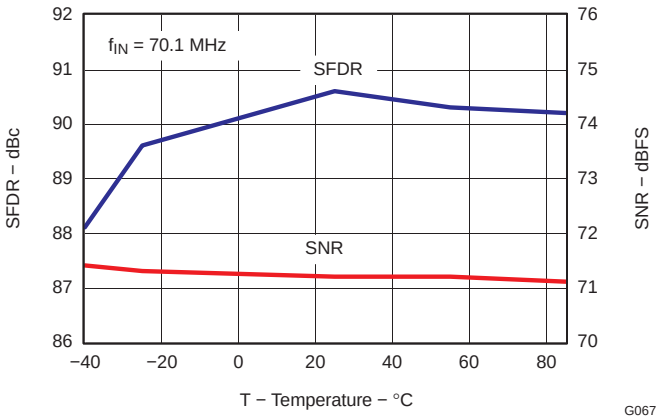

Figure 70.

TYPICAL CHARACTERISTICS - ADS62P22 (F_S= 65 MSPS) (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

PERFORMANCE vs INPUT AMPLITUDE

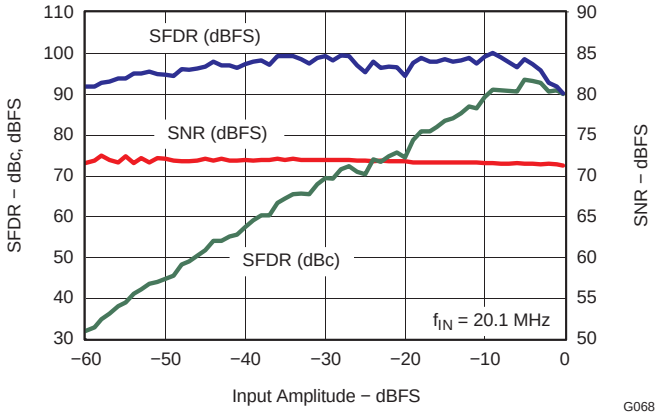

Figure 71.

PERFORMANCE vs CLOCK AMPLITUDE

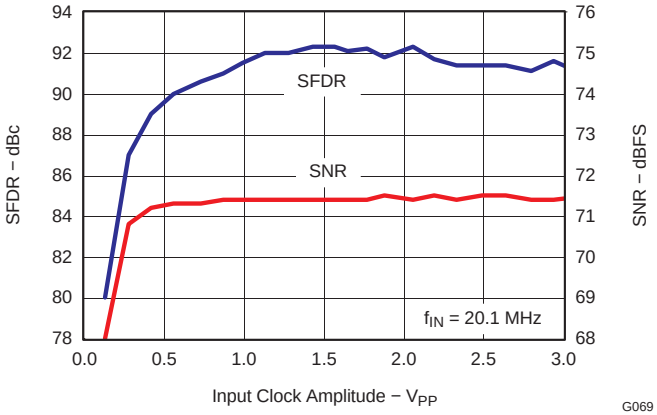

Figure 72.

PERFORMANCE vs INPUT CLOCK DUTY CYCLE

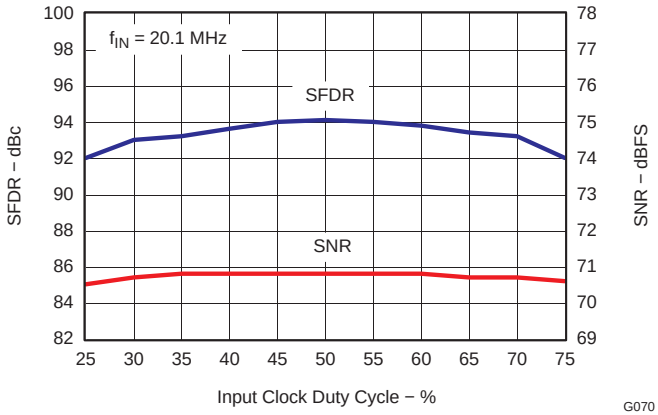

Figure 73.

OUTPUT NOISE HISTOGRAM WITH INPUTS TIED TO COMMON-MODE

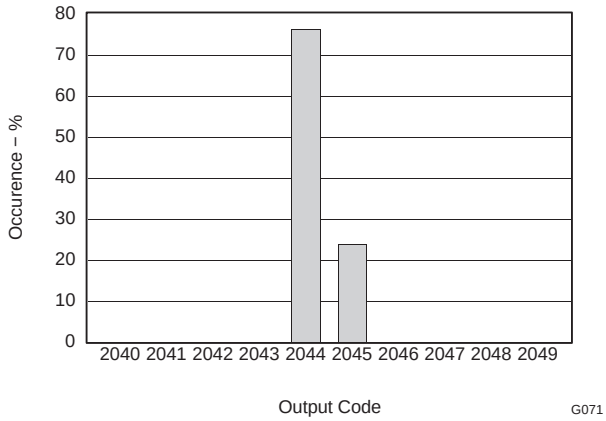

Figure 74.

PERFORMANCE IN EXTERNAL REFERENCE MODE

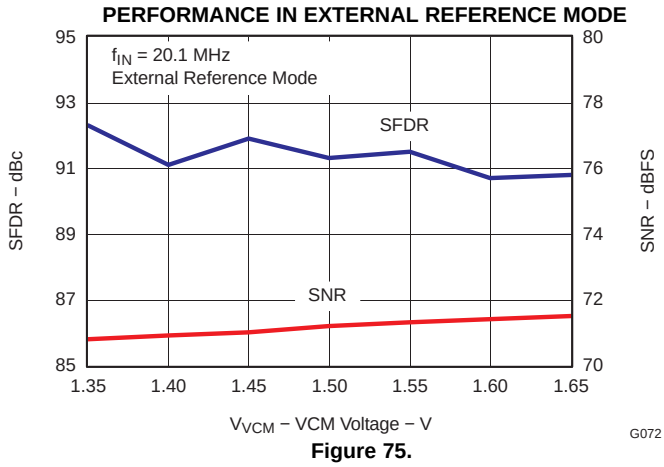

Figure 75.

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TYPICAL CHARACTERISTICS - LOW SAMPLING FREQUENCIES

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

F_S = 25 MSPS

SFDR vs INPUT FREQUENCY

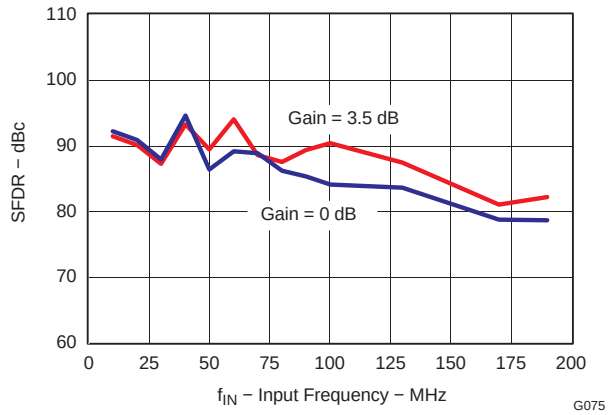

Figure 76.

SNR vs INPUT FREQUENCY

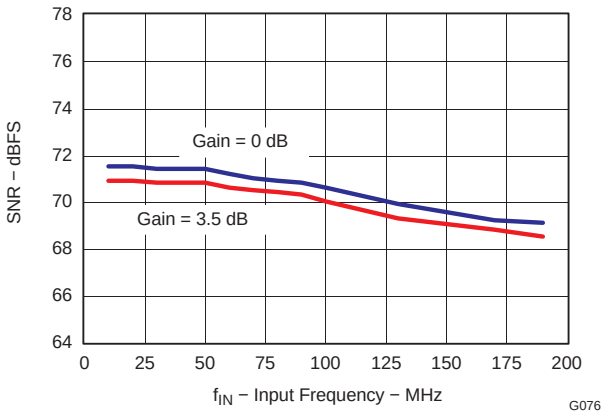

Figure 77.

COMMON PLOTS

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

COMMON-MODE REJECTION RATIO vs FREQUENCY

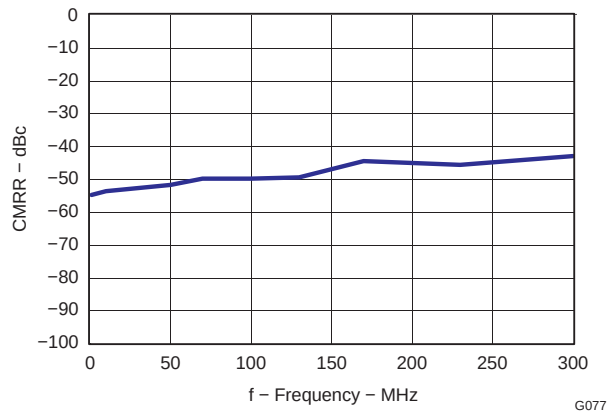

Figure 78.

POWER DISSIPATION vs SAMPLING FREQUENCY (DDR LVDS and CMOS)

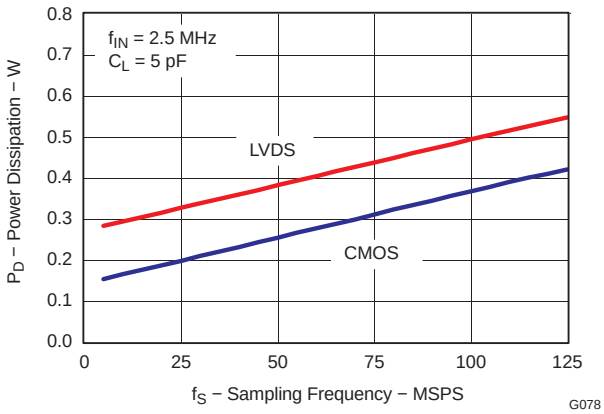

Figure 79.

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COMMON PLOTS (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

DRVDD current (CMOS interface)
vs
SAMPLING FREQUENCY across load capacitance

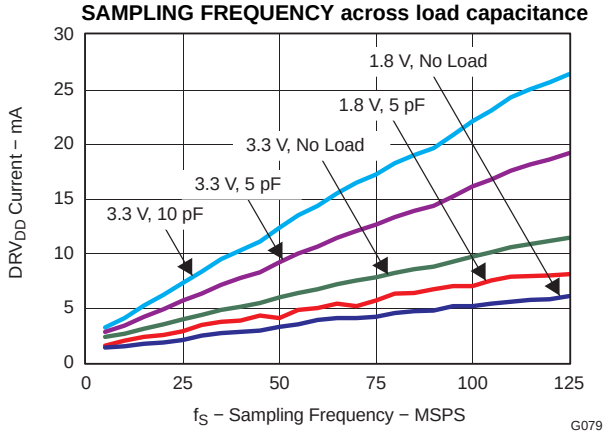

Figure 80.

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APPLICATION INFORMATION

THEORY OF OPERATION

ADS62P2X is a low power 12-bit dual channel pipeline ADC family fabricated in a CMOS process using switched capacitor techniques.

The conversion process is initiated by a rising edge of the external input clock. Once the signal is captured by the input sample and hold, the input sample is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline resulting in a data latency of 14 clock cycles. The output is available as 12-bit data, in DDR LVDS or CMOS and coded in either straight offset binary or binary 2s complement format.

ANALOG INPUT

The analog input consists of a switched-capacitor based differential sample and hold architecture.

This differential topology results in very good AC performance even for high input frequencies at high sampling rates. The INP and INM pins have to be externally biased around a common-mode voltage of 1.5 V, available on VCM pin 13. For a full-scale differential input, each input pin INP, INM has to swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2 V_{PP} differential input swing. The maximum swing is determined by the internal reference voltages REFP (2.5 V nominal) and REFM (0.5 V, nominal).

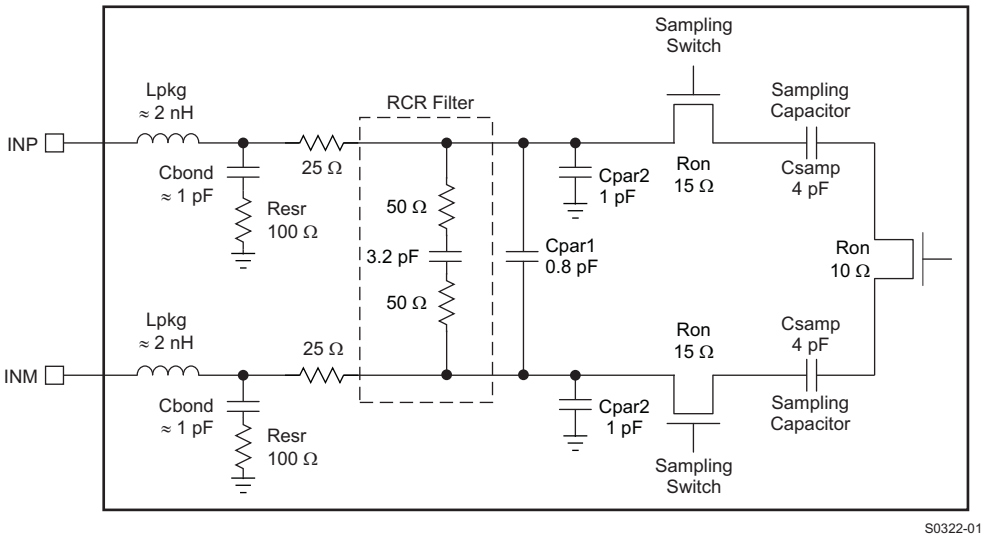

Figure 81. Analog Input Equivalent Circuit

The input sampling circuit has a high 3-dB bandwidth that extends up to 450 MHz (measured from the input pins to the sampled voltage).

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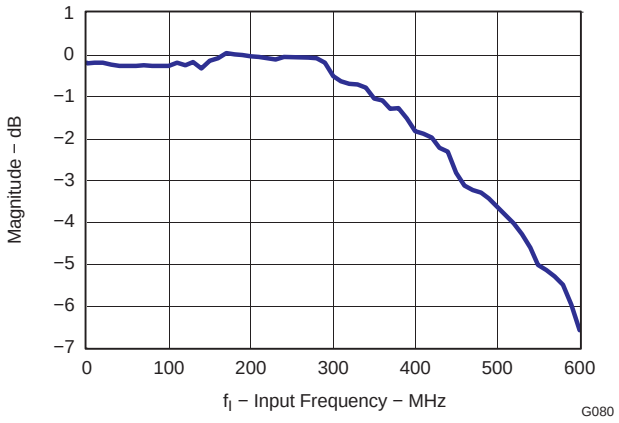

Figure 82. ADC Analog Bandwidth

Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even order harmonic rejection. A < 5 Ω resistor in series with each input pin is recommended to damp out ringing caused by the package parasitics.

It is also necessary to present low impedance (50 Ω) for the common mode switching currents. This can be achieved by using two resistors from each input terminated to the common mode voltage (VCM).

In addition, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. While doing this, the ADC input impedance must be considered. Figure 83 and Figure 84 show the impedance (Zin = Rin || Cin) looking into the ADC input pins.

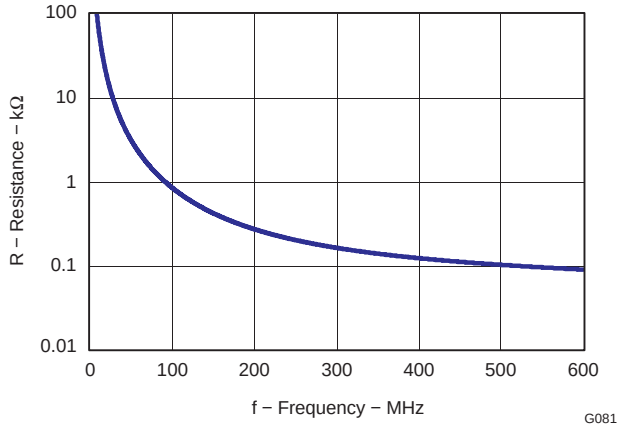

Figure 83. ADC Analog Input Resistance (Rin) Across Frequency

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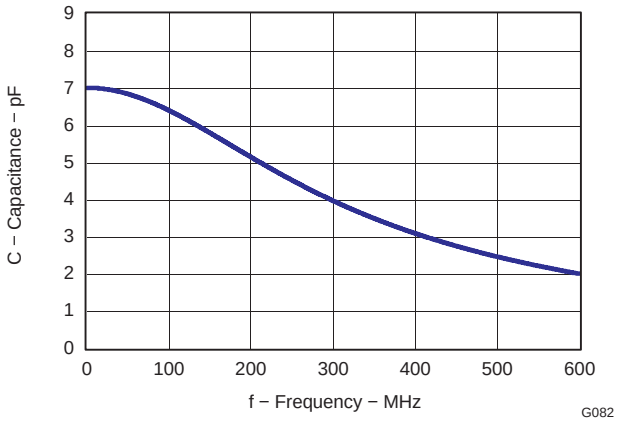

Figure 84. ADC Analog Input Capacitance (Cin) Across Frequency

Using RF-Transformer Based Drive Circuits

Figure 85 shows a configuration using a single 1:1 turns ratio transformer (for example, Coilcraft WBC1-1) that can be used for low input frequencies (about 100 MHz). The single-ended signal is fed to the primary winding of the RF transformer. The transformer is terminated on the secondary side. Putting the termination on the secondary side helps to shield the kickbacks caused by the sampling circuit from the RF transformer's leakage inductances. The termination is accomplished by two resistors connected in series, with the center point connected to the 1.5 V common mode (VCM pin). The value of the termination resistors (connected to common mode) has to be low (< 100 Ω) to provide a low-impedance path for the ADC common-mode switching currents.

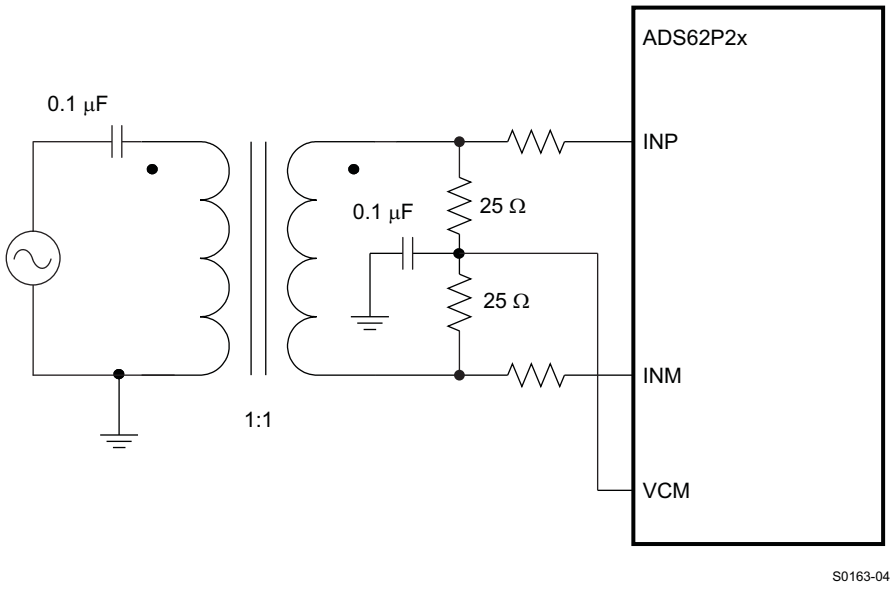

Figure 85. Drive Circuit at Low Input Frequencies

At high input frequencies, the mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch, and good performance is obtained for high frequency input signals. Figure 86 shows an example using two transformers (Coilcraft WBC1-1). An additional termination resistor pair (enclosed within the shaded box) may be required between the two transformers to improve the balance between the P and M sides. The center point of this termination must be connected to ground.

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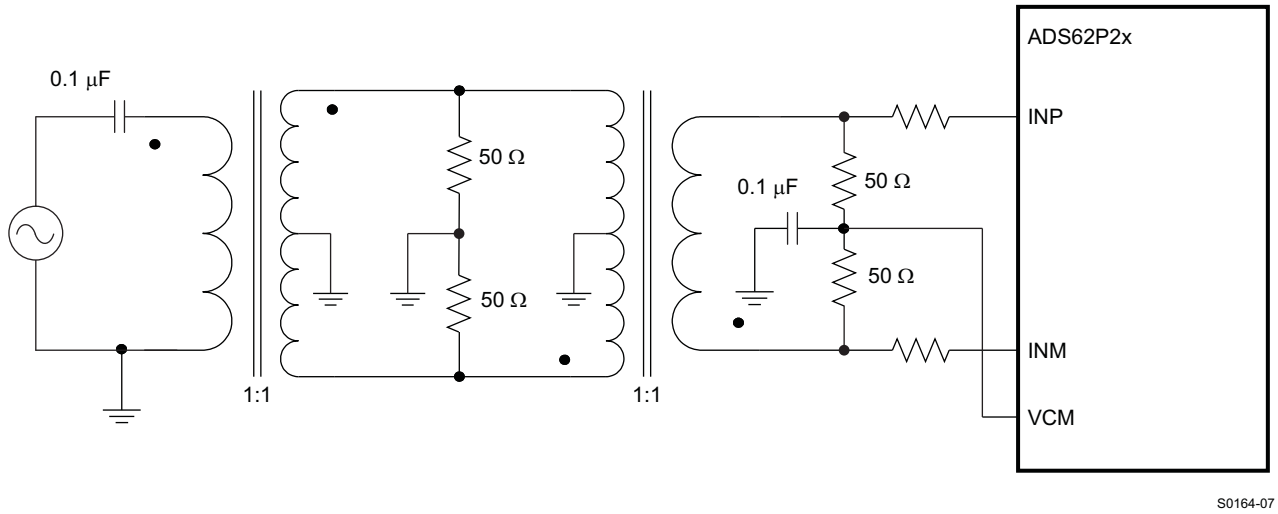

Figure 86. Drive Circuit at High Input Frequencies

Using Differential Amplifier Drive Circuits

Figure 87 shows a drive circuit using a differential amplifier (TI's THS4509) to convert a single-ended input to differential output that can be interface to the ADC analog input pins. In addition to the single-ended to differential conversion, the amplifier also provides gain (10 dB). R_{FIL} helps to isolate the amplifier outputs from the switching input of the ADC. Together with C_{FIL} it also forms a low-pass filter that band-limits the noise (and signal) at the ADC input. As the amplifier output is ac-coupled, the common-mode voltage of the ADC input pins is set using two 200 Ω resistors connected to VCM.

The amplifier output can also be dc-coupled. Using the output common-mode control of the THS4509, the ADC input pins can be biased to 1.5 V. In this case, use +4 V and –1 V supplies for the THS4509 so that its output common-mode voltage (1.5 V) is at mid-supply.

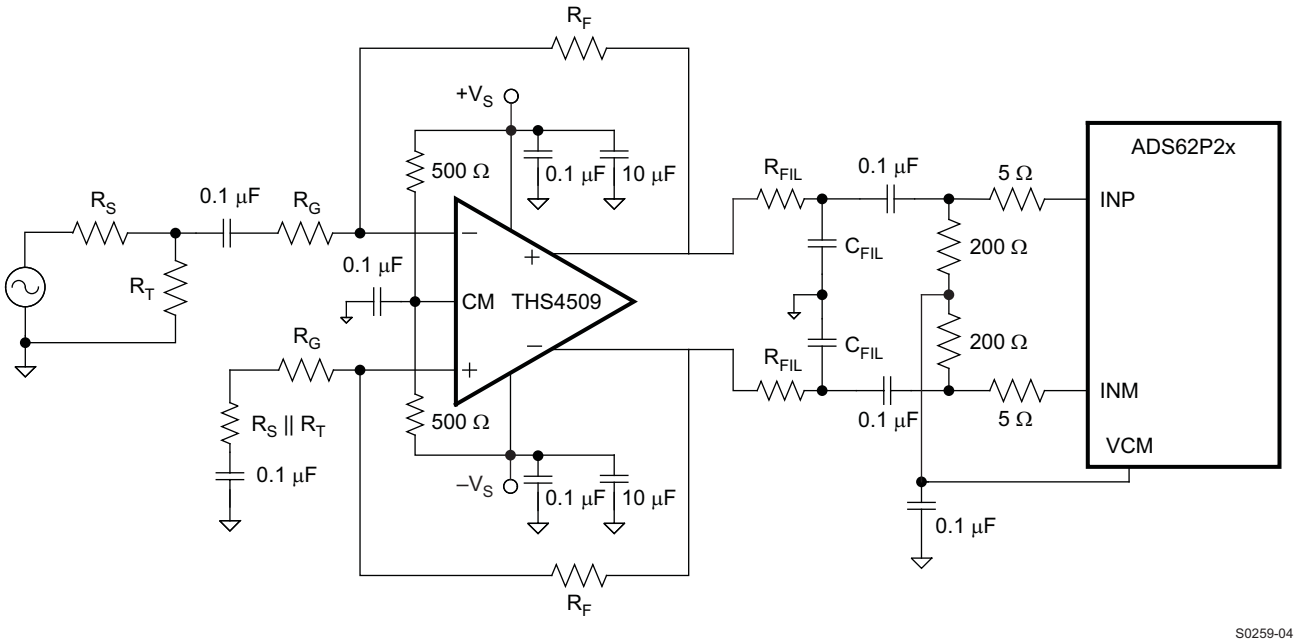

Figure 87. Drive Circuit Using the THS4509

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Input Common-Mode

To ensure a low-noise common-mode reference, the VCM pin is filtered with a 0.1 µF low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. The input stage of the ADC sinks a common-mode current in the order of 165 µA (at 125 MSPS). Equation 1 describes the dependency of the common-mode current and the sampling frequency.

$$\frac{165\ \mu A \times Fs}{125\ MSPS} \quad (1)$$

This equation helps to design the output capability and impedance of the CM driving circuit accordingly.

REFERENCE

ADS62P2X has built-in internal references REFP and REFM, requiring no external components. Design schemes are used to linearize the converter load seen by the references; this and the on-chip integration of the requisite reference capacitors eliminates the need for external decoupling. The full-scale input range of the converter can be controlled in the external reference mode as explained below. The internal or external reference modes can be selected by programming the serial interface register bit (REF).

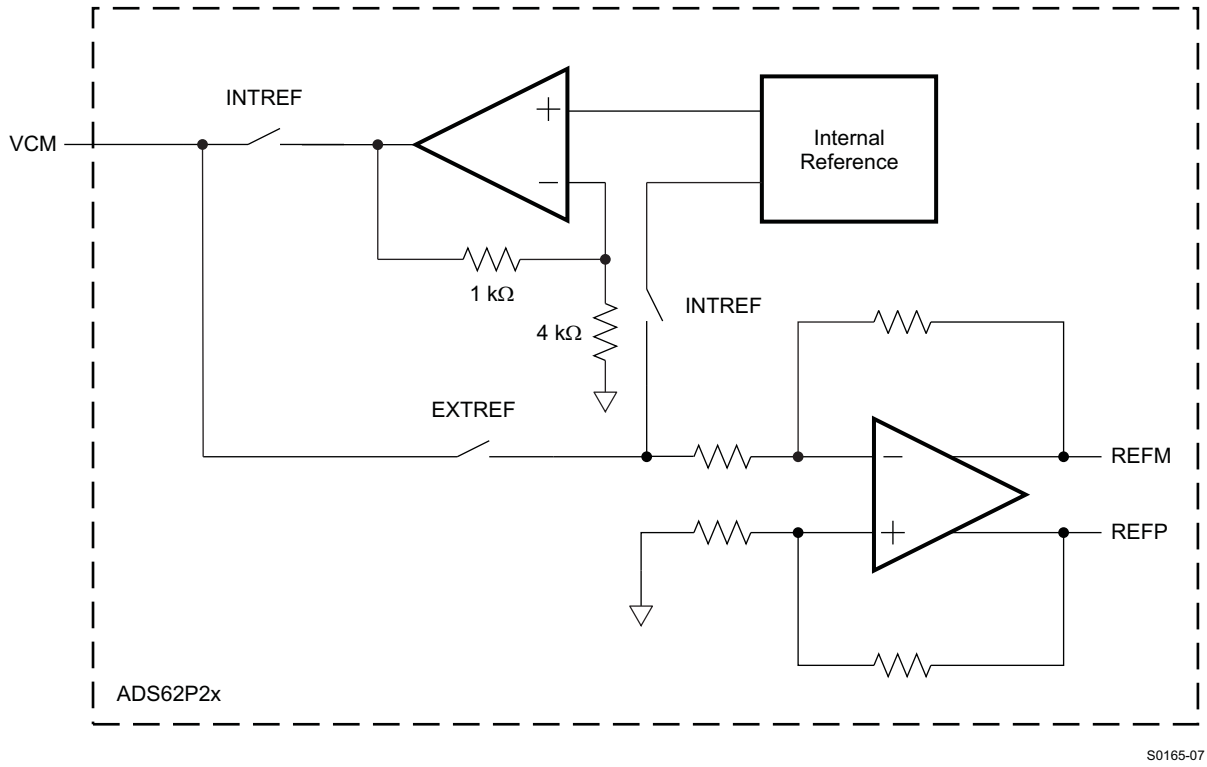

Figure 88. Reference Section

Internal Reference

When the device is in internal reference mode, the REFP and REFM voltages are generated internally. Common-mode voltage (1.5 V nominal) is output on VCM pin, which can be used to externally bias the analog input pins.

External Reference

When the device is in external reference mode, the VCM acts as a reference input pin. The voltage forced on the VCM pin is buffered and gained by 1.33 internally, generating the REFP and REFM voltages. The differential input voltage corresponding to full-scale is given in Equation 2.

Full-scale differential input pp = (Voltage forced on VCM) × 1.33 (2) (2)

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In this mode, the 1.5 V common-mode voltage to bias the input pins has to be generated externally.

COARSE GAIN AND PROGRAMMABLE FINE GAIN

ADS62P2X includes gain settings that can be used to get improved SFDR performance (over 0 dB gain mode). For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 20.

The coarse gain is a fixed setting of 3.5 dB and is designed to improve SFDR with little degradation in SNR. The fine gain is programmable in 0.5 dB steps from 0 to 6 dB; however the SFDR improvement is achieved at the expense of SNR. So, the programmable fine gain makes it possible to trade-off between SFDR and SNR. The coarse gain makes it possible to get best SFDR but without losing SNR significantly.

The gains can be programmed using the serial interface (bits COARSE GAIN and FINE GAIN). Note that the default gain after reset is 0 dB.

Table 20. Full-Scale Range Across Gains

GAIN, dB	TYPE	FULL-SCALE, V_{PP}
0	Default after reset	2V
3.5	Coarse (fixed)	1.34
0.5	Fine (programmable)	1.89
1.0		1.78
1.5		1.68
2.0		1.59
2.5		1.50
3.0		1.42
3.5		1.34
4.0		1.26
4.5		1.19
5.0		1.12
5.5		1.06
6.0		1.00

CLOCK INPUT

The clock inputs can be driven differentially (sine, LVPECL or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5 kΩ resistors as shown in Figure 89. This allows using transformer-coupled drive circuits for sine wave clock or ac-coupling for LVPECL, LVDS clock sources (Figure 91 and Figure 92).

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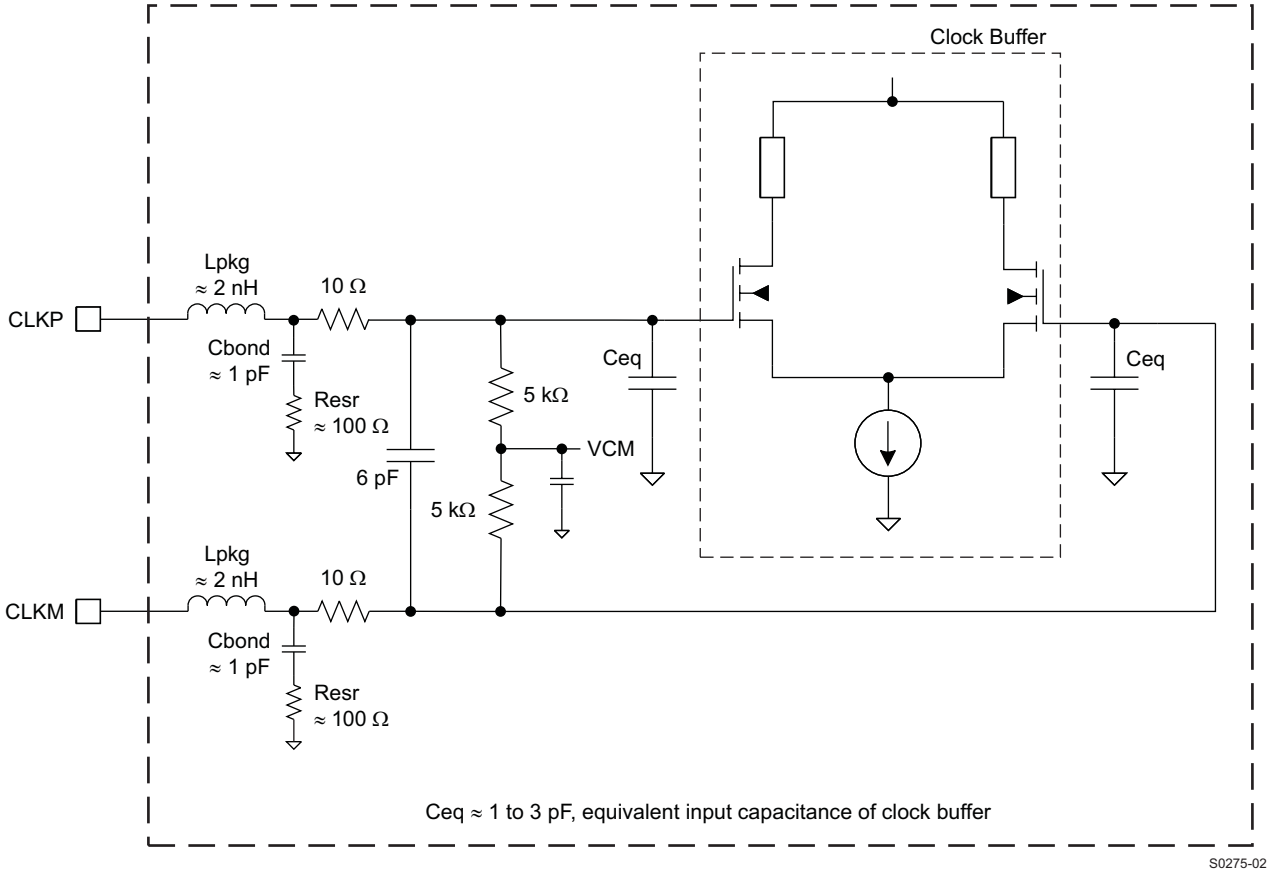

Figure 89. Internal Clock Buffer

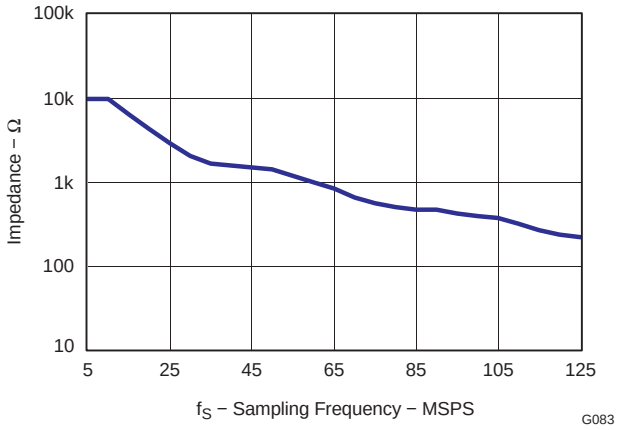

Figure 90. Clock Input Impedance

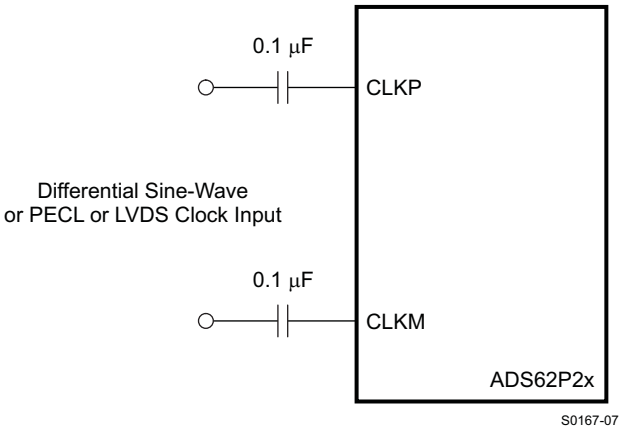

Figure 91. Differential Clock Driving Circuit

Single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 92.

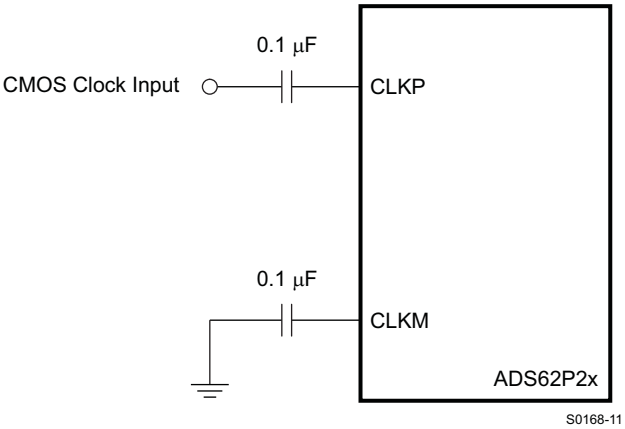

Figure 92. Single-Ended Clock Driving Circuit

For best performance, the clock inputs have to be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effect of jitter. There is no change in performance with a non-50% duty cycle clock input.

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POWER DOWN

ADS62P2X has three powerdown modes – powerdown global, individual channel standby and individual channel output buffer disable. These can be set using either the serial register bits or using the control pins CTRL1 to CTRL3.

Table 21. Power Down Modes

POWERDOWN MODES	CONFIGURE USING				WAKE-UP TIME
	SERIAL INTERFACE <POWER DOWN MODES>	PARALLEL CONTROL PINS			
		CTRL1	CTRL2	CTRL3	
Normal operation	000	low	low	low	—
Channel A output buffer disabled	001	low	low	high	Fast (100 ns)
Channel B output buffer disabled	010	low	high	low	Fast (100 ns)
Channel A and B output buffer disabled	011	low	high	high	Fast (100 ns)
Channel A and B powered down	100	high	low	low	Slow (15 µS)
Channel A standby	101	high	low	high	Fast (100 ns)
Channel B standby	110	high	high	low	Fast (100 ns)
Multiplexed (MUX) mode – Output data of channel A and B is multiplexed and available on DB11 to DB0 pins.	111	high	high	high	—

PowerDown Global

In this mode, the entire chip including both the A/D converters, internal reference and the output buffers are powered down resulting in reduced total power dissipation of about 50 mW. The output buffers are in high impedance state. The wake-up time from the global power down to data becoming valid in normal mode is typically 15 µs.

Channel Standby (Individual or Both Channels)

This mode allows the individual ADCs to be powered down. The internal references are active and this results in fast wake-up time, about 100 ns. The total power dissipation in standby is about 482 mW.

Output Buffer Disable (Individual or Both Channels)

Each channel's output buffer can be disabled and put in high impedance state -- wakeup time from this mode is fast, about 100 ns.

Input Clock Stop

In addition to the above, the converter enters a low-power mode when the input clock frequency falls below 1 MSPS. The power dissipation is about 140 mW.

POWER SUPPLY SEQUENCE

During power-up, the AVDD and DRVDD supplies can come up in any sequence. The two supplies are separated in the device. Externally, they can be driven from separate supplies or derived from a single supply.

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DIGITAL OUTPUT INFORMATION

ADS62P2X provides 12 bit data per channel and a common output clock synchronized with the data. The output interface can be either parallel CMOS or DDR LVDS voltage levels and can be selected using serial register bit **<OUTPUT INTERFACE>** or parallel pin SEN.

Parallel CMOS Interface

In the CMOS mode, the output buffer supply (DRVDD) can be operated over a wide range from 1.8 V to 3.3 V (typical). Each data bit is output on separate pin as CMOS voltage level, every clock cycle (see Figure 93).

For DRVDD > 2.2 V, it is recommended to use the CMOS output clock (CLKOUT) to latch data in the receiving chip. The rising edge of CLKOUT can be used to latch data in the receiver, even at the highest sampling speed. It is recommended to minimize the load capacitance seen by data and clock output pins by using short traces to the receiver. Also, match the output data and clock traces to minimize the skew between them.

For DRVDD < 2.2 V, it is recommended to use external clock (for example, input clock delayed to get desired setup/hold times).

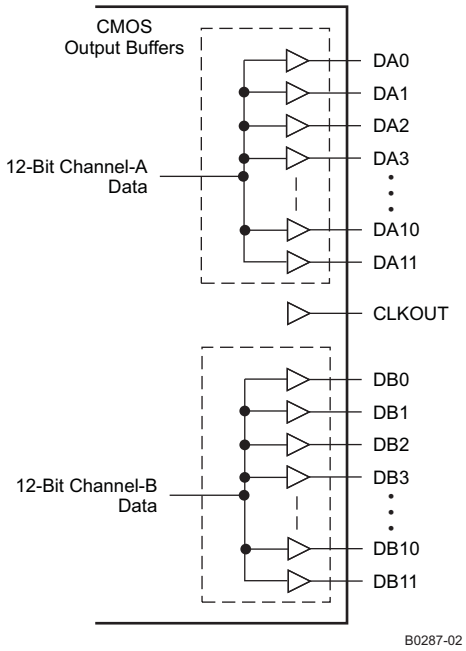

Figure 93. CMOS Output Interface

Output Buffer Strength Programmability

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs during the instant of sampling and degrade the SNR. The coupling and SNR degradation increases as the output buffer drive is made stronger. To minimize this, ADS62P2X CMOS output buffers are designed with controlled drive strength to get best SNR. The default drive strength also ensures wide data stable window for load capacitances up to 5 pF and DRVDD supply voltage > 2.2 V.

To ensure wide data stable window for load capacitance > 5 pF, there exists option to increase the output data and clock drive strengths using the serial interface (DATAOUT STRENGTH and CLKOUT STRENGTH). Note that for DRVDD supply voltage < 2.2 V, it is recommended to use maximum drive strength (for any value of load capacitance).

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CMOS Mode Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

Digital current due to CMOS output switching = $C_L \times DRVDD \times (N \times F_{AVG})$,

where C_L = load capacitance, $N \times F_{AVG}$ = average number of output bits switching.

Figure 80 shows the current with various load capacitances across sampling frequencies at 2 MHz analog input frequency.

DDR LVDS Interface

The LVDS interface works only with 3.3 V DRVDD supply. In this mode, the 12 data bits of each channel and a common output clock are available as LVDS (Low Voltage Differential Signal) levels. Two successive data bits are multiplexed and output on each LVDS differential pair every clock cycle (DDR – Double Data Rate, Figure 95).

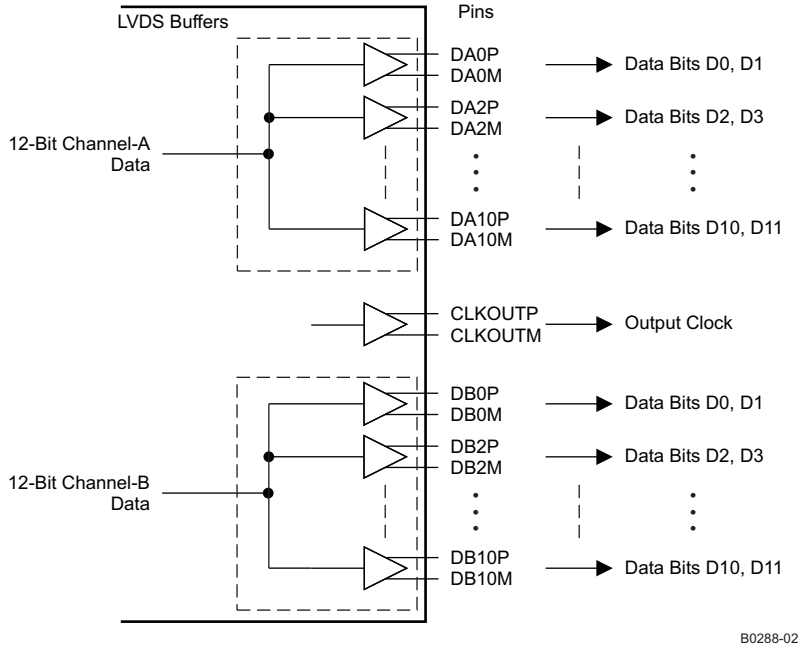

Figure 94. DDR LVDS Outputs

Even data bits D0, D2, D4, D6, D8, D10 are output at the rising edge of CLKOUTP and odd data bits D1, D3, D5, D7, D9, D11 are output at the falling edge of CLKOUTP. Both the rising and falling edges of CLKOUTP have to be used to capture all the data bits.

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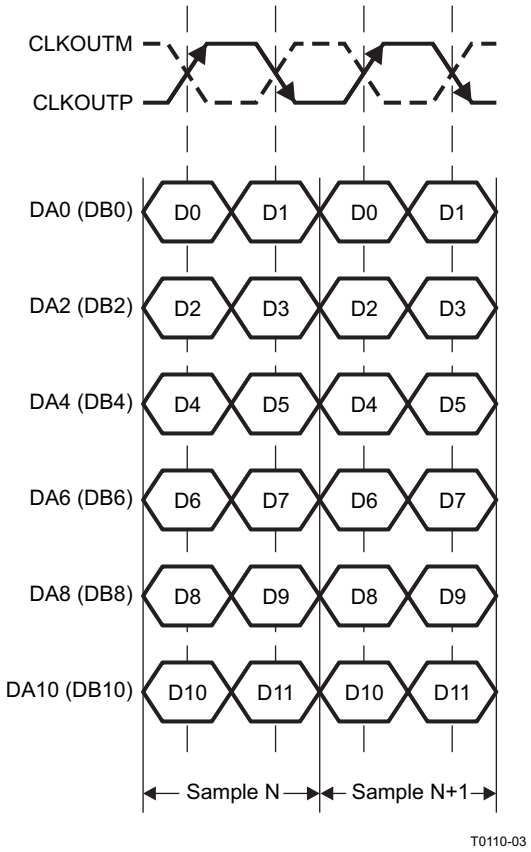

Figure 95. DDR LVDS Interface

LVDS Buffer Current Programmability

The default LVDS buffer output current is 3.5 mA. When terminated by 100 Ω, this results in a 350-mV single-ended voltage swing (700-mV_{PP} differential swing). The LVDS buffer currents can also be programmed to 2.5 mA, 4.5 mA, and 1.75 mA (LVDS CURRENT). In addition, there exists a current double mode, where this current is doubled for the data and output clock buffers (register bits CURRENT DOUBLE).

LVDS Buffer Internal Termination

An internal termination option is available (using the serial interface), by which the LVDS buffers are differentially terminated inside the device. The termination resistances available are – 300 Ω, 185 Ω, and 150 Ω (nominal with ±20% variation). Any combination of these three terminations can be programmed; the effective termination is the parallel combination of the selected resistances. This results in eight effective terminations from open (no termination) to 60 Ω.

The internal termination helps to absorb any reflections coming from the receiver end, improving the signal integrity. With 100 Ω internal and 100 Ω external termination, the voltage swing at the receiver end is halved (compared to no internal termination). The voltage swing can be restored by using the LVDS current double mode. Figure 96 and Figure 97 compare the LVDS eye diagrams without and with 100 Ω internal termination. With internal termination, the eye looks clean even with 10 pF load capacitance (from each output pin to ground). The terminations can be programmed using register bits (LVDS TERMINATION).

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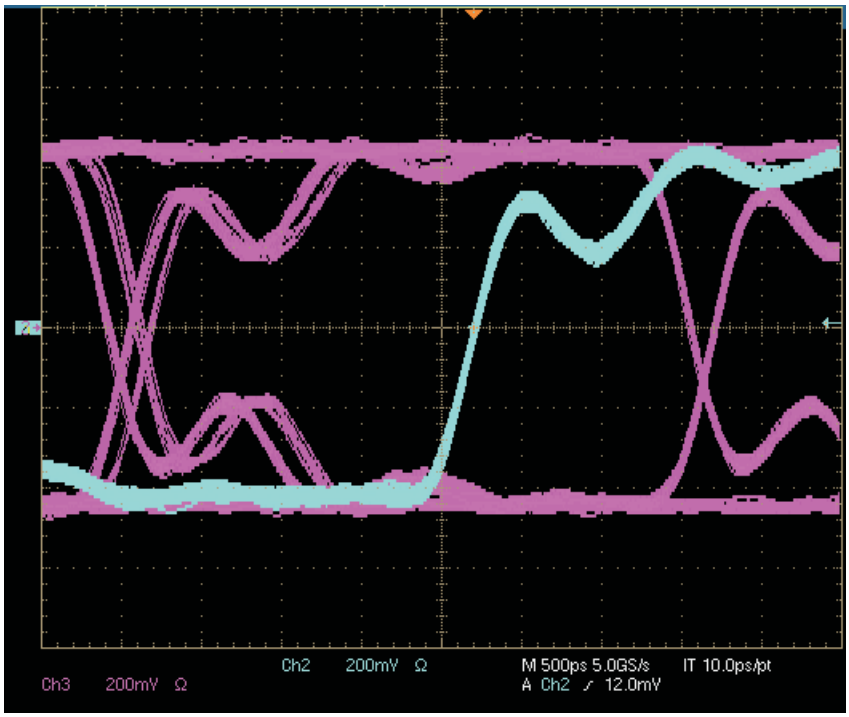

Figure 96. LVDS Eye Diagram – No Internal Termination, External Termination = 100 Ω

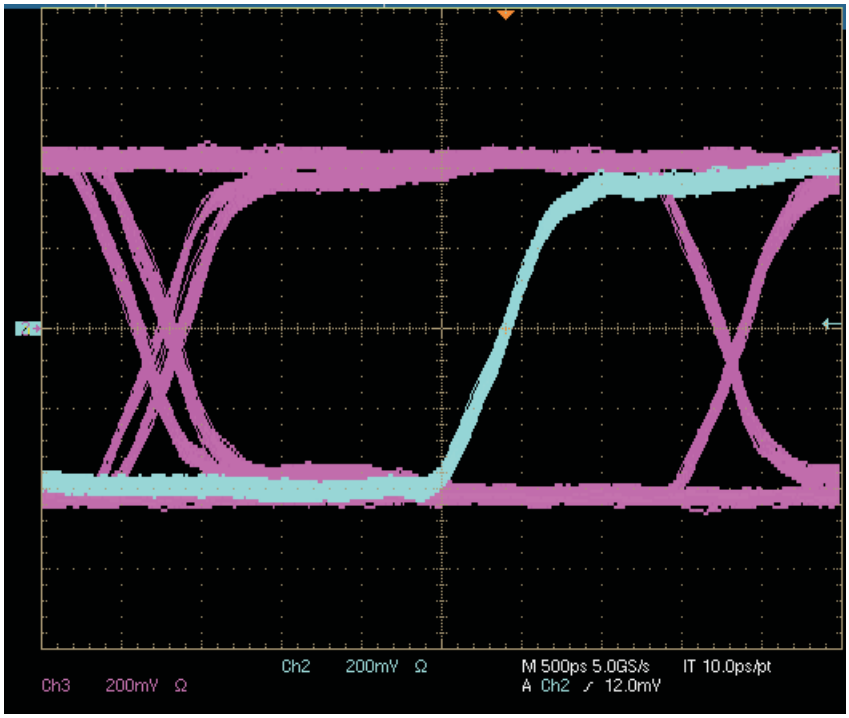

Figure 97. LVDS Eye Diagram – With 100 Ω Internal Termination, External termination = 100 Ω and LVDS current Double Mode Enabled

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Output Data Format

Two output data formats are supported – 2s complement and straight binary. They can be selected using the serial interface register bit <**DATA FORMAT**> or controlling the SEN pin in parallel configuration mode.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full scale level. For a positive overdrive, the output code is 0x7FF in offset binary output format, and 0x3FF in 2s complement output format. For a negative input overdrive, the output code is 0x000 in offset binary output format and 0x400 in 2s complement output format.

Multiplexed Output mode

This mode is available only with CMOS interface. In this mode, the digital outputs of both the channels are multiplexed and output on a single bus (DB0 - DB11 pins), as per the timing diagram shown in Figure 98. The channel A output pins (DA0 - DA11) are three-stated. Since the output data rate on the DB bus is effectively doubled, this mode is recommended only for low sampling frequencies (< 65 MSPS).

This mode can be enabled using register bits <**POWERDOWN MODES**> or using the parallel pins CTRL1, CTRL2, and CTRL3.

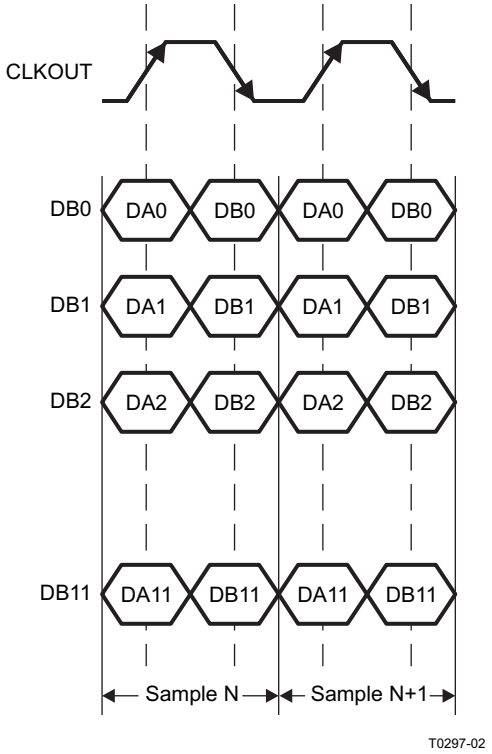

Figure 98. Multiplexed Mode – Output Timing

Low Latency Mode

The default latency of ADS62P2X is 14 clock cycles. For applications, which cannot tolerate large latency, ADS62P2X includes a special mode with 10 clock cycles latency. In the low latency condition, the Digital Processing block is bypassed and its features (offset correction, fine gain, decimation filters) are not available.

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DETAILS OF DIGITAL PROCESSING BLOCK

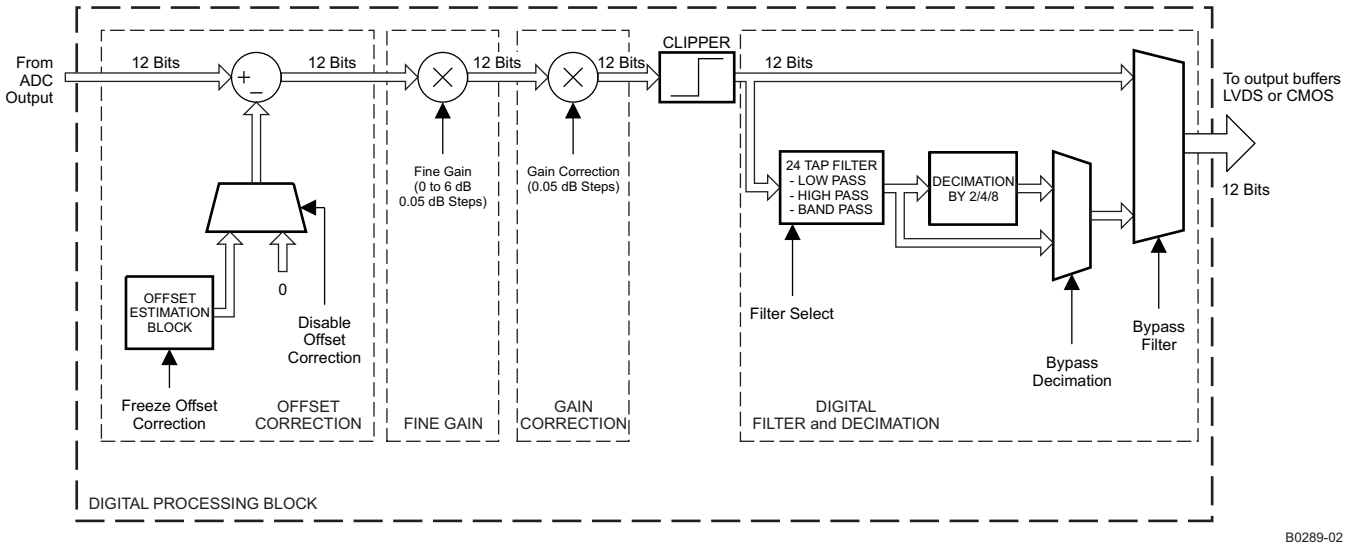

Figure 99. Digital Processing Block Diagram

Offset Correction

ADS62P2X has an internal offset correction algorithm that estimates and corrects dc offset up to ±10 mV. The correction can be enabled using the serial register bit (OFFSET LOOP EN). Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using register bits (OFFSET LOOP TC) as described in Table 22.

Table 22. Time Constant of Offset Correction Algorithm

<OFFSET LOOP TC> D6-D5-D4	TIME CONSTANT (TC_{CLK}), Number of clock cycles	TIME CONSTANT, sec (= TC_{CLK} × 1/Fs)(1)
000	2^{27}	1.1
001	2^{26}	0.55
010	2^{25}	0.27
011	2^{24}	0.13
100	2^{28}	2.15
101	2^{29}	4.3
110	2^{27}	1.1
111	2^{27}	1.1

(1) Sampling frequency, Fs = 125 MSPS

It is also possible to freeze the offset correction using the serial interface (<**OFFSET LOOP FREEZE**>). Once frozen, the offset estimation becomes inactive and the last estimated value is used for correction every clock cycle. Note that the offset correction is disabled by default after reset.

Figure 100 shows the time response of the offset correction algorithm, after it is enabled (for clarity, an example with no applied input signal is shown). A few time constants after the correction is enabled, the offset gets cancelled and the output code approaches the ideal value of 2048.

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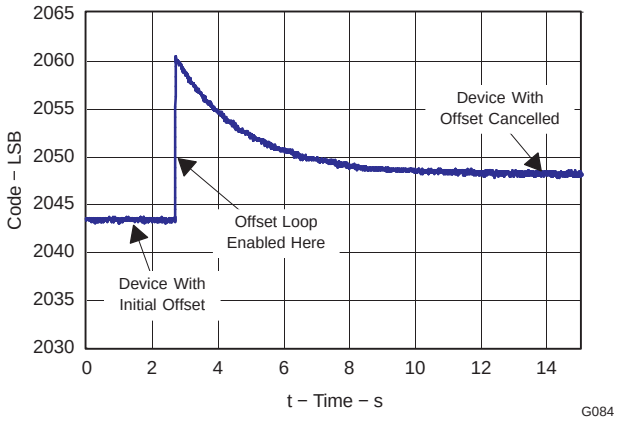

Figure 100. Time Response of Offset Correction

Gain Correction

ADS62P2X has ability to make fine corrections to the ADC channel gain. The corrections can be done in steps of 0.05 dB, up to a maximum of 0.5 dB, using the register bits (GAIN CORRECTION). Only positive corrections are supported and the same correction applies to both the channels.

Table 23. Gain Correction Values

<GAIN CORRECTION> D3-D2-D1-D0	AMOUNT OF CORRECTION, dB
0000	0
0001	+0.05
0010	+0.1
0011	+0.15
0100	+0.20
0101	+0.25
0110	+0.30
0111	+0.35
1000	+0.40
1001	+0.45
1010	+0.5
Other combinations	Unused

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Decimation Filters

ADS62P2X includes option to decimate the ADC output data with in-built low-pass, high-pass, or band-pass filters.

The decimation rate and type of filter can be selected using register bits (DECIMATION RATE) and (DECIMATION FILTER TYPE). Decimation rates of 2, 4, or 8 are available and either low-pass, high-pass, or band-pass filters can be selected (see Table 24). By default, the decimation filter is disabled – use register bit **<FILTER ENABLE>** to enable it.

Table 24. Decimation Filter Modes

COMBINATION OF DECIMATION RATES AND FILTER TYPES		<DECIMATION RATE>			<DECIMATION FILTER FREQ BAND>		<FILTER COEFF SELECT>	<FILTER ENABLE>
DECIMATION	TYPE OF FILTER							
Decimate by 2	In-built low-pass filter (pass band = 0 to Fs/4)	0	0	0	0	0	0	1
	In-built high-pass filter (pass band = Fs/4 to Fs/2)	0	0	0	0	1	0	1
Decimate by 4	In-built low-pass filter (pass band = 0 to Fs/8)	0	0	1	0	0	0	1
	In-built 2nd band-pass filter (pass band = Fs/8 to Fs/4)	0	0	1	0	1	0	1
	In-built 3rd band-pass filter (pass band = Fs/4 to 3Fs/8)	0	0	1	1	0	0	1
	In-built last band-pass filter (pass band = 3Fs/8 to Fs/2)	0	0	1	1	1	0	1
Decimate by 2	Custom filter (user programmable coefficients)	0	0	0	X	X	1	1
Decimate by 4	Custom filter (user programmable coefficients)	0	0	1	X	X	1	1
Decimate by 8	Custom filter (user programmable coefficients)	1	0	0	X	X	1	1
NO decimation	Custom filter (user programmable coefficients)	0	1	1	X	X	1	0

Decimation Filter Equation

The decimation filter is implemented as 24-tap FIR with symmetrical coefficients (each coefficient is 12-bit signed). The filter equation is:

$$y(n) = \left(\frac{1}{2^{11}}\right) \times [h0 \times x(n) + h1 \times x(n-1) + h2 \times x(n-2) + \ ... \ + h11 \times x(n-11) + h11 \times x(n-12) + \ ... \ + h1 \times x(n-22) + h0 \times x(n-23)] \quad (3)$$

By setting the register bit <ODD TAP ENABLE> = 1, a 23-tap FIR is implemented:

$$y(n) = \left(\frac{1}{2^{11}}\right) x[h0 \times x(n) + h1 \times x(n-1) + h2 \times x(n-2) + ... \ + h10 \times x(n-10) + h11 \times x(n-11) + h10 \times x(n-12) + ... \ + h1 \times x(n-21) + h0 \times x(n-22)] \quad (4)$$

In the above equations,

h0, h1 …h11 are 12-bit signed representation of the coefficients,
x(n) is the input data sequence to the filter
y(n) is the filter output sequence

Pre-defined Coefficients

The in-built filter types (low-pass, high-pass, and band-pass) use pre-defined coefficients. The frequency response of the in-built filters is shown in Figure 101 and Figure 102.

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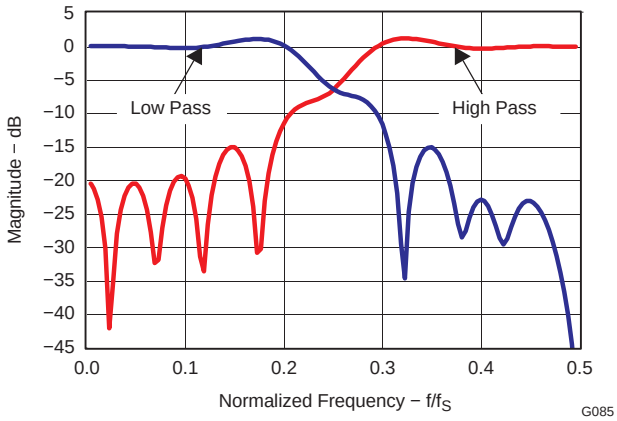

Figure 101. Decimate by 2 Filter Response

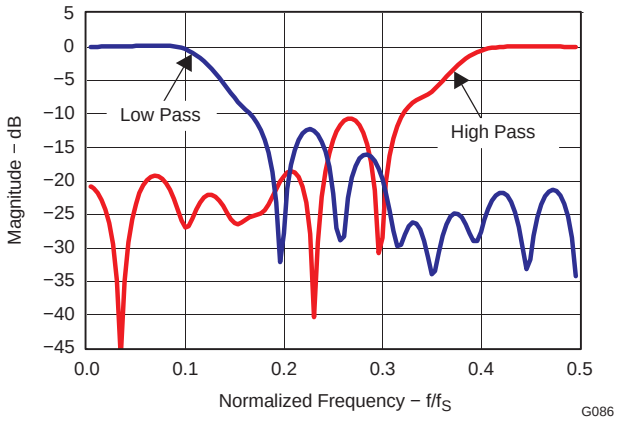

Figure 102. Decimate by 4 Filter Response

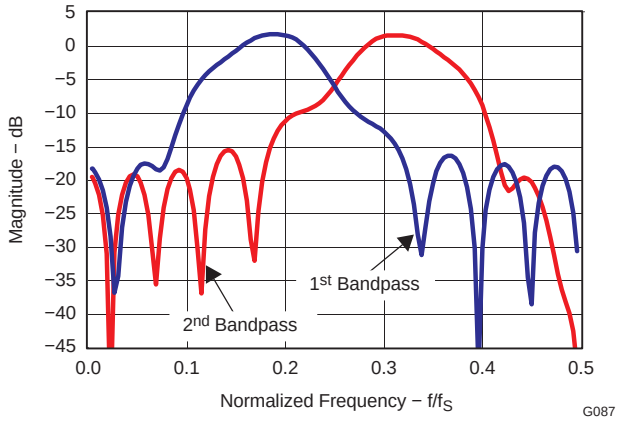

Figure 103. Decimate by 4 Band-Pass Response

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Table 25. Predefined Coefficients for Decimation by 2 Filters

COEFFICIENTS	DECIMATE BY 2	
	LOW-PASS FILTER	HIGH-PASS FILTER
h0	23	-22
h1	-37	-65
h2	-6	-52
h3	68	30
h4	-36	66
h5	-61	-35
h6	35	-107
h7	118	38
h8	-100	202
h9	-197	-41
h10	273	-644
h11	943	1061

Table 26. Predefined Coefficients for Decimation by 4 Filters

COEFFICIENTS	DECIMATE BY 4			
	LOW-PASS FILTER	1st BAND-PASS FILTER	2ND BAND-PASS FILTER	HIGH-PASS FILTER
h0	-17	-7	-34	32
h1	-50	19	-34	-15
h2	71	-47	-101	-95
h3	46	127	43	22
h4	24	73	58	-8
h5	-42	0	-28	-81
h6	-100	86	-5	106
h7	-97	117	-179	-62
h8	8	-190	294	-97
h9	202	-464	86	310
h10	414	-113	-563	-501
h11	554	526	352	575

Custom Filter Coefficients with Decimation

The filter coefficients can also be programmed by the user (custom). For custom coefficients, set the register bit (FILTER COEFF SELECT) and load the coefficients (h0 to h11) in registers 1E to 2F using the serial interface (Table 27) as:

Register content = 12 bit signed representation of [real coefficient value × 2^{11}]

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Custom Filter Coefficients without Decimation

The filter with custom coefficients can also be used with the decimation mode disabled. In this mode, the filter implementation is 12-tap FIR:

$$y(n) = \left(\frac{1}{2^{11}}\right) x[h6 \times x(n) + h7 \times x(n-1) + h8 \times x(n-2) + \ldots + h11 \times x(n-5) + h11 \times x(n-6) + \ldots + h7 \times x(n-10) + h6 \times x(n-11)] \quad (5)$$

Table 27. Register Map of Custom Coefficients

A7–A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
1E	Coefficient h0 <7:0>							
1F	Coefficient h1 <3:0>				Coefficient h0 <11:8>			
20	Coefficient h1 <11:4>							
21	Coefficient h2 <7:0>							
22	Coefficient h3 <3:0>				Coefficient h2 <11:8>			
23	Coefficient h3 <11:4>							
24	Coefficient h4 <7:0>							
25	Coefficient h5 <3:0>				Coefficient h4 <11:8>			
26	Coefficient h5 <11:4>							
27	Coefficient h6 <7:0>							
28	Coefficient h7 <3:0>				Coefficient h6 <11:8>			
29	Coefficient h7 <11:4>							
2A	Coefficient h8 <7:0>							
2B	Coefficient h9 <3:0>				Coefficient h8 <11:8>			
2C	Coefficient h9 <11:4>							
2D	Coefficient h10 <7:0>							
2E	Coefficient h11 <3:0>				Coefficient h10 <11:8>			
2F	Coefficient h11 <11:4>							

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BOARD DESIGN CONSIDERATIONS

Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the EVM User Guide (SLAU237) for details on layout and grounding.

Supply Decoupling

As ADS62P2X already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power supply noise, so the optimum number of capacitors would depend on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

It is recommended to use separate supplies for the analog and digital supply pins to isolate digital switching noise from sensitive analog circuitry. In case only a single 3.3-V supply is available, it should be routed first to AVDD. It can then be tapped and isolated with a ferrite bead (or inductor) with decoupling capacitor, before being routed to DRVDD.

Exposed Thermal Pad

It is necessary to solder the exposed pad at the bottom of the package to a ground plane for best thermal performance. For detailed information, see application notes ***QFN Layout Guidelines*** (SLOA122) and ***QFN/SON PCB Attachment*** (SLUA271).

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DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay

The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate

The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate

The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs

Integral Nonlinearity (INL)

The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error

Gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error due to reference inaccuracy and error due to the channel. Both these errors are specified independently as E_{GREF} and E_{GCHAN}.

To a first order approximation, the total gain error will be $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from (1-0.5/100) x FS_{ideal} to (1+0.5/100) x FS_{ideal}.

Offset Error

The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

Temperature Drift

The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX}–T_{MIN}$.

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Signal-to-Noise Ratio

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$SNR = 10Log^{10}\frac{P_S}{P_N} \quad (6)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10}\frac{P_S}{P_N + P_D} \quad (7)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Number of Bits (ENOB)

The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (8)$$

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$THD = 10Log^{10}\frac{P_S}{P_N} \quad (9)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR)

The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion

IMD3 is the ratio of the power of the fundamental (at frequencies f1 and f2) to the power of the worst spectral component at either frequency 2f1–f2 or 2f2–f1. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

DC Power Supply Rejection Ratio (DC PSRR)

The DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

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AC Power Supply Rejection Ratio (AC PSRR)

AC PSRR is the measure of rejection of variations in the supply voltage of the ADC. If ΔV_{SUP} is the change in the supply voltage and ΔV_{OUT} is the resultant change in the ADC output code (referred to the input), then

$$PSRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \quad (10)$$

Common Mode Rejection Ratio (CMRR)

CMRR is the measure of rejection of variations in the input common-mode voltage of the ADC. If ΔVcm is the change in the input common-mode voltage and ΔV_{OUT} is the resultant change in the ADC output code (referred to the input), then

$$CMRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \quad (11)$$

Voltage Overload Recovery

The number of clock cycles taken to recover to less than 1% error for a 6-dB overload on the analog inputs. A 6-dBFS sine wave at Nyquist frequency is used as the test stimulus.

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REVISION HISTORY

Changes from Revision A (February 2008) to Revision B **Page**

- Changed Data setup time from 1.7 to 0.6 8
- Changed Data setup time from 2.3 to 1.5 8
- Changed Data setup time from 2.5 to 1.0 8
- Changed Data setup time from 3.1 to 2.3 8
- Changed Data setup time from 3.9 to 2.4 8
- Changed Data setup time from 4.5 to 3.8 8
- Changed Data setup time from 5.4 to 3.8 8
- Changed Data setup time from 6.0 to 5.2 8
- Changed Data hold time from 0.7 to 1.0 8
- Changed Data hold time from 1.7 to 2.3 8
- Changed Data hold time from 0.7 to 1.0 8
- Changed Data hold time from 1.7 to 2.3 8
- Changed Data hold time from 0.7 to 1.0 8
- Changed Data hold time from 1.7 to 2.3 8
- Changed Data hold time from 0.7 to 1.0 8
- Changed Data hold time from 1.7 to 2.3 8
- Changed Clock propagation delay from 4.3 to 3.5 8
- Changed Clock propagation delay from 5.8 to 5.5 8
- Changed Clock propagation delay from 7.3 to 7.5 8
- Changed Clock propagation delay from 4.3 to 3.5 8
- Changed Clock propagation delay from 5.8 to 5.5 8
- Changed Clock propagation delay from 7.3 to 7.5 8
- Changed Clock propagation delay from 4.3 to 3.5 8
- Changed Clock propagation delay from 5.8 to 5.5 8
- Changed Clock propagation delay from 7.3 to 7.5 8
- Changed Clock propagation delay from 4.3 to 3.5 8
- Changed Clock propagation delay from 5.8 to 5.5 8
- Changed Clock propagation delay from 7.3 to 7.5 8
- Changed LVDS bit clock duty cycle from 40% to 46% 8
- Changed LVDS bit clock duty cycle from 47% to 50% 8
- Changed LVDS bit clock duty cycle from 55% to 53% 8
- Changed LVDS bit clock duty cycle from 40% to 46% 8
- Changed LVDS bit clock duty cycle from 47% to 50% 8
- Changed LVDS bit clock duty cycle from 55% to 53% 8
- Changed LVDS bit clock duty cycle from 40% to 46% 8
- Changed LVDS bit clock duty cycle from 47% to 50% 8
- Changed LVDS bit clock duty cycle from 55% to 53% 8
- Changed LVDS bit clock duty cycle from 40% to 46% 8
- Changed LVDS bit clock duty cycle from 47% to 50% 8
- Changed LVDS bit clock duty cycle from 55% to 53% 8
- Changed Data setup time from 2.9 to 2.0 9
- Changed Data setup time from 4.4 to 3.5 9
- Changed Data setup time from 3.6 to 2.8 9
- Changed Data setup time from 5.1 to 4.3 9

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- Changed Data setup time from 5.1 to 4.3 9
- Changed Data setup time from 6.6 to 5.8 9
- Changed Data setup time from 6.5 to 5.7 9
- Changed Data setup time from 8.0 to 7.2 9
- Changed Data hold time from 1.3 to 2.0 9
- Changed Data hold time from 2.7 to 3.5 9
- Changed Data hold time from 2.1 to 2.7 9
- Changed Data hold time from 3.5 to 4.2 9
- Changed Data hold time from 3.6 to 4.2 9
- Changed Data hold time from 5.0 to 5.7 9
- Changed Data hold time from 5.1 to 5.6 9
- Changed Data hold time from 6.5 to 7.1 9
- Changed Clock propagation delay from 5 to 5.8 9
- Changed Clock propagation delay from 6.5 to 7.3 9
- Changed Clock propagation delay from 7.9 to 8.8 9
- Changed Clock propagation delay from 5 to 5.8 9
- Changed Clock propagation delay from 6.5 to 7.3 9
- Changed Clock propagation delay from 7.9 to 8.8 9
- Changed Clock propagation delay from 5 to 5.8 9
- Changed Clock propagation delay from 6.5 to 7.3 9
- Changed Clock propagation delay from 7.9 to 8.8 9
- Changed Clock propagation delay from 5 to 5.8 9
- Changed Clock propagation delay from 6.5 to 7.3 9
- Changed Clock propagation delay from 7.9 to 8.8 9
- Changed Output clock duty cycle from 50% to 53% 9
- Changed Output clock duty cycle from 55% to 60% 9
- Changed Output clock duty cycle from 50% to 53% 9
- Changed Output clock duty cycle from 55% to 60% 9
- Changed Output clock duty cycle from 50% to 53% 9
- Changed Output clock duty cycle from 55% to 60% 9
- Changed Output clock duty cycle from 50% to 53% 9
- Changed Output clock duty cycle from 55% to 60% 9
- Changed Data rise time/Data fall time from 0.8 to 1.0 9
- Changed Data rise time/Data fall time from 1.5 to 1.8 9
- Changed Data rise time/Data fall time from 2.4 to 2.5 9
- Changed Data rise time/Data fall time from 0.8 to 1.0 9
- Changed Data rise time/Data fall time from 1.5 to 1.8 9
- Changed Data rise time/Data fall time from 2.4 to 2.5 9
- Changed Data rise time/Data fall time from 0.8 to 1.0 9
- Changed Data rise time/Data fall time from 1.5 to 1.8 9
- Changed Data rise time/Data fall time from 2.4 to 2.5 9
- Changed Data rise time/Data fall time from 0.8 to 1.0 9
- Changed Data rise time/Data fall time from 1.5 to 1.8 9
- Changed Data rise time/Data fall time from 2.4 to 2.5 9
- Changed Output clock rise time/Output clock fall time from 0.8 to 1.0 9
- Changed Output clock rise time/Output clock fall time from 1.5 to 1.8 9
- Changed Output clock rise time/Output clock fall time from 2.4 to 2.5 9

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- Changed Output clock rise time/Output clock fall time from 0.8 to 1.0 9
- Changed Output clock rise time/Output clock fall time from 1.5 to 1.8 9
- Changed Output clock rise time/Output clock fall time from 2.4 to 2.5 9
- Changed Output clock rise time/Output clock fall time from 0.8 to 1.0 9
- Changed Output clock rise time/Output clock fall time from 1.5 to 1.8 9
- Changed Output clock rise time/Output clock fall time from 2.4 to 2.5 9
- Changed Output clock rise time/Output clock fall time from 0.8 to 1.0 9
- Changed Output clock rise time/Output clock fall time from 1.5 to 1.8 9
- Changed Output clock rise time/Output clock fall time from 2.4 to 2.5 9
- Added PARALLEL CMOS INTERFACE, DRVDD = 1.8 V, maximum buffer drive strength timing characteristics 9
- Added PARALLEL CMOS INTERFACE, DRVDD = 1.8 V, MULTIPLEXED MODE, maximum buffer drive strength timing characteristics 10
- Changed DB10 to DB0 pins to DB11 to DB0 pins in Table 6 14
- Changed DA10 to DA0 pins to DB11 to DB0 pins in D2-D0 bit description 20
- Changed DA13 to DA0 pins to DB11 to DB0 pins in Table 21 51

Changes from Revision B (December 2008) to Revision C **Page**

- Changed pins 19, 20 and 29, 30 25
- Changed pins 19, 20 and 29, 30 27

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS62P22IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ62P22	Samples
ADS62P22IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ62P22	Samples
ADS62P23IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ62P23	Samples
ADS62P23IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ62P23	Samples
ADS62P24IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ62P24	Samples
ADS62P24IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ62P24	Samples
ADS62P25IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ62P25	Samples
ADS62P25IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ62P25	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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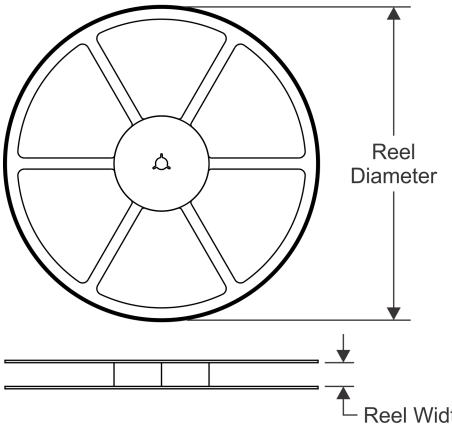
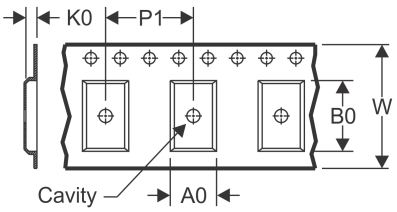
TAPE AND REEL INFORMATION

REEL DIMENSIONS

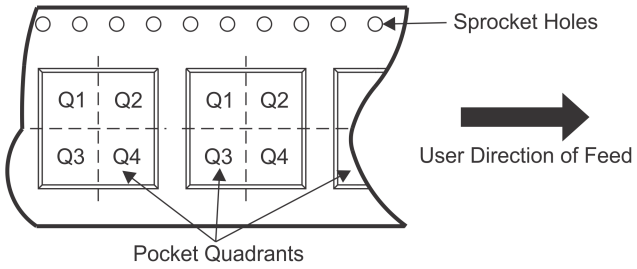


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

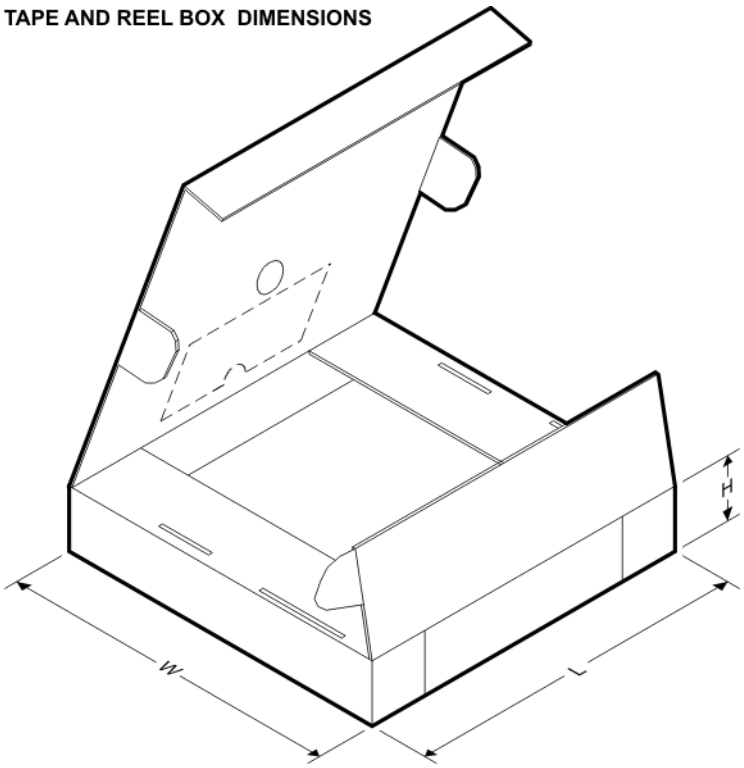
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS62P22IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS62P22IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS62P23IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS62P23IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS62P24IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS62P24IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS62P25IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS62P25IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

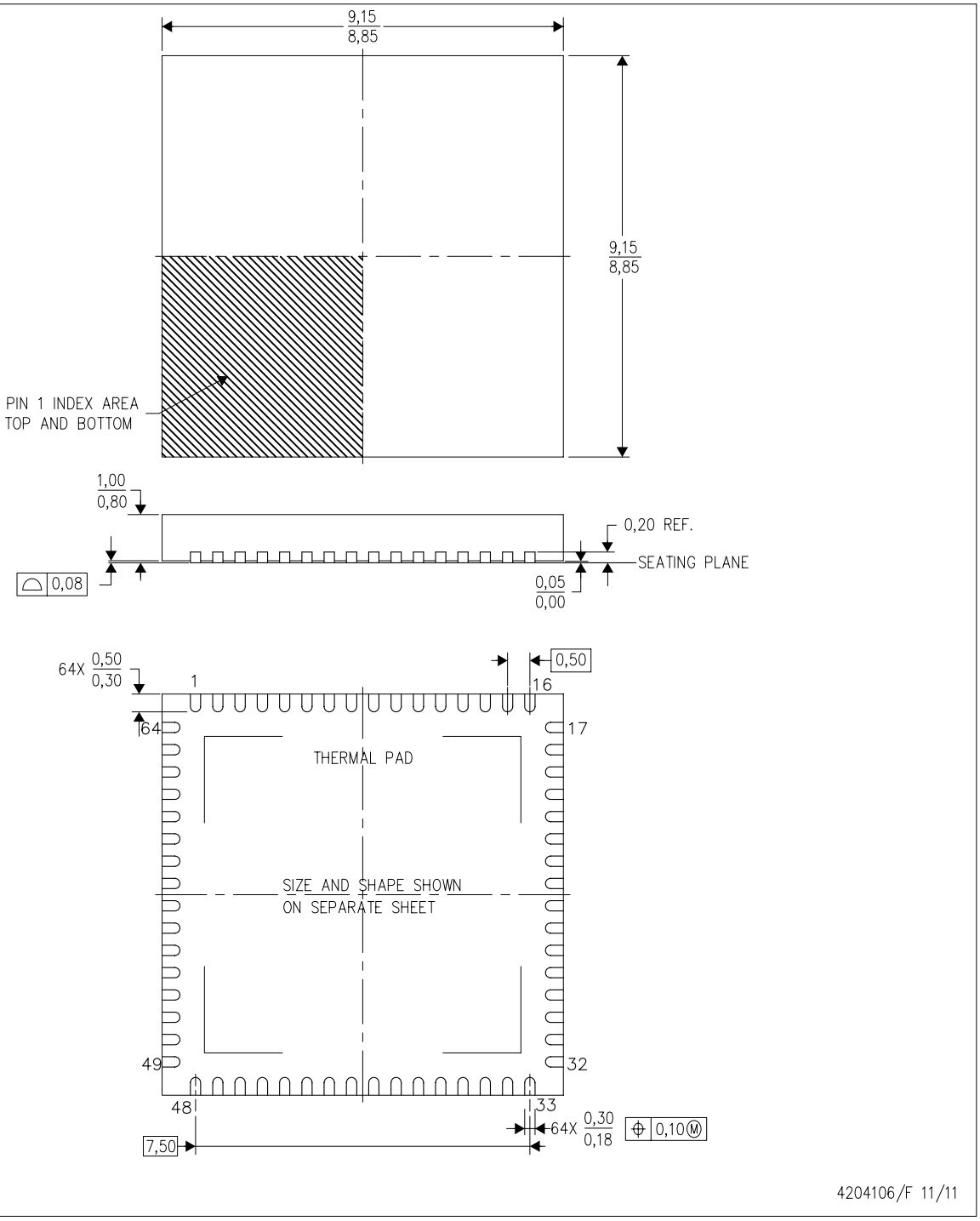
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS62P22IRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
ADS62P22IRGCT	VQFN	RGC	64	250	213.0	191.0	55.0
ADS62P23IRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
ADS62P23IRGCT	VQFN	RGC	64	250	213.0	191.0	55.0
ADS62P24IRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
ADS62P24IRGCT	VQFN	RGC	64	250	213.0	191.0	55.0
ADS62P25IRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
ADS62P25IRGCT	VQFN	RGC	64	250	213.0	191.0	55.0

RGC(S–PVQFN–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

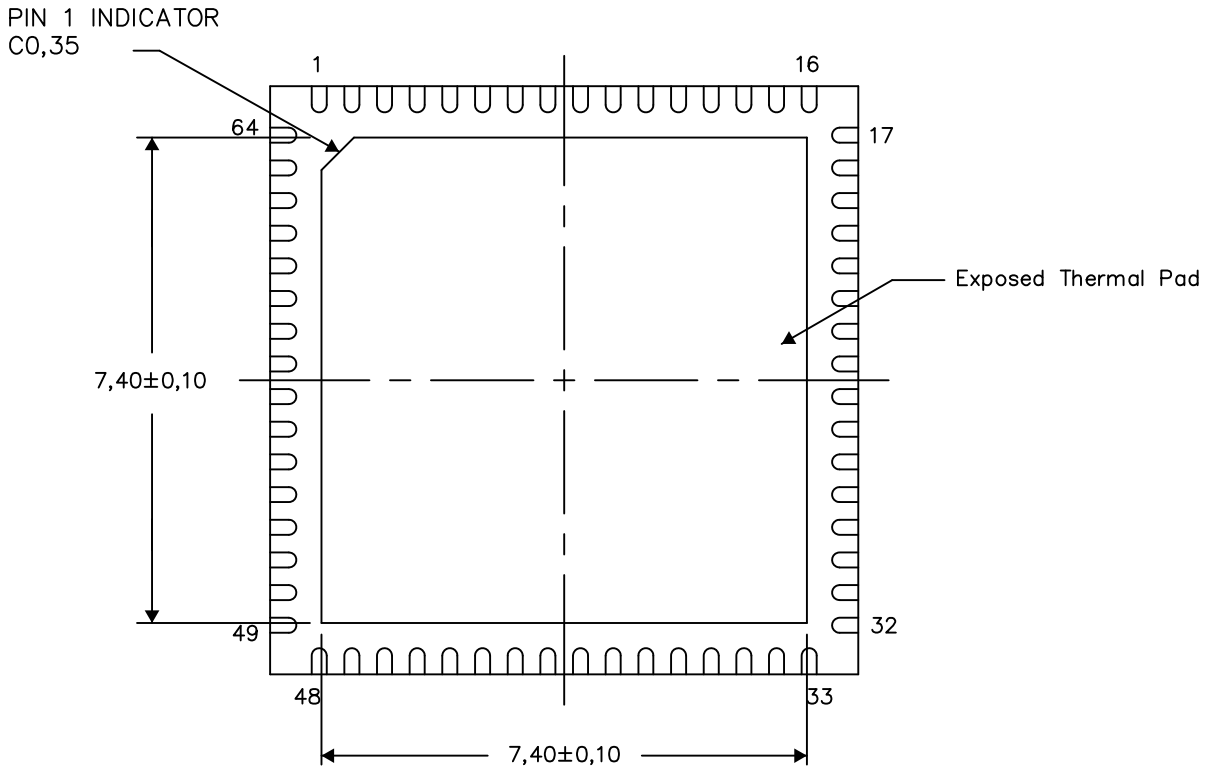
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



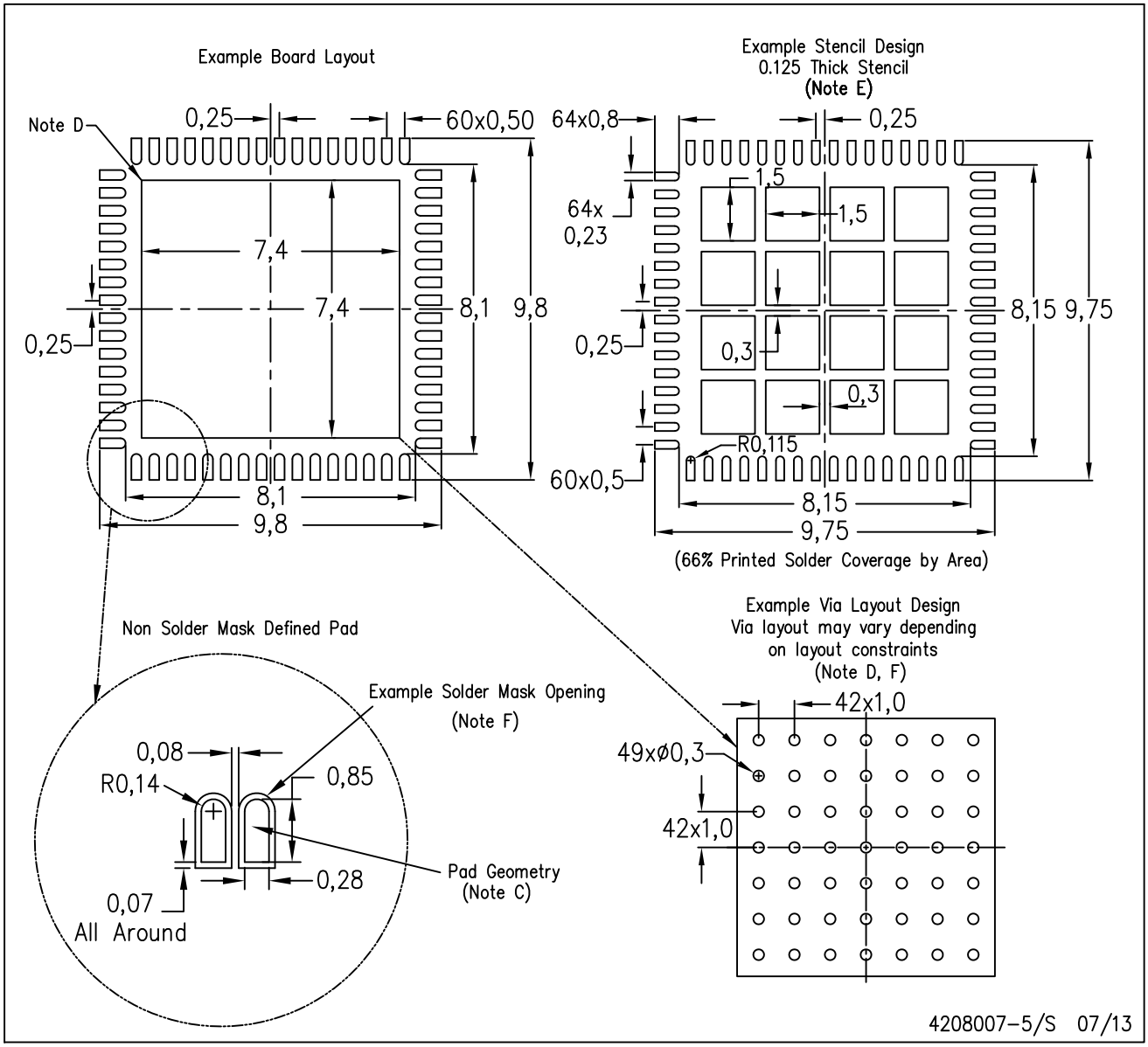
Bottom View

Exposed Thermal Pad Dimensions

4206192–4/AC 10/13

NOTE: A. All linear dimensions are in millimeters

RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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