TEXAS INSTRUMENTS

AMC1303E0510, AMC1303M0510, AMC1303E0520, AMC1303M0520
AMC1303E2510, AMC1303M2510, AMC1303E2520, AMC1303M2520

SBAS771B – JUNE 2017 – REVISED JUNE 2018

AMC1303x Small, High-Precision, Reinforced Isolated Delta-Sigma Modulators With Internal Clock

1 Features

- Pin-Compatible Family Optimized for Shunt-Resistor-Based Current Measurements:
  - ±50-mV or ±250-mV Input Voltage Ranges
  - Manchester Coded or Uncoded Bitstream Options
  - 10-MHz and 20-MHz Clock Options
- Excellent DC Performance:
  - Offset Error: ±50 µV or ±100 µV (max)
  - Offset Drift: ±1 µV/°C (max)
  - Gain Error: ±0.2% (max)
  - Gain Drift: ±40 ppm/°C (max)
- Transient Immunity: 100 kV/µs (typ)
- System-Level Diagnostic Features
- Safety-Related Certifications:
  - 7000-V_{PK} Reinforced Isolation per DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01
  - 5000-V_{RMS} Isolation for 1 Minute per UL1577
  - CAN/CSA No. 5A-Component Acceptance Service Notice, IEC 60950-1, and IEC 60065 End Equipment Standards
- Fully Specified Over the Extended Industrial Temperature Range: –40°C to +125°C

2 Applications

- Shunt-Resistor-Based Current Sensing and Isolated Voltage Measurement in:
  - Industrial Motor Drives
  - Photovoltaic Inverters
  - Uninterruptible and Isolated Power Supplies
  - Power Factor Correction Circuits

3 Description

The AMC1303 (AMC1303x0510, AMC1303x0520, AMC1303x2510, and AMC1303x2520) is a family of precision, delta-sigma (ΔΣ) modulators with the output separated from the input circuitry by a capacitive double isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 7000 V_{PK} according to the DIN V VDE V 0884-11 and UL1577 standards. Used in conjunction with isolated power supplies, this isolated modulator separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage.

The input of the AMC1303 is optimized for direct connection to shunt resistors or other low voltage-level signal sources. The ±50-mV input voltage range option allows significant reduction of the power dissipation through the shunt. The output bit-stream of the AMC1303 is synchronized to the internally generated clock and is Manchester coded (AMC1303Ex) or uncoded (AMC1303Mx). By using an integrated digital filter (such as those in the TMS320F2807x or TMS320F2837x microcontroller families) to decimate the bitstream, the device can achieve 16 bits of resolution with a dynamic range of 85 dB at an effective output data rate of 78 kSPS.

The bitstream output of the Manchester coded AMC1303Ex versions supports single-wire data and clock transfer without having to consider the setup and hold time requirements of the receiving device.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC1303x	SOIC (8)	5.85 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

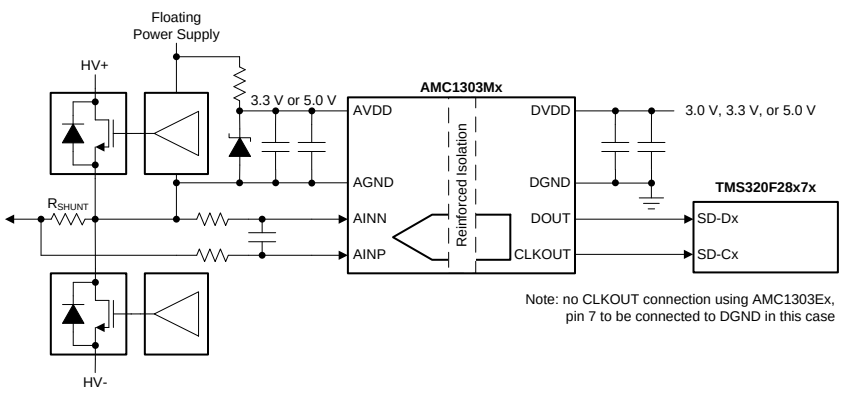


Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Device Comparison Table ... 3
6 Pin Configuration and Functions ... 3
7 Specifications ... 4
7.1 Absolute Maximum Ratings ... 4
7.2 ESD Ratings ... 4
7.3 Recommended Operating Conditions ... 4
7.4 Thermal Information ... 4
7.5 Power Ratings ... 4
7.6 Insulation Specifications ... 5
7.7 Safety-Related Certifications ... 6
7.8 Safety Limiting Values ... 6
7.9 Electrical Characteristics: AMC1303x05x ... 7
7.10 Electrical Characteristics: AMC1303x25x ... 9
7.11 Switching Characteristics ... 11
7.12 Insulation Characteristics Curves ... 12
7.13 Typical Characteristics ... 13
8 Detailed Description ... 19
8.1 Overview ... 19
8.2 Functional Block Diagram ... 19
8.3 Feature Description ... 20
8.4 Device Functional Modes ... 24
9 Application and Implementation ... 25
9.1 Application Information ... 25
9.2 Typical Applications ... 26
10 Power Supply Recommendations ... 31
11 Layout ... 32
11.1 Layout Guidelines ... 32
11.2 Layout Example ... 32
12 Device and Documentation Support ... 33
12.1 Device Support ... 33
12.2 Documentation Support ... 33
12.3 Related Links ... 33
12.4 Receiving Notification of Documentation Updates 33
12.5 Community Resources ... 33
12.6 Trademarks ... 34
12.7 Electrostatic Discharge Caution ... 34
12.8 Glossary ... 34
13 Mechanical, Packaging, and Orderable Information ... 34

4 Revision History

Changes from Revision A (July 2017) to Revision B **Page**

- Changed *Reinforced Isolation Capacitor Lifetime Projection* figure ... 12

Changes from Original (June 2017) to Revision A **Page**

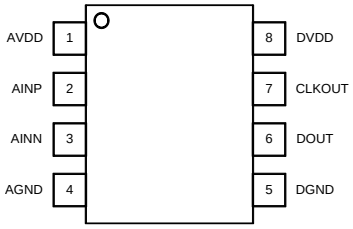
- Released AMC1303x05 devices to production ... 1
- Added Added ±50 μV to first *DC Performance* sub-bullet to reflect the AMC1303x05 devices ... 1
- Changed *prevent* to *minimize* in condition statement of *Safety Limiting Values* table ... 6
- Added *Electrical Characteristics: AMC1303x05x* table ... 7
- Added AMC13063x05 devices to *Typical Characteristics* section ... 13

5 Device Comparison Table

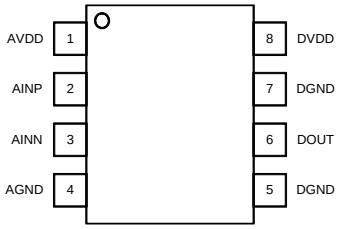
PART NUMBER	LINEAR INPUT VOLTAGE RANGE	DIFFERENTIAL INPUT RESISTANCE	DIGITAL OUTPUT INTERFACE	INTERNAL CLOCK FREQUENCY
AMC1303E0510	±50 mV	4.9 kΩ	Manchester coded CMOS	10 MHz
AMC1303E2510	±250 mV	22 kΩ	Manchester coded CMOS	
AMC1303M0510	±50 mV	4.9 kΩ	Uncoded CMOS	
AMC1303M2510	±250 mV	22 kΩ	Uncoded CMOS	
AMC1303E0520	±50 mV	4.9 kΩ	Manchester coded CMOS	20 MHz
AMC1303E2520	±250 mV	22 kΩ	Manchester coded CMOS	
AMC1303M0520	±50 mV	4.9 kΩ	Uncoded CMOS	
AMC1303M2520	±250 mV	22 kΩ	Uncoded CMOS	

6 Pin Configuration and Functions

AMC1303Mx: DWV Package
8-Pin SOIC
Top View



AMC1303Ex: DWV Package
8-Pin SOIC
Top View



Pin Functions

NAME	AMC1303Mx	AMC1303Ex	I/O	DESCRIPTION
AGND	4	4	—	Analog (high-side) ground reference
AINN	3	3	I	Inverting analog input
AINP	2	2	I	Noninverting analog input
AVDD	1	1	—	Analog (high-side) power supply, 3.0 V to 5.5 V. See the *Power Supply Recommendations* section for decoupling recommendations.
CLKOUT	7	—	O	Modulator clock output, 10 MHz (on AMC1303Mxx10) or 20 MHz (on AMC1303Mxx20) nominal
DGND	5	5	—	Digital (controller-side) ground reference
DGND	—	7	—	Connect this pin to the controller-side ground for AMC1303Ex derivates
DOUT	6	6	O	Modulator bitstream output. This pin is a Manchester coded output for the AMC1303Ex derivates.
DVDD	8	8	—	Digital (controller-side) power supply, 2.7 V to 5.5 V. See the *Power Supply Recommendations* section for decoupling recommendations.

7 Specifications

7.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
Supply voltage, AVDD to AGND or DVDD to DGND	–0.3	6.5	V
Analog input voltage at AINP, AINN	AGND – 6	AVDD + 0.5	V
Digital output voltage at DOUT, CLKOUT	DGND – 0.5	DVDD + 0.5	V
Input current to any pin except supply pins	–10	10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog (high-side) supply voltage (AVDD to AGND)	3.0	5.0	5.5	V
DVDD	Digital (controller-side) supply voltage (DVDD to DGND)	2.7	3.3	5.5	V
T_A	Operating ambient temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		AMC1303x DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	AMC1303Exxx20, AVDD = DVDD = 5.5 V			89.65	mW
		AMC1303Mxxx20, AVDD = DVDD = 5.5 V			93.50	
P_{D1}	Maximum power dissipation (high-side supply)	AMC1303xxx20, AVDD = 5.5 V			53.90	mW
P_{D2}	Maximum power dissipation (low-side supply)	AMC1303Exxx20, DVDD = 5.5 V			35.75	mW
		AMC1303Mxxx20, DVDD = 5.5 V			39.60	

7.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 9	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 9	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation (2 × 0.0105 mm)	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At ac voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At ac voltage (sine wave)	1500	V_{RMS}
		At dc voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	7000	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	8400	
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2-µs, 50-µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge(4)	Method a, after input/output safety test subgroup 2 / 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM} = 2545\ V_{PK}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM} = 3394\ V_{PK}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and type test, $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM} = 3977\ V_{PK}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.5 V_{PP} at 1 MHz	~1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	Ω
		V_{IO} = 500 V at T_S = 150°C	> 10^{9}	Ω
	Pollution degree		2	
	Climatic category		40/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 5000 V_{RMS} or 7000 V_{DC}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ = 6000 V_{RMS}, t = 1 s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

7.7 Safety-Related Certifications

VDE	UL
Certified according to DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output (I/O) circuitry. A failure of the I/O may allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current, see Figure 3	θ_{JA} = 112.2°C/W, VDD1 = VDD2 = 5.5 V, T_J = 150°C, T_A = 25°C			202.5	mA
		θ_{JA} = 112.2°C/W, VDD1 = VDD2 = 3.6 V, T_J = 150°C, T_A = 25°C			309.4	
P_S	Safety input, output, or total power, see Figure 4	θ_{JA} = 112.2°C/W, T_J = 150°C, T_A = 25°C			1114 (1)	mW
T_S	Maximum safety temperature				150	°C

(1) Input, output, or the sum of input and output power must not exceed this value.

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

7.9 Electrical Characteristics: AMC1303x05x

minimum and maximum specifications apply from T_A = –40°C to +125°C, AVDD = 3.0 V to 5.5 V, DVDD = 2.7 V to 5.5 V, AINP = –50 mV to 50 mV, AINN = AGND, and $sinc^3$ filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
$V_{Clipping}$	Differential input voltage before clipping output	V_{IN} = AINP – AINN		±64		mV
FSR	Specified linear differential full-scale	V_{IN} = AINP – AINN	–50		50	mV
	Absolute common-mode input voltage(1)	(AINP + AINN) / 2 to AGND	–2		AVDD	V
V_{CM}	Operating common-mode input voltage	(AINP + AINN) / 2 to AGND	–0.032		AVDD – 2.1	V
V_{CMov}	Common-mode overvoltage detection level	(AINP + AINN) / 2 to AGND	AVDD – 2			V
	Hysteresis of the common-mode overvoltage detection level			90		mV
C_{IN}	Single-ended input capacitance	AINN = AGND		4		pF
C_{IND}	Differential input capacitance			2		pF
R_{IN}	Single-ended input resistance	AINN = AGND		4.75		kΩ
R_{IND}	Differential input resistance			4.9		kΩ
I_{IB}	Input bias current	AINP = AINN = AGND, $I_{IB} = I_{IBP} + I_{IBN}$	–97	–72	–57	µA
I_{IO}	Input offset current			±10		nA
CMTI	Common-mode transient immunity		50	100		kV/µs
CMRR	Common-mode rejection ratio	AINP = AINN, f_{IN} = 0 Hz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–99		dB
		AINP = AINN, f_{IN} from 0.1 Hz to 50 kHz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–98		
PSRR	Power-supply rejection ratio	AINP = AINN = AGND, 3.0 V ≤ AVDD ≤ 5.5 V, at dc		–108		dB
		AINP = AINN = AGND, 3.0 V ≤ AVDD ≤ 5.5 V, 10 kHz, 100-mV ripple		–107		
BW	Input bandwidth(2)	AMC1303x0510		430		kHz
		AMC1303x0520		800		
DC ACCURACY						
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
INL	Integral nonlinearity(3)	Resolution: 16 bits	–4	±1	4	LSB
E_O	Offset error	Initial, at T_A = 25°C, AINP = AINN = AGND	–50	±2.5	50	µV
TCE_O	Offset error thermal drift(4)		–1	±0.25	1	µV/°C
E_G	Gain error	Initial, at T_A = 25°C	–0.2%	±0.005%	0.2%	
TCE_G	Gain error thermal drift(5)		–40	±20	40	ppm/°C
AC ACCURACY						
SNR	Signal-to-noise ratio	AMC1303x0510, f_{IN} = 35 Hz	81	84		dB
		AMC1303x0520, f_{IN} = 35 Hz	79	83		
THD	Total harmonic distortion	f_{IN} = 35 Hz		–97	–86	dB
SFDR	Spurious-free dynamic range	AMC1303x0510, f_{IN} = 35 Hz		96		dB
		AMC1303x0520, f_{IN} = 35 Hz		97		

(1) Steady-state voltage supported by the device in case of a system failure. See the specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the *Absolute Maximum Ratings* table.

(2) This parameter is the –3-dB, second-order, roll-off frequency of the integrated differential input amplifier to consider for antialiasing filter designs.

(3) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.

(4) Offset error drift is calculated using the box method as described by the following equation: $TCE_O = \frac{value_{MAX} - value_{MIN}}{TempRange}$.

(5) Gain error drift is calculated using the box method as described by the following equation: $TCE_G(ppm) = \left(\frac{value_{MAX} - value_{MIN}}{value \times TempRange}\right) \times 10^6$.

Electrical Characteristics: AMC1303x05x (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C, AVDD = 3.0 V to 5.5 V, DVDD = 2.7 V to 5.5 V, AINP = –50 mV to 50 mV, AINN = AGND, and $sinc^3$ filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL OUTPUTS (CMOS Logic)						
C_{LOAD}	Output load capacitance			30		pF
V_{OH}	High-level output voltage	I_{OH} = –20 µA	DVDD – 0.1			V
		I_{OH} = –4 mA	DVDD – 0.4			
V_{OL}	Low-level output voltage	I_{OL} = 20 µA			0.1	V
		I_{OL} = 4 mA			0.4	
POWER SUPPLY						
I_{AVDD}	High-side supply current	AMC1303x0510, 3.0 V ≤ AVDD ≤ 3.6 V		5.4	7.3	mA
		AMC1303x0510, 4.5 V ≤ AVDD ≤ 5.5 V		6.0	8.0	
		AMC1303x0520, 3.0 V ≤ AVDD ≤ 3.6 V		6.3	8.5	
		AMC1303x0520, 4.5 V ≤ AVDD ≤ 5.5 V		7.2	9.8	
I_{DVDD}	Controller-side supply current	AMC1303E0510, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		3.3	4.5	mA
		AMC1303E0510, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		3.6	5.0	
		AMC1303M0510, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		3.5	4.7	
		AMC1303M0510, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		3.9	5.4	
		AMC1303E0520, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		4.1	5.5	
		AMC1303E0520, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		4.7	6.5	
		AMC1303M0520, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		4.6	6.0	
		AMC1303M0520, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		5.4	7.2	

7.10 Electrical Characteristics: AMC1303x25x

minimum and maximum specifications apply from T_A = –40°C to +125°C, AVDD = 3.0 V to 5.5 V, DVDD = 2.7 V to 5.5 V, AINP = –250 mV to 250 mV, AINN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, AVDD = 5 V, and DVDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
$V_{Clipping}$	Differential input voltage before clipping output	V_{IN} = AINP – AINN		±320		mV
FSR	Specified linear differential full-scale	V_{IN} = AINP – AINN	–250		250	mV
	Absolute common-mode input voltage(1)	(AINP + AINN) / 2 to AGND	–2		AVDD	V
V_{CM}	Operating common-mode input voltage	(AINP + AINN) / 2 to AGND	–0.16		AVDD – 2.1	V
V_{CMov}	Common-mode overvoltage detection level	(AINP + AINN) / 2 to AGND	AVDD – 2			V
	Hysteresis of common-mode overvoltage detection level			90		mV
C_{IN}	Single-ended input capacitance	AINN = AGND		2		pF
C_{IND}	Differential input capacitance			1		pF
R_{IN}	Single-ended input resistance	AINN = AGND		19		kΩ
R_{IND}	Differential input resistance			22		kΩ
I_{IB}	Input bias current	AINP = AINN = AGND, $I_{IB} = I_{IBP} + I_{IBN}$	–82	–60	–48	µA
I_{IO}	Input offset current			±5		nA
CMTI	Common-mode transient immunity		50	100		kV/µs
CMRR	Common-mode rejection ratio	AINP = AINN, f_{IN} = 0 Hz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–98		dB
		AINP = AINN, f_{IN} from 0.1 Hz to 50 kHz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–98		
PSRR	Power-supply rejection ratio	AINP = AINN = AGND, 3.0 V ≤ AVDD ≤ 5.5 V, at dc		–97		dB
		AINP = AINN = AGND, 3.0 V ≤ AVDD ≤ 5.5 V, 10-kHz, 100-mV ripple		–94.5		
BW	Input bandwidth(2)	AMC1303x2510		510		kHz
		AMC1303x2520		900		
DC ACCURACY						
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
INL	Integral nonlinearity(3)	Resolution: 16 bits	–4	±1	4	LSB
E_O	Offset error	Initial, at T_A = 25°C, AINP = AINN = AGND	–100	±4.5	100	µV
TCE_O	Offset error thermal drift(4)		–1	±0.15	1	µV/°C
E_G	Gain error	Initial, at T_A = 25°C	–0.2%	–0.005%	0.2%	
TCE_G	Gain error thermal drift(5)		–40	±20	40	ppm/°C
AC ACCURACY						
SNR	Signal-to-noise ratio	AMC1303x2510, f_{IN} = 35 Hz	85	87		dB
		AMC1303x2520, f_{IN} = 35 Hz	84.5	86.5		
THD	Total harmonic distortion	AMC1303x2510, f_{IN} = 35 Hz		–97	–86	dB
		AMC1303x2520, f_{IN} = 35 Hz		–101	–86	
SFDR	Spurious-free dynamic range	f_{IN} = 35 Hz		98		dB

(1) Steady-state voltage supported by the device in case of a system failure. See the specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the *Absolute Maximum Ratings* table.

(2) This parameter is the –3-dB, second-order, roll-off frequency of the integrated differential input amplifier to consider for antialiasing filter designs.

(3) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.

(4) Offset error drift is calculated using the box method as described by the following equation: $$TCE_O = \frac{value_{MAX} - value_{MIN}}{TempRange}.$$

(5) Gain error drift is calculated using the box method as described by the following equation: $$TCE_G(ppm) = \left(\frac{value_{MAX} - value_{MIN}}{value \times TempRange}\right) \times 10^6$$

Electrical Characteristics: AMC1303x25x (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C, AVDD = 3.0 V to 5.5 V, DVDD = 2.7 V to 5.5 V, AINP = –250 mV to 250 mV, AINN = AGND, and $sinc^3$ filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, AVDD = 5 V, and DVDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL OUTPUTS (CMOS LOGIC)						
C_{LOAD}	Output load capacitance			30		pF
V_{OH}	High-level output voltage	I_{OH} = –20 µA	DVDD – 0.1			V
		I_{OH} = –4 mA	DVDD – 0.4			
V_{OL}	Low-level output voltage	I_{OL} = 20 µA			0.1	V
		I_{OL} = 4 mA			0.4	
POWER SUPPLY						
I_{AVDD}	High-side supply current	AMC1303x2510, 3.0 V ≤ AVDD ≤ 3.6 V		5.4	7.3	mA
		AMC1303x2510, 4.5 V ≤ AVDD ≤ 5.5 V		6.0	8.0	
		AMC1303x2520, 3.0 V ≤ AVDD ≤ 3.6 V		6.3	8.5	
		AMC1303x2520, 4.5 V ≤ AVDD ≤ 5.5 V		7.2	9.8	
I_{DVDD}	Controller-side supply current	AMC1303E2510, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		3.3	4.5	mA
		AMC1303E2510, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		3.6	5.0	
		AMC1303M2510, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		3.5	4.7	
		AMC1303M2510, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		3.9	5.4	
		AMC1303E2520, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		4.1	5.5	
		AMC1303E2520, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		4.7	6.5	
		AMC1303M2520, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		4.6	6.0	
		AMC1303M2520, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		5.4	7.2	

7.11 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLK}	Internal clock frequency, on the CLKOUT pin of the AMC1303Mx only	AMC1303Mxx10	9.6	10	10.4	MHz
		AMC1303Mxx20	19.2	20	20.8	
Duty Cycle	Internal clock duty cycle(1), on the CLKOUT pin of the AMC1303Mx only		45%	50%	55%	
t_h	DOUT hold time after rising edge of CLKOUT	AMC1303Mx, C_{LOAD} = 15 pF	7			ns
t_d	DOUT delay time after rising edge of CLKOUT	AMC1303Mx, C_{LOAD} = 15 pF			15	ns
t_r	DOUT, CLKOUT rise time	10% to 90%, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		0.8	3.5	ns
		10% to 90%, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		1.8	3.9	
t_f	DOUT, CLKOUT fall time	90% to 10%, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		0.8	3.5	ns
		90% to 10%, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		1.8	3.9	
t_{ASTART}	Analog startup time	AVDD step to 3.0 V with DVDD ≥ 2.7 V		0.5		ms

(1) Duty cycle values are specified by design.

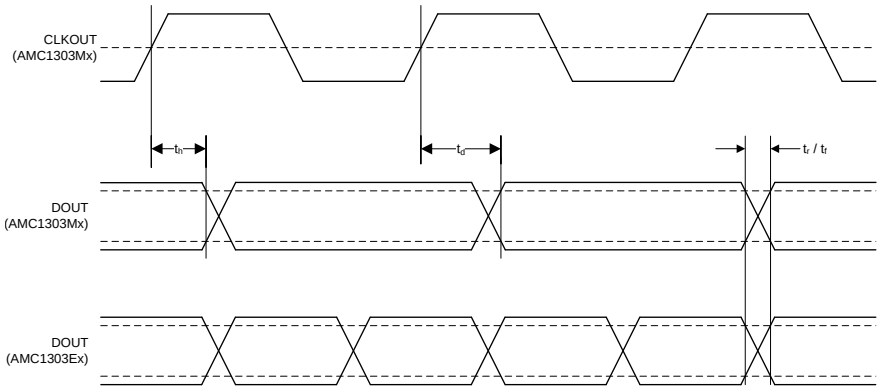


Figure 1. AMC1303Mx Digital Interface Timing

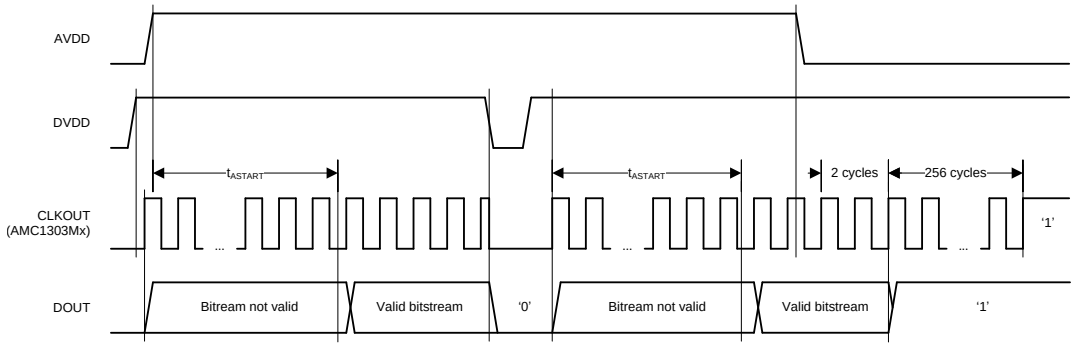


Figure 2. Digital Interface Startup Timing

7.12 Insulation Characteristics Curves

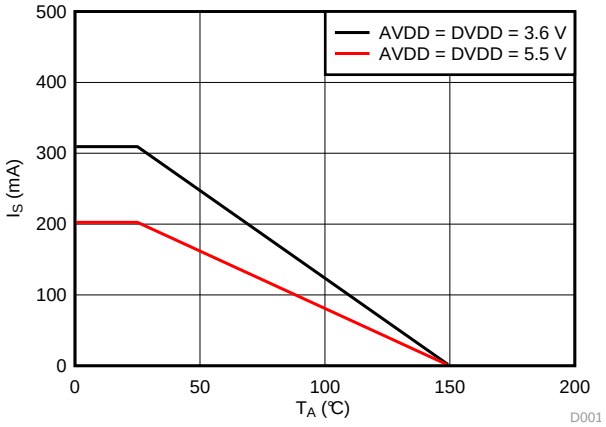


Figure 3. Thermal Derating Curve for Safety-Limiting Current per VDE

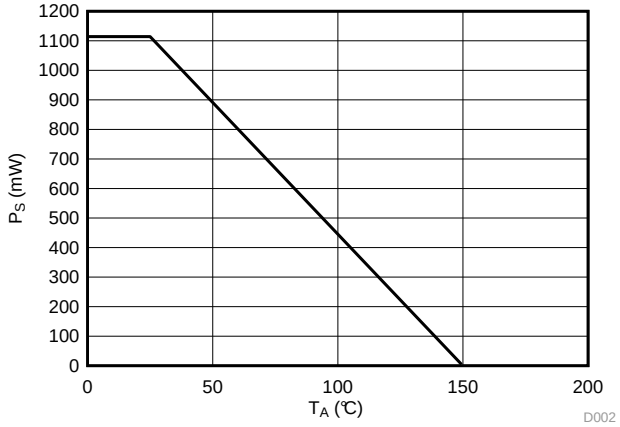
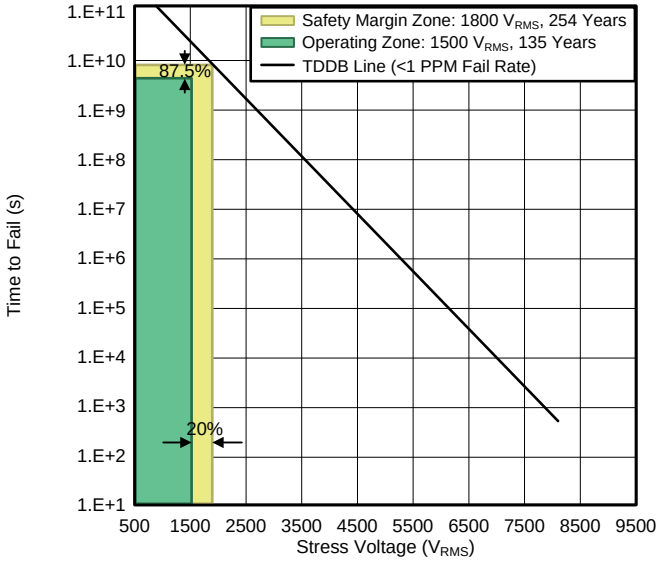


Figure 4. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60 Hz,
isolation working voltage = 1500 V_{RMS}, operating lifetime = 135 years

Figure 5. Reinforced Isolation Capacitor Lifetime Projection

7.13 Typical Characteristics

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1303x05x) or –250 mV to 250 mV (AMC1303x25x), AINN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted)

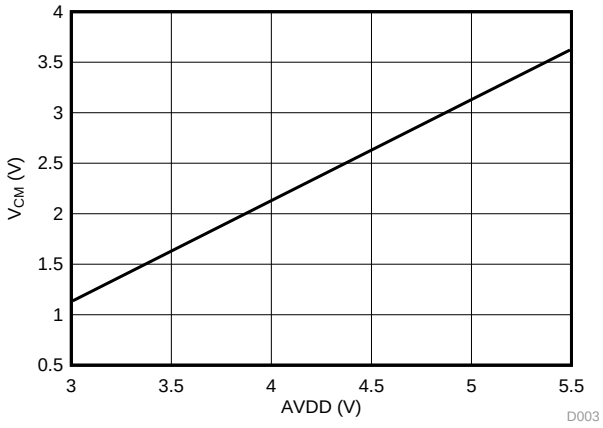


Figure 6. Maximum Operating Common-Mode Input Voltage vs High-Side Supply Voltage

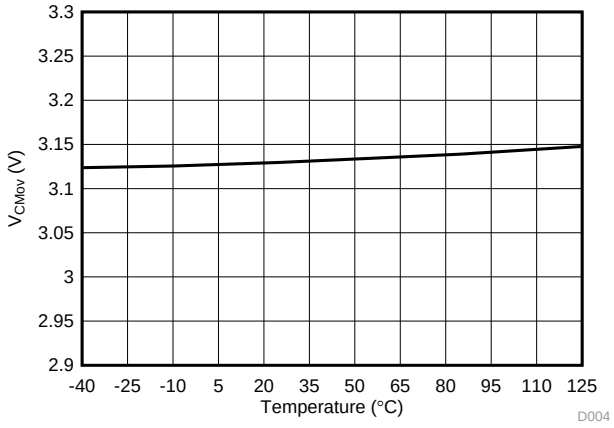


Figure 7. Common-Mode Overvoltage Detection Level vs Temperature

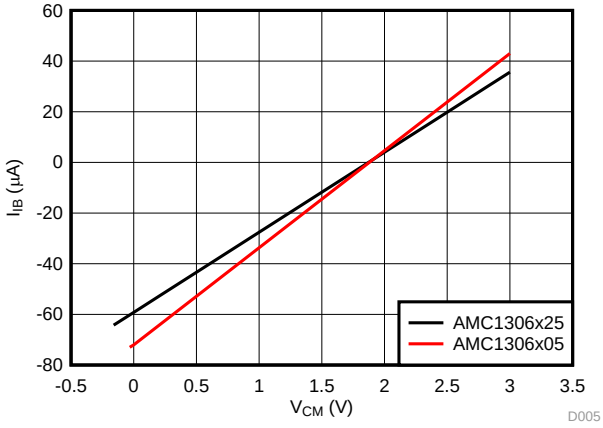


Figure 8. Input Bias Current vs Common-Mode Input Voltage

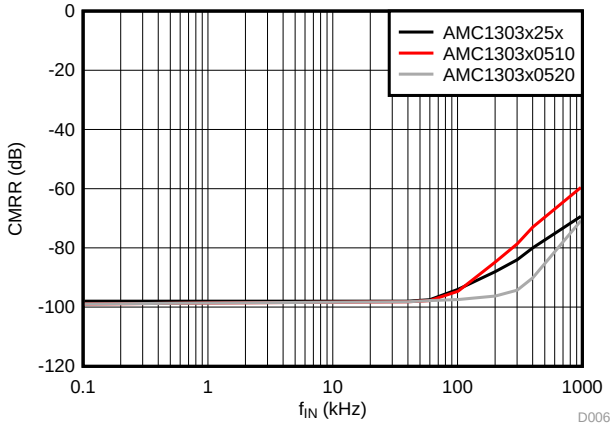


Figure 9. Common-Mode Rejection Ratio vs Input Signal Frequency

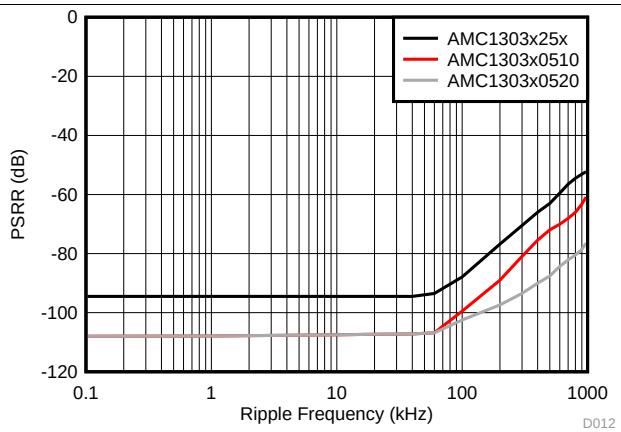


Figure 10. Power-Supply Rejection Ratio vs Ripple Frequency

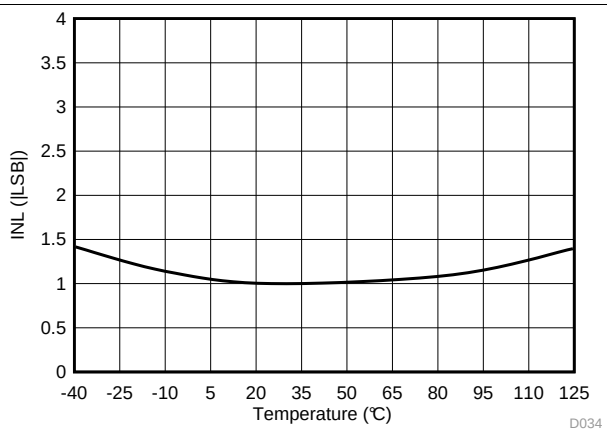


Figure 11. Integral Nonlinearity vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1303x05x) or –250 mV to 250 mV (AMC1303x25x), AINN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted)

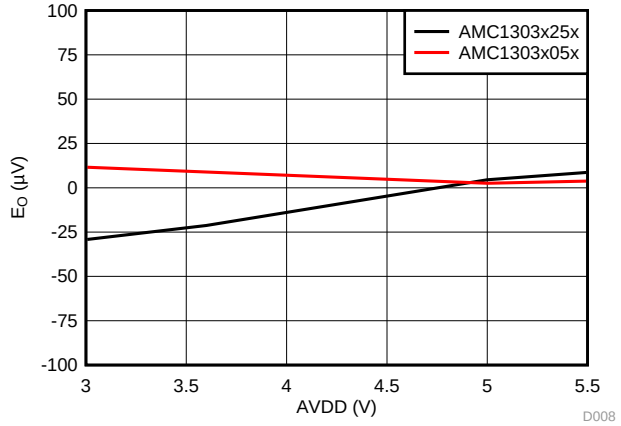


Figure 12. Offset Error vs High-Side Supply Voltage

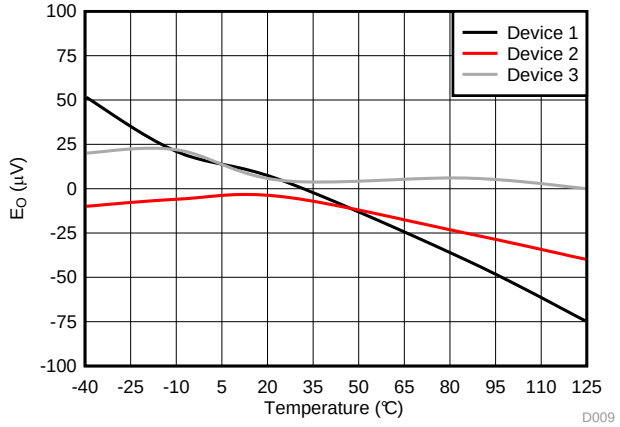


Figure 13. Offset Error vs Temperature

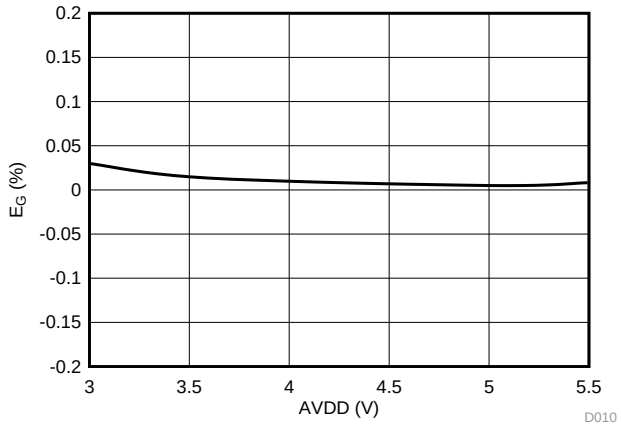


Figure 14. Gain Error vs High-Side Supply Voltage

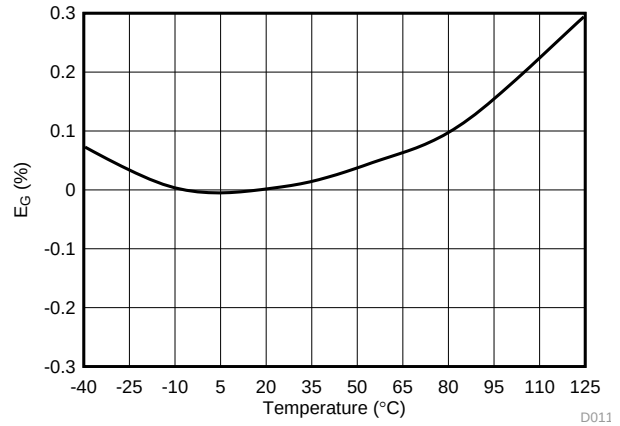


Figure 15. Gain Error vs Temperature

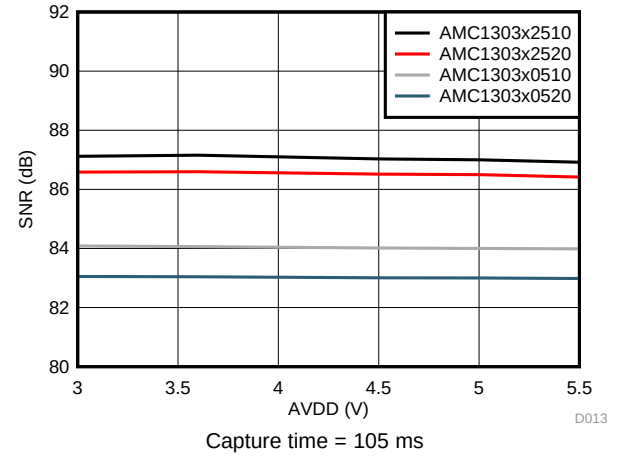


Figure 16. Signal-to-Noise Ratio vs High-Side Supply Voltage

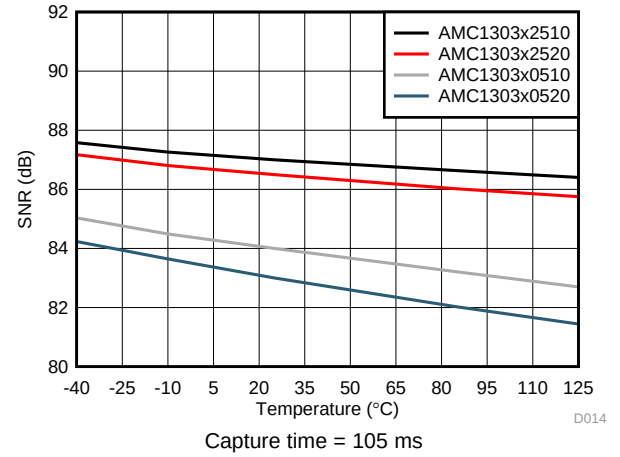
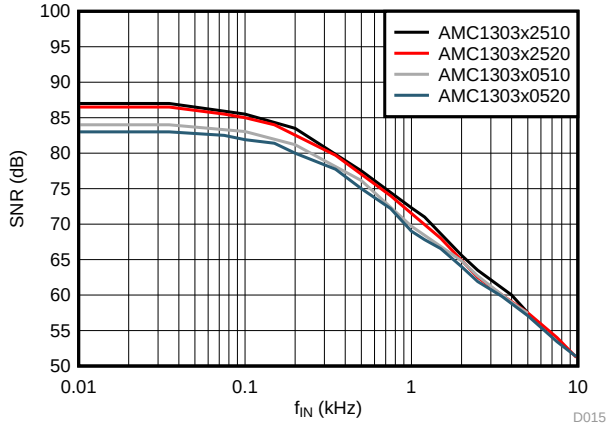


Figure 17. Signal-to-Noise Ratio vs Temperature

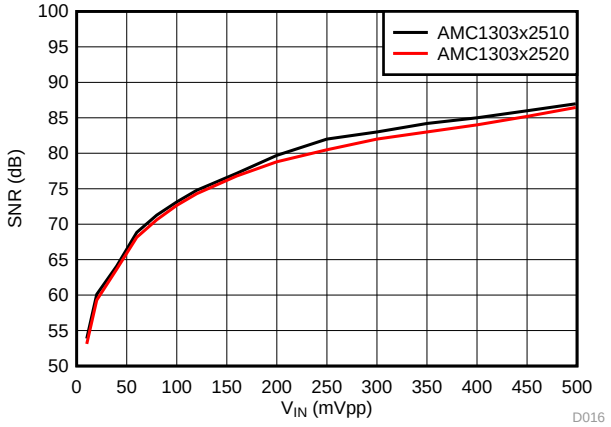
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1303x05x) or –250 mV to 250 mV (AMC1303x25x), AINN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted)



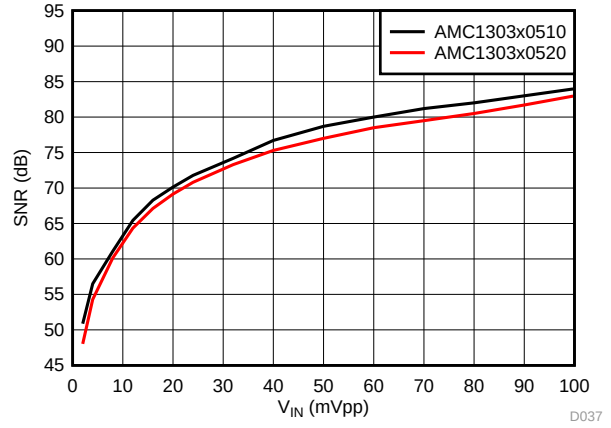
Capture time = 105 ms

Figure 18. Signal-to-Noise Ratio vs Input Signal Frequency



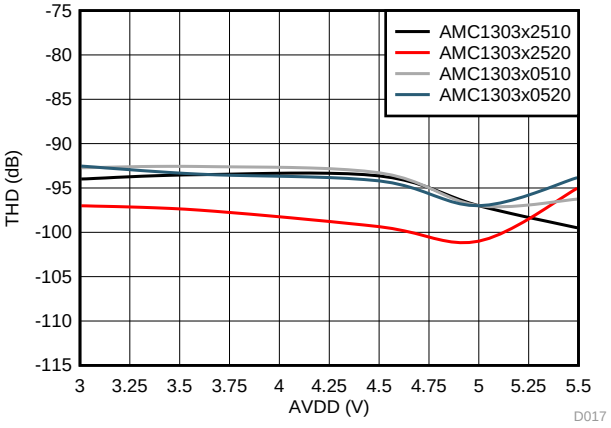
AMC1303x25x, capture time = 105 ms

Figure 19. Signal-to-Noise Ratio vs Input Signal Amplitude



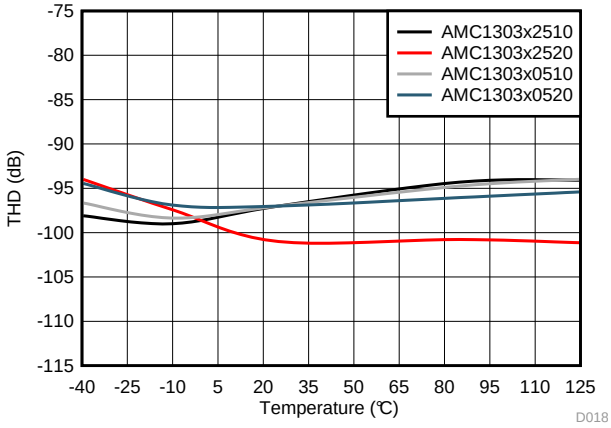
AMC1303x05x, capture time = 105 ms

Figure 20. Signal-to-Noise Ratio vs Input Signal Amplitude



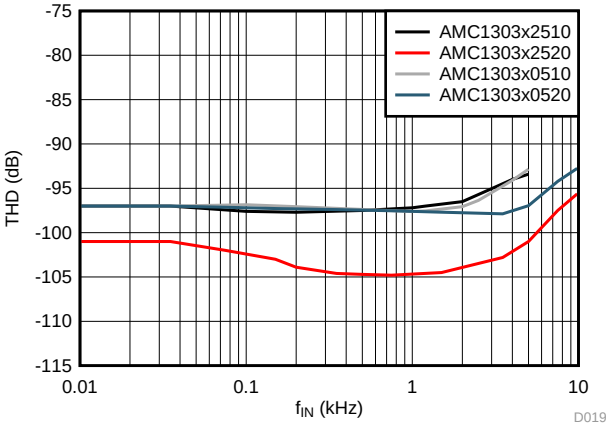
Capture time = 839 ms

Figure 21. Total Harmonic Distortion vs High-Side Supply Voltage



Capture time = 839 ms

Figure 22. Total Harmonic Distortion vs Temperature

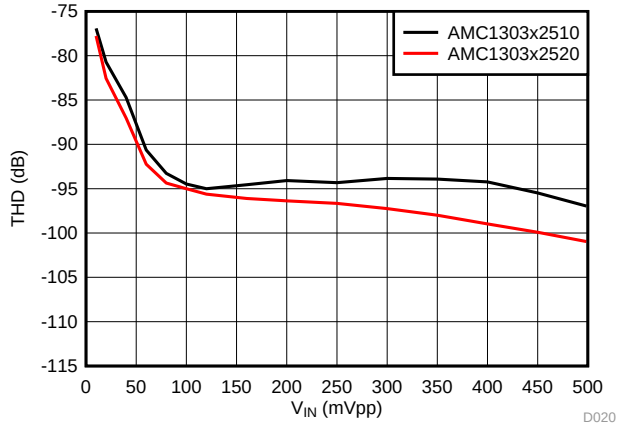


Capture time = 839 ms

Figure 23. Total Harmonic Distortion vs Input Signal Frequency

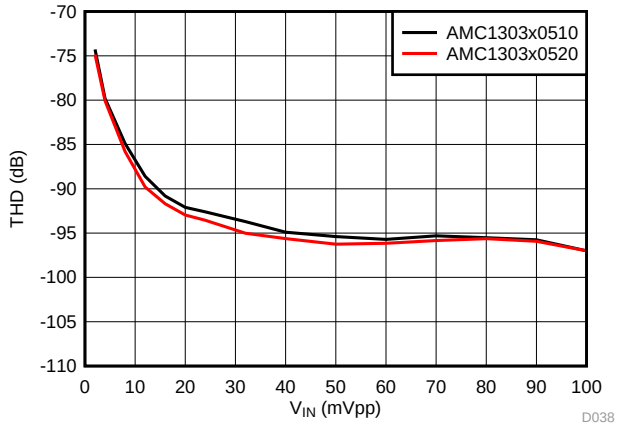
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1303x05x) or –250 mV to 250 mV (AMC1303x25x), AINN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted)



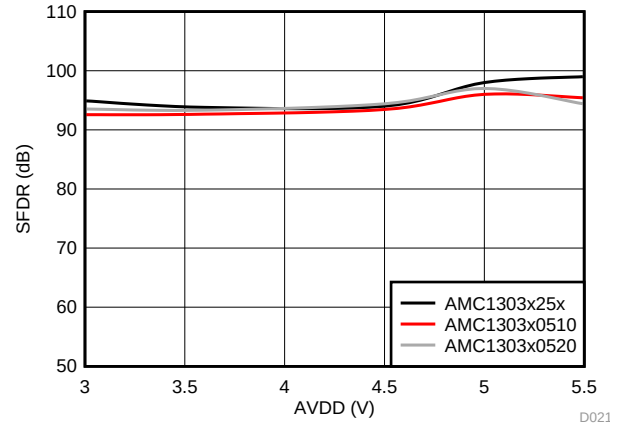
AMC1303x25x, capture time = 839 ms

Figure 24. Total Harmonic Distortion vs Input Signal Amplitude



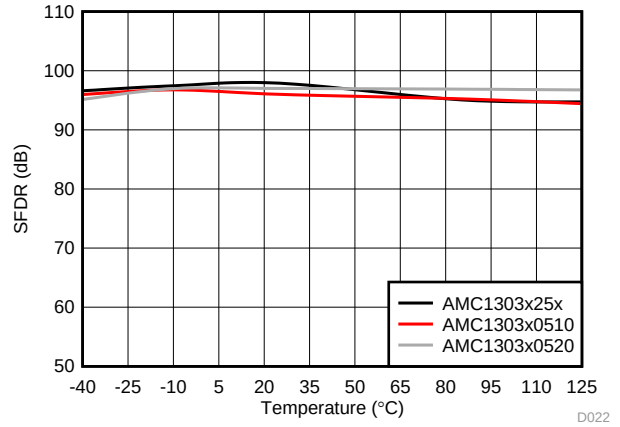
AMC1303x05x, capture time = 839 ms

Figure 25. Total Harmonic Distortion vs Input Signal Amplitude



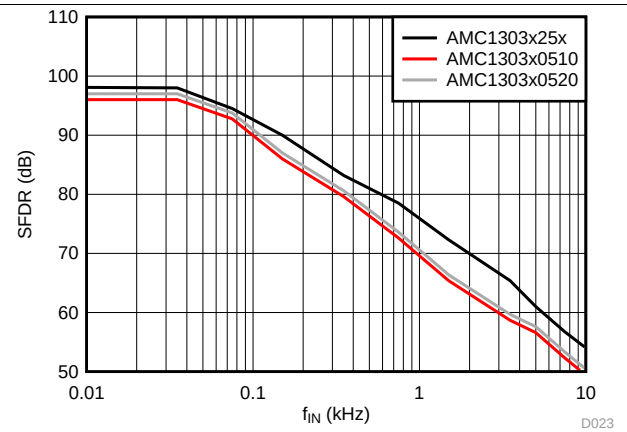
Capture time = 105 ms

Figure 26. Spurious-Free Dynamic Range vs High-Side Supply Voltage



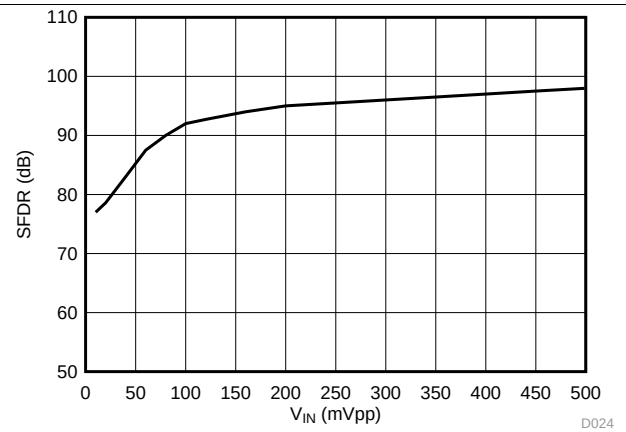
Capture time = 105 ms

Figure 27. Spurious-Free Dynamic Range vs Temperature



Capture time = 105 ms

Figure 28. Spurious-Free Dynamic Range vs Input Signal Frequency

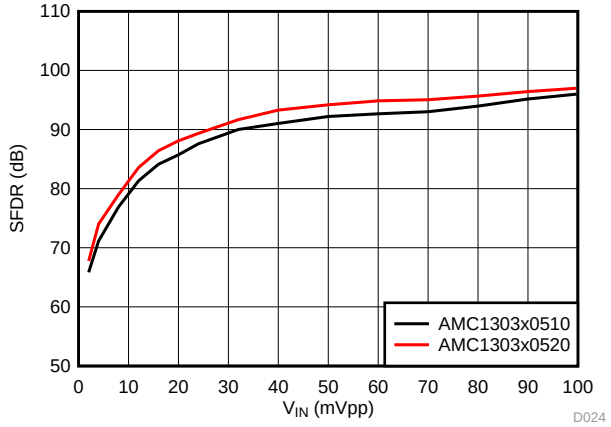


AMC1303x25x, capture time = 105 ms

Figure 29. Spurious-Free Dynamic Range vs Input Signal Amplitude

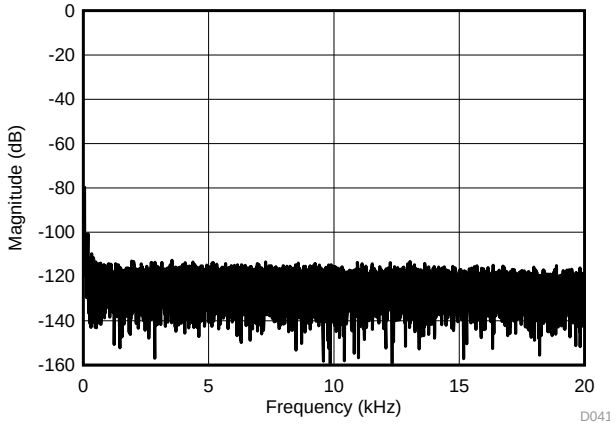
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1303x05x) or –250 mV to 250 mV (AMC1303x25x), AINN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted)



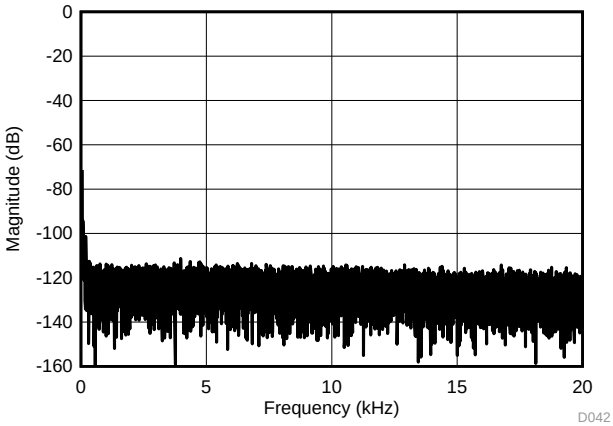
AMC1303x05x, capture time = 105 ms

Figure 30. Spurious-Free Dynamic Range vs Input Signal Amplitude



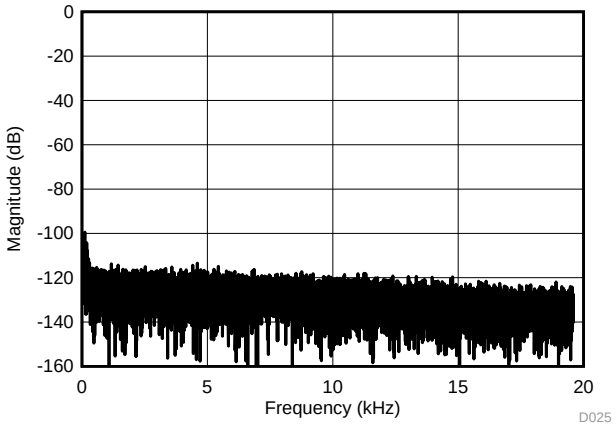
AMC1303x0510, capture time = 839 ms, V_{IN} = 100 mV_{PP}

Figure 31. Frequency Spectrum With 35-Hz Input Signal



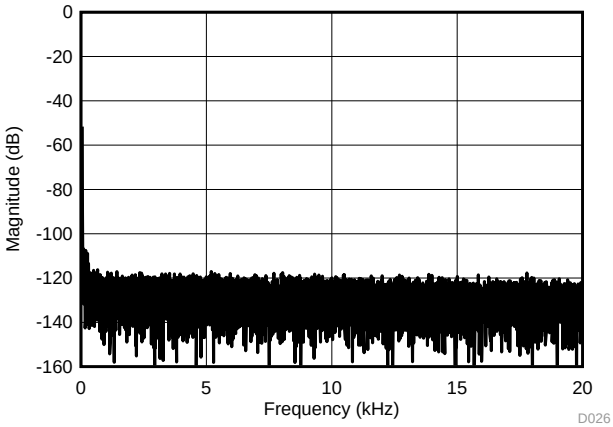
AMC1303x0520, capture time = 839 ms, V_{IN} = 100 mV_{PP}

Figure 32. Frequency Spectrum With 35-Hz Input Signal



AMC1303x2510, capture time = 839 ms, V_{IN} = 500 mV_{PP}

Figure 33. Frequency Spectrum With 35-Hz Input Signal



AMC1303x2520, capture time = 839 ms, V_{IN} = 500 mV_{PP}

Figure 34. Frequency Spectrum With 35-Hz Input Signal

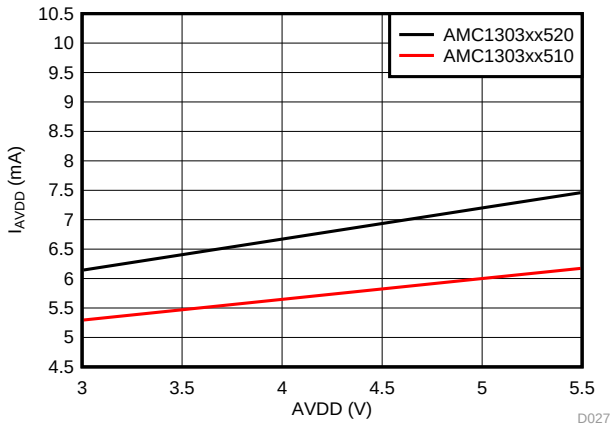


Figure 35. High-Side Supply Current vs High-Side Supply Voltage

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1303x05x) or –250 mV to 250 mV (AMC1303x25x), AINN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted)

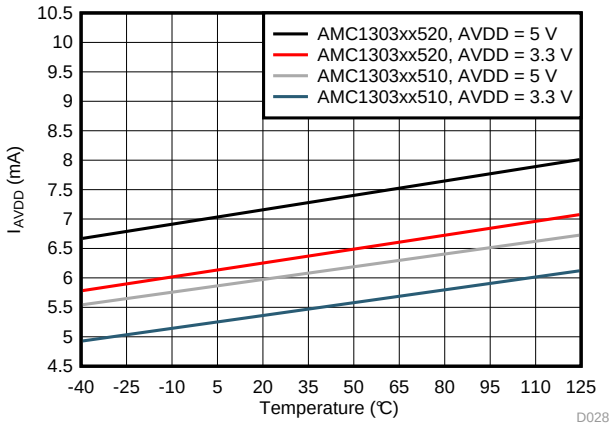


Figure 36. High-Side Supply Current vs Temperature

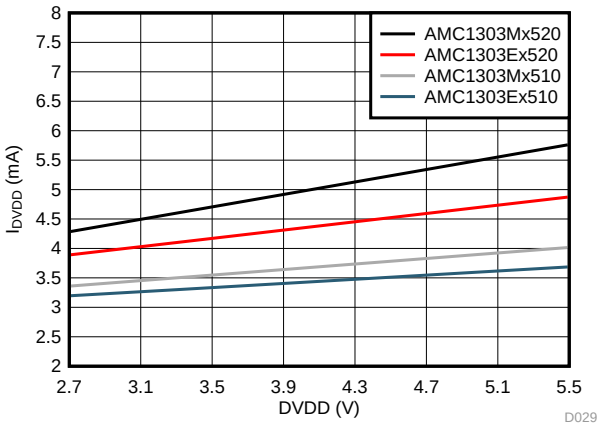


Figure 37. Controller-Side Supply Current vs Controller-Side Supply Voltage

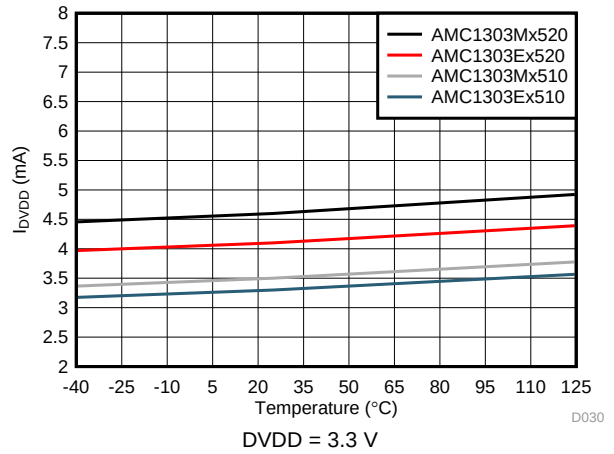


Figure 38. Controller-Side Supply Current vs Temperature

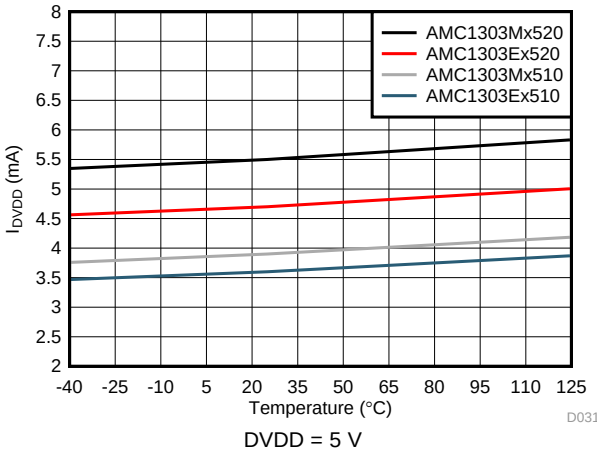


Figure 39. Controller-Side Supply Current vs Temperature

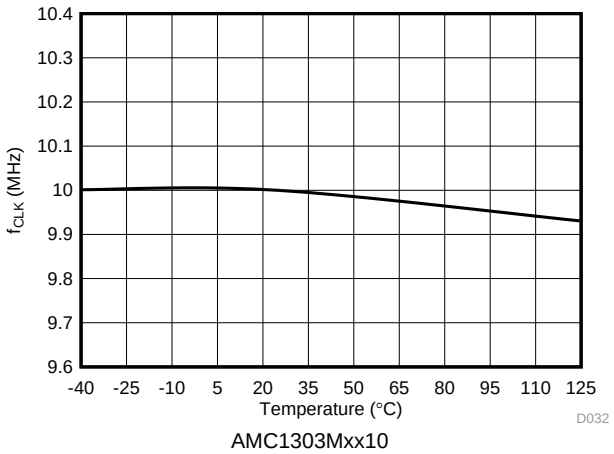


Figure 40. Output Clock Frequency vs Temperature

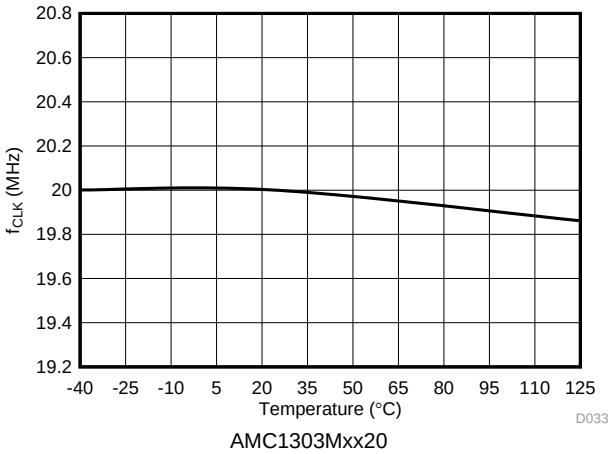


Figure 41. Output Clock Frequency vs Temperature

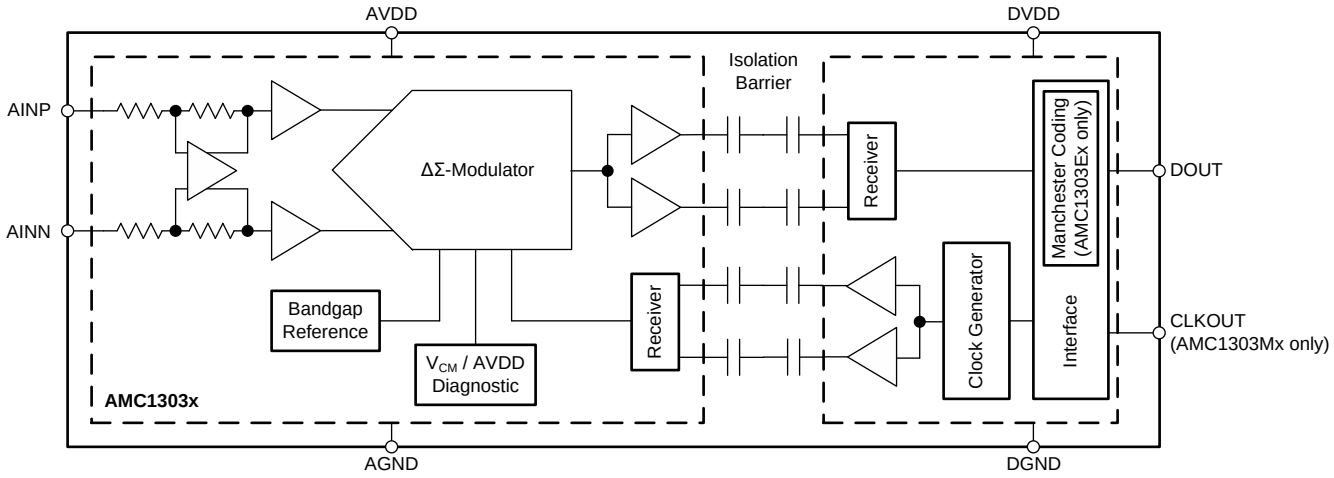
8 Detailed Description

8.1 Overview

The analog input stage of the AMC1303 is a fully differential amplifier feeding the switched-capacitor input of a second-order, delta-sigma (ΔΣ) modulator stage that digitizes the input signal into a 1-bit output stream. The isolated data output DOUT of the converter provides a stream of digital ones and zeros that is synchronous to the internally-generated clock at the CLKOUT pin (active on AMC1303Mx derivates only) with a frequency as specified in the *Switching Characteristics* table. The time average of this serial bit-stream output is proportional to the analog input voltage.

The *Functional Block Diagram* section shows a detailed block diagram of the AMC1303. The analog input range is tailored to directly accommodate a voltage drop across a shunt resistor used for current sensing. The SiO_2-based capacitive isolation barrier supports a high level of magnetic field immunity as described in the application report *ISO72x Digital Isolator Magnetic-Field Immunity* (SLLA181A), available for download at www.ti.com. The extended clock frequency of 20 MHz on the AMC1303xxx20 supports faster control loops and higher performance levels compared to the other solutions available on the market.

8.2 Functional Block Diagram

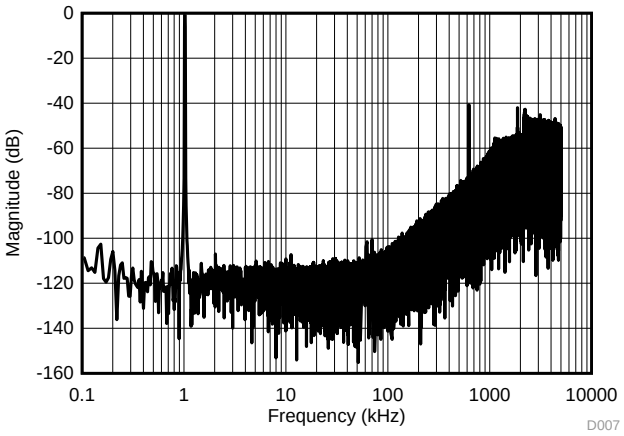


8.3 Feature Description

8.3.1 Analog Input

The AMC1303 incorporates a front-end circuitry that contains a differential amplifier and sampling stage, followed by a ΔΣ modulator. The gain of the differential amplifier is set by internal precision resistors to a factor of 4 for devices with a specified input voltage range of ±250 mV (for the AMC1303x25x), or to a factor of 20 in devices with a ±50-mV input voltage range (for the AMC1303x05x), resulting in a differential input resistance of 4.9 kΩ (for the AMC1303x05x) or 22 kΩ (for the AMC1303x25x).

For reduced offset and offset drift, the differential amplifier is chopper-stabilized with the switching frequency set at f_{CLK} / 32. Figure 42 shows that the switching frequency generates a spur.



AMC1303xxx20, $sinc^3$ filter, OSR = 2, f_{IN} = 1 kHz

Figure 42. Quantization Noise Shaping

Consider the input resistance of the AMC1303 in designs with high-impedance signal sources that can cause degradation of gain and offset specifications. The importance of this effect, however, depends on the desired system performance. Additionally, the input bias current caused by the internal common-mode voltage at the output of the differential amplifier causes an offset that is dependent on the actual amplitude of the input signal. See the *Isolated Voltage Sensing* section for more details on reducing these effects.

There are two restrictions on the analog input signals (AINP and AINN). First, if the input voltage exceeds the range AGND – 6 V to AVDD + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on. In addition, the linearity and noise performance of the device are ensured only when the differential analog input voltage remains within the specified linear full-scale range (FSR), that is ±250 mV (for the AMC1303x25x) or ±50 mV (for the AMC1303x05x), and within the specified input common-mode voltage range.

Feature Description (continued)

8.3.2 Modulator

The modulator implemented in the AMC1303 (such as the one conceptualized in Figure 43) is a second-order, switched-capacitor, feed-forward ΔΣ modulator. The analog input voltage V_{IN} and the output V_5 of the 1-bit digital-to-analog converter (DAC) are subtracted, providing an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage, resulting in output voltage V_3 that is subtracted from the input signal V_{IN} and the output of the first integrator V_2. Depending on the polarity of the resulting voltage V_4, the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage V_5, causing the integrators to progress in the opposite direction and forcing the value of the integrator output to track the average value of the input.

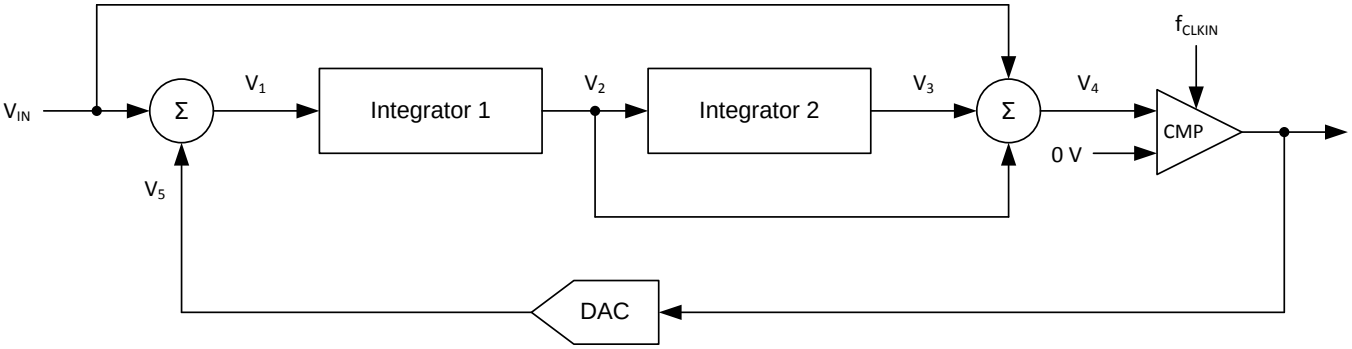


Figure 43. Block Diagram of a Second-Order Modulator

The modulator shifts the quantization noise to high frequencies; see Figure 42. Therefore, use a low-pass digital filter at the output of the device to increase the overall performance. This filter is also used to convert the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). TI's microcontroller families TMS320F2807x and TMS320F2837x offer a suitable programmable, hardwired filter structure called a *sigma-delta filter module* (SDFM) optimized for usage with the AMC1303 family. Also, SD24_B converters on the MSP430F677x microcontrollers offer a path to directly access the integrated sinc-filters, thus offering a system-level solution for multichannel, isolated current sensing. An additional option is to use a suitable application-specific device, such as the AMC1210 (a four-channel digital sinc-filter). Alternatively, a field-programmable gate array (FPGA) can be used to implement the filter.

Feature Description (continued)

8.3.3 Isolation Channel Signal Transmission

The AMC1303 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the capacitive SiO_2-based isolation barrier. The transmitter modulates the bitstream at TX IN in Figure 44 with an internally-generated, 480-MHz carrier across the isolation barrier to represent a digital *zero* and sends a *no signal* to represent the digital *one*. The receiver demodulates the signal after advanced signal conditioning and produces the output. The symmetrical design of each isolation channel improves the CMTI performance and reduces the radiated emissions caused by the high-frequency carrier. Figure 44 shows a block diagram of an isolation channel integrated in the AMC1303.

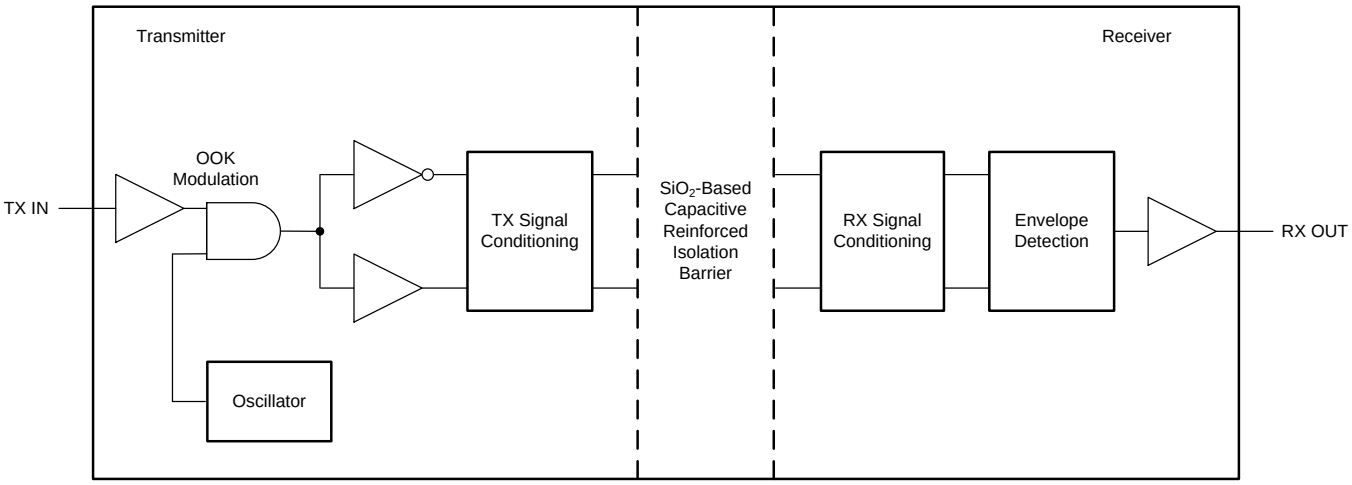


Figure 44. Block Diagram of an Isolation Channel

Figure 45 shows the concept of the on-off keying scheme.

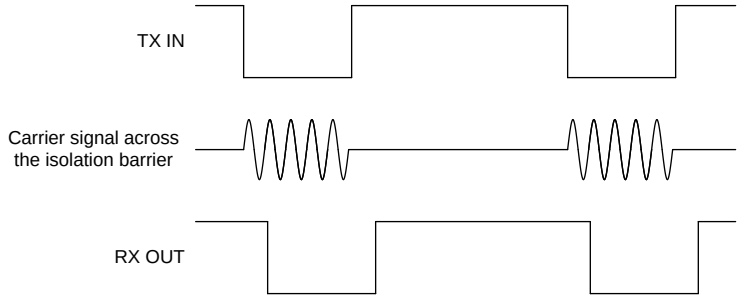


Figure 45. OOK-Based Modulation Scheme

Feature Description (continued)

8.3.4 Digital Output

A differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time. A differential input of 250 mV (for the AMC1303x25x) or 50 mV (for the AMC1303x05x) produces a stream of ones and zeros that are high 89.06% of the time. With 16 bits of resolution on the decimation filter, that percentage ideally corresponds to code 58368. A differential input of –250 mV (–50 mV for the AMC1303x05x) produces a stream of ones and zeros that are high 10.94% of the time and ideally results in code 7168 with a 16-bit resolution decimation filter. These input voltages are also the specified linear ranges of the different AMC1303 versions with performance as specified in this document. If the input voltage value exceeds these ranges, the output of the modulator shows nonlinear behavior where the quantization noise increases. The output of the modulator clips with a stream of only zeros with an input less than or equal to –320 mV (–64 mV for the AMC1303x05x) or with a stream of only ones with an input greater than or equal to 320 mV (64 mV for the AMC1303x05x). In this case, however, the AMC1303 generates a single 1 (if the input is at negative full-scale) or 0 every 128 clock cycles to indicate proper device function (see the *Fail-Safe Output* section for more details). Figure 46 shows the input voltage versus the output modulator signal.

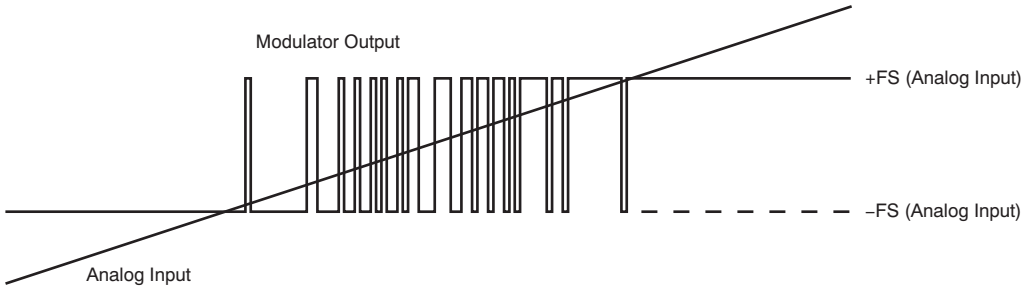


Figure 46. Analog Input versus AMC1303 Modulator Output

Equation 1 calculates the density of ones in the output bit-stream for any input voltage value (with the exception of a full-scale input signal, as described in the *Output Behavior in Case of a Full-Scale Input* section):

$$\frac{V_{IN} + V_{Clipping}}{2 \times V_{Clipping}} \quad (1)$$

The AMC1303 internally generates the clock signal required for the modulator. This clock is provided externally at the CLKOUT pin on AMC1303Mx devices only. For more details, see the *Switching Characteristics* section.

8.3.5 Manchester Coding Feature

The AMC1303Ex offers the IEEE 802.3-compliant Manchester coding feature that generates at least one transition per bit to support clock signal recovery from the bitstream. A Manchester coded bitstream is free of dc components. The Manchester coding combines the clock and data information using exclusive or (XOR) logical operation. Figure 47 shows the resulting bitstream.

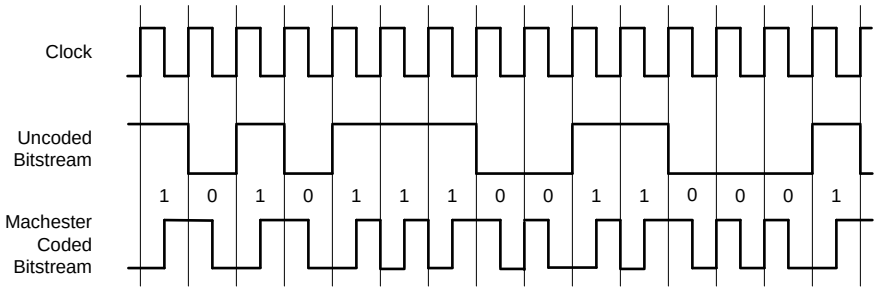


Figure 47. Manchester Coded Output of the AMC1303Ex

8.4 Device Functional Modes

8.4.1 Fail-Safe Output

In the case of a missing high-side supply voltage AVDD, the output of the ΔΣ modulator is not defined and can cause a system malfunction. In systems with high safety requirements, this behavior is not acceptable. Therefore, as shown in Figure 2, the AMC1303 implements a fail-safe output function that pulls the DOUT and CLKOUT outputs (AMC1303Mx only) to a steady-state logic 1 in case of a missing AVDD.

Similarly, as also shown in Figure 48, if the common-mode voltage of the input reaches or exceeds the specified common-mode overvoltage detection level V_{CMov} as defined in the *Electrical Characteristics* table, the AMC1303 generates a steady-state bitstream of logic 1's at the DOUT output.

In both cases, the steady-state logic 1 occurs on the DOUT output with a delay of two clock cycles after the event of either exceeded common-mode input voltage or missing AVDD. Another 256 clock cycles are required for the CLKOUT pin of the AMC1303Mx to be held at logic 1.

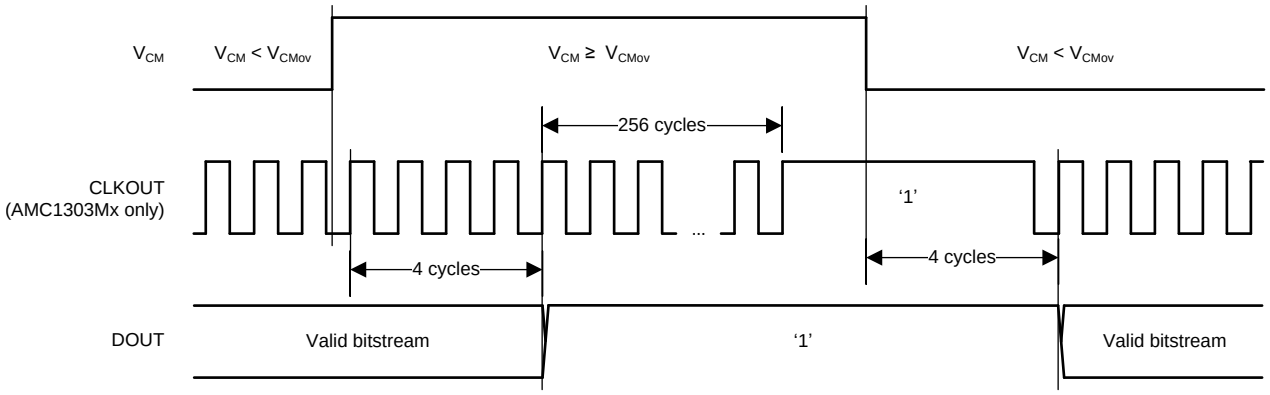


Figure 48. Fail-Safe Output of the AMC1303

8.4.2 Output Behavior in Case of a Full-Scale Input

If a full-scale input signal is applied to the AMC1303 (that is, $|V_{IN}| \geq |V_{Clipping}|$), Figure 49 shows that the device generates a single one or zero every 128 bits at DOUT, depending on the actual polarity of the signal being sensed. In this way, differentiating between a missing AVDD and a full-scale input signal is possible on the system level.

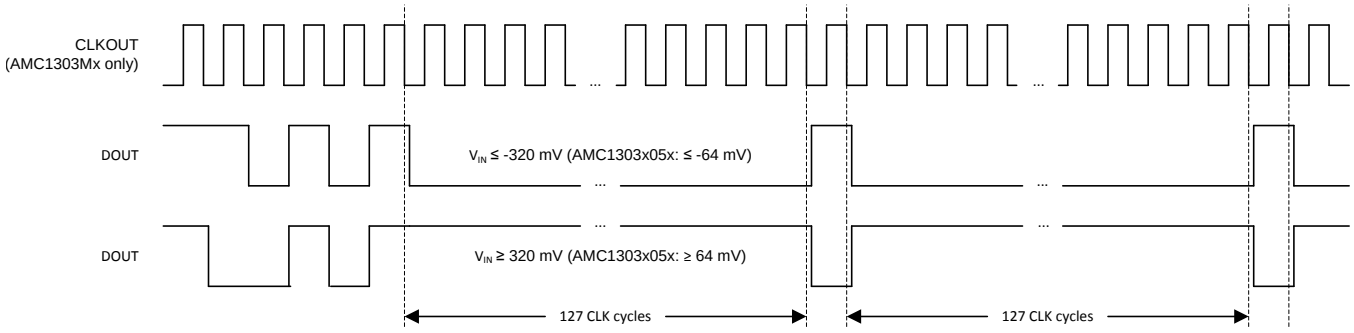


Figure 49. Overrange Output of the AMC1303

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Digital Filter Usage

The modulator generates a bit stream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). A very simple filter, shown in Equation 2, built with minimal effort and hardware, is a $sinc^3$-type filter:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \tag{2}$$

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All the characterization in this document is done with a $sinc^3$ filter with an oversampling ratio (OSR) of 256 and an output word size of 16 bits.

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. shows the ENOB of the AMC1303 with different oversampling ratios. In this document, Equation 3 calculates this number from the SNR:

$$ENOB = \frac{SNR - 1.76\,dB}{6.05\,dB} \tag{3}$$

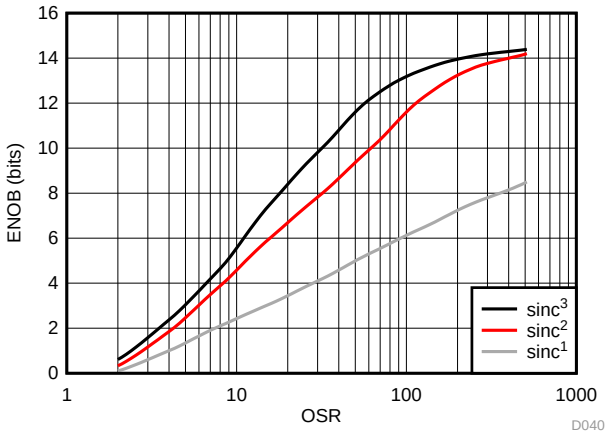


Figure 50. Measured Effective Number of Bits versus Oversampling Ratio

An example code for implementing a $sinc^3$ filter in an FPGA is discussed in application note *Combining ADS1202 with FPGA Digital Filter for Current Measurement in Motor Control Applications*, available for download at www.ti.com.

9.2 Typical Applications

9.2.1 Frequency Inverter Application

Isolated ΔΣ modulators are widely used in new-generation frequency inverter designs because of their high ac and dc performance. Frequency inverters are critical parts of industrial motor drives, photovoltaic inverters (string and central inverters), uninterruptible power supplies (UPS), and other industrial applications.

Figure 51 shows a simplified schematic of the AMC1303Mx in a typical frequency inverter application as used in industrial motor drives with shunt resistors (R_{SHUNT}) used for current sensing. Depending on the system design, either all three or only two motor phase currents are sensed.

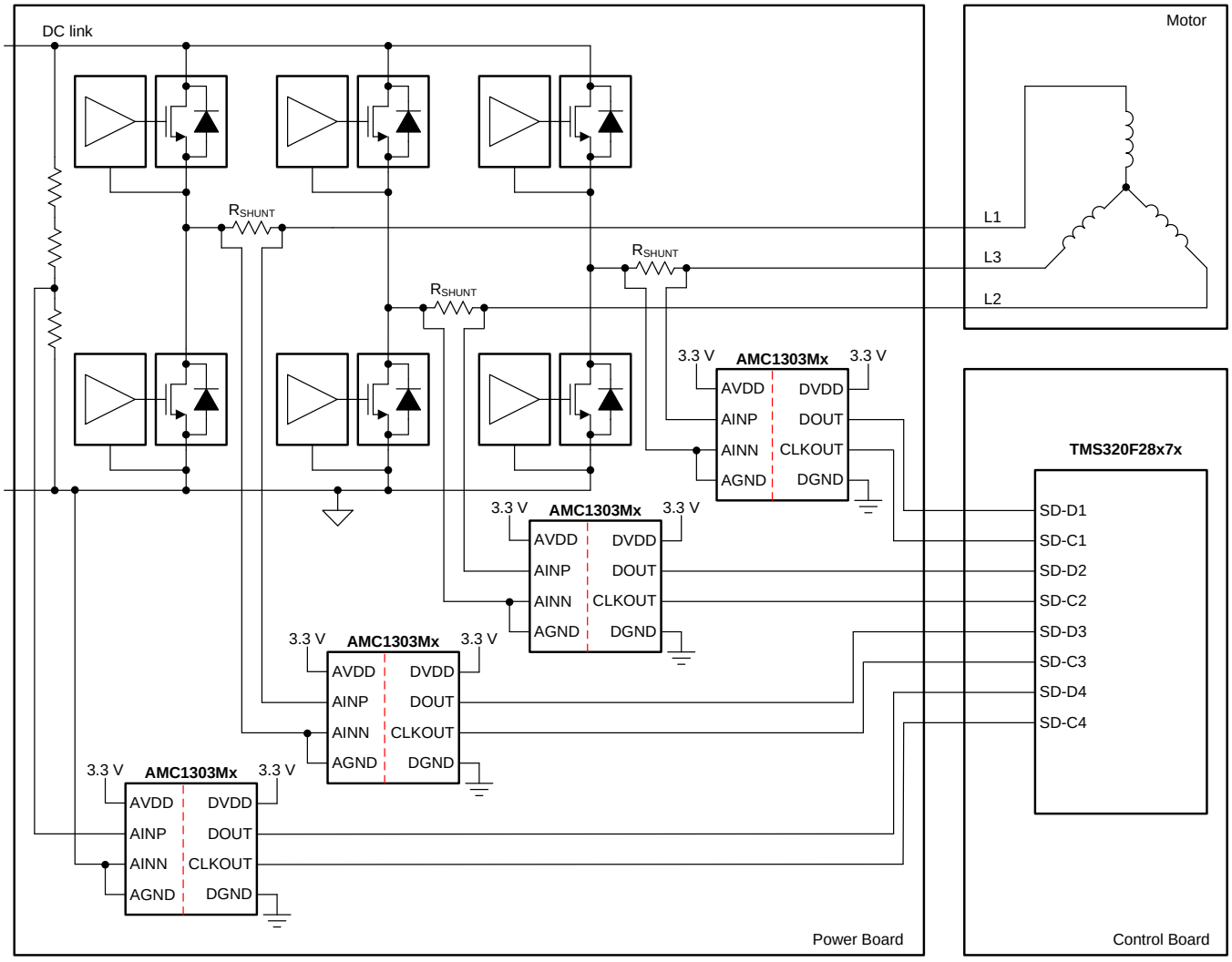


Figure 51. Simplified Diagram of the AMC1303Mx in a Frequency Inverter Application

Typical Applications (continued)

Figure 52 shows how the Manchester coded bitstream output of the AMC1303Ex minimizes the wiring efforts of the connection between the power and the control board. This bitstream output also allows the clock to be generated locally on the power board without the having to adjust the propagation delay time of each DOUT connection to fulfill the setup and hold time requirements of the microcontroller.

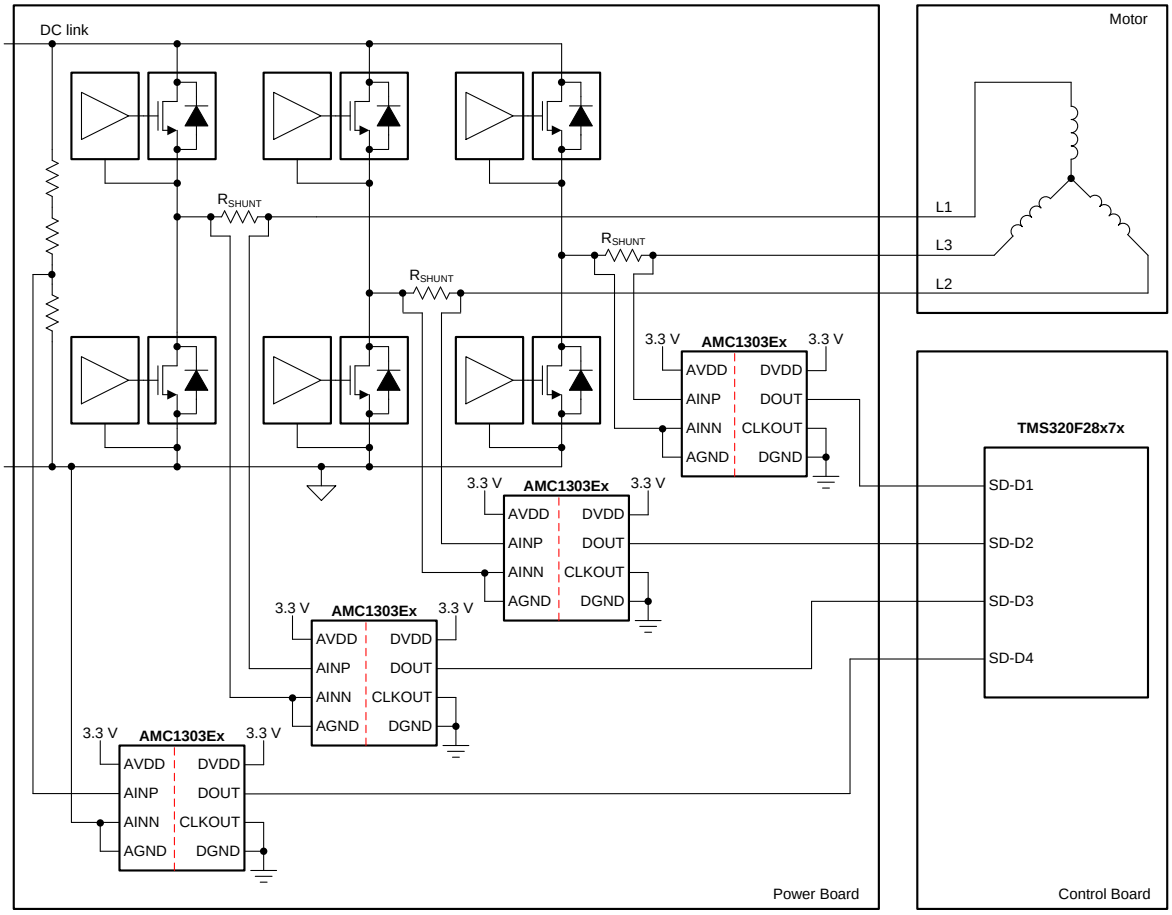


Figure 52. Simplified Diagram of the AMC1303Ex in a Frequency Inverter Application

In both examples shown previously, an additional fourth AMC1303 is used to support isolated voltage sensing of the dc link. This high voltage is reduced using a resistive divider and is sensed by the device across a smaller resistor. The value of this resistor can degrade the performance of the measurement, as described in the *Isolated Voltage Sensing* section.

9.2.1.1 Design Requirements

Table 1 lists the parameters for the typical application in the *Frequency Inverter Application* section.

Table 1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Voltage drop across the shunt for a linear response	AMC1303x25x: ±250 mV (maximum)
	AMC1303x05x: ±50 mV (maximum)

9.2.1.2 Detailed Design Procedure

The high-side power supply (AVDD) for the AMC1303 device is derived from the power supply of the upper gate driver. Further details are provided in the *Power Supply Recommendations* section.

The floating ground reference (AGND) is derived from one of the ends of the shunt resistor that is connected to the negative input of the AMC1303 (AINN). If a four-pin shunt is used, the inputs of the device are connected to the inner leads and AGND is connected to one of the outer shunt leads.

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times R_{SHUNT}$.

Consider the following two restrictions to choose the proper value of the shunt resistor R_{SHUNT}:

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range: $V_{SHUNT} \leq \pm 250$ mV
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $|V_{SHUNT}| \leq |V_{Clipping}|$

The typically recommended RC filter in front of a ΔΣ modulator to improve signal-to-noise performance of the signal path is not required for the AMC1303. By design, the input bandwidth of the analog front-end of the device is limited as specified in the *Electrical Characteristics* table.

For modulator output bitstream filtering, a device from TI's TMS320F2807x family of low-cost microcontrollers (MCUs) or TMS320F2837x family of dual-core MCUs is recommended. These families support up to eight channels of dedicated hardwired filter structures that significantly simplify system level design by offering two filtering paths per channel: one providing high accuracy results for the control loop and one fast response path for overcurrent detection.

9.2.1.3 Application Curves

In motor control applications, a very fast response time for overcurrent detection is required. The time for fully settling the filter in case of a step-signal at the input of the modulator depends on its order; that is, a $sinc^3$ filter requires three data updates for full settling (with $f_{DATA} = f_{CLK} / OSR$). Therefore, for overcurrent protection, filter types other than $sinc^3$ can be a better choice; an alternative is the $sinc^2$ filter. Figure 53 and Figure 54 compare the settling times of different filter orders.

The delay time of a sinc filter with a continuous signal is half of its settling time.

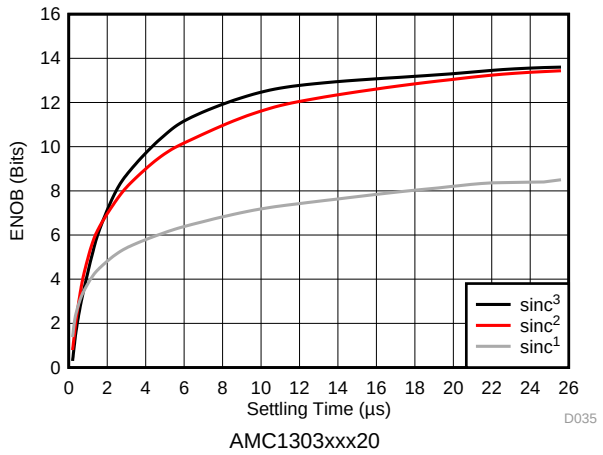


Figure 53. Measured Effective Number of Bits versus Settling Time

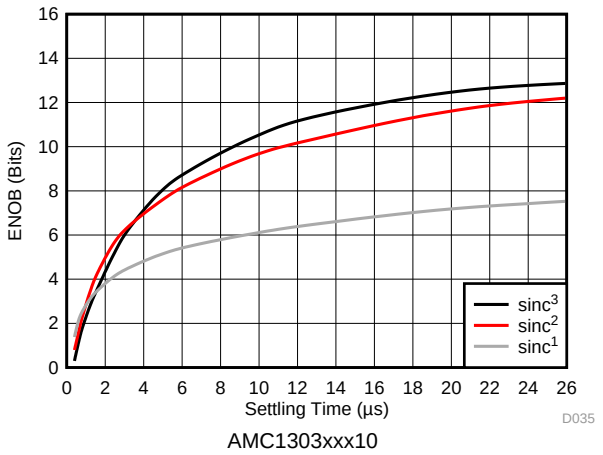


Figure 54. Measured Effective Number of Bits versus Settling Time

9.2.2 Isolated Voltage Sensing

The AMC1303 is optimized for usage in current-sensing applications using low-resistance shunts. However, the device can also be used in isolated voltage-sensing applications if the effect of the (usually higher) value of the resistor used in this case is considered. For best performance, TI recommends using the ±250-mV versions of the device (AMC1303x25xx) for this use case.

Figure 55 shows a simplified circuit typically used in high-voltage-sensing applications. The high value resistors (R1 and R2) are used as voltage dividers and dominate the current value definition. The resistance of the sensing resistor R3 is chosen to meet the input voltage range of the AMC1303. This resistor and the differential input resistance of the AMC1303x25x is 22 kΩ also create a voltage divider that results in an additional gain error. With the assumption of R1, R2, and R_{IND} having a considerably higher value than R3, the resulting total gain error can be estimated using Equation 4, with E_G being the gain error of the AMC1303.

$$\left|E_{Gtot}\right| = \left|E_G\right| + \frac{R3}{R_{IN}} \tag{4}$$

This gain error can be minimized during the initial system-level gain calibration procedure.

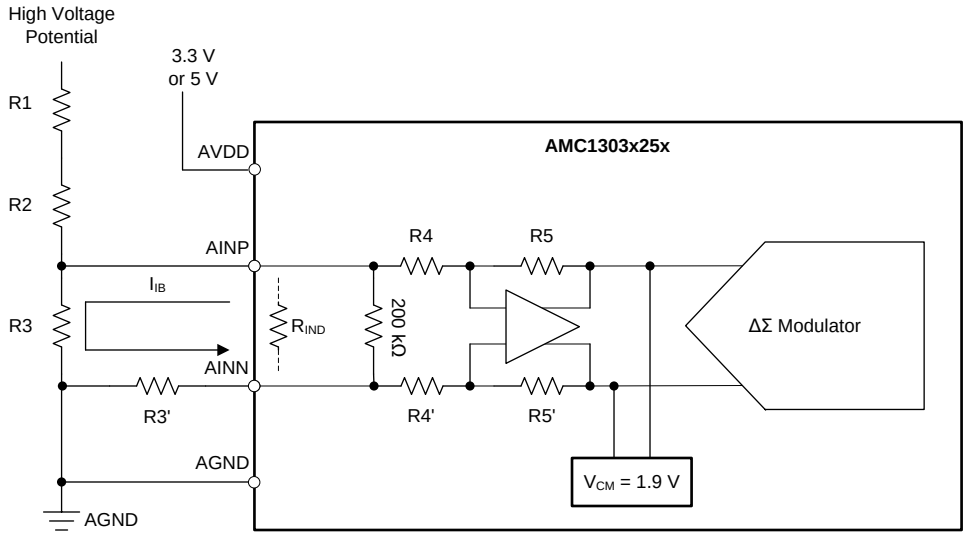


Figure 55. Using the AMC1303x25x for Isolated Voltage Sensing

9.2.2.1 Design Requirements

Table 2 lists the parameters for the typical application in the *Isolated Voltage Sensing* section.

Table 2. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Voltage drop across the resistor R3 for a linear response	AMC1303x25x: ±250 mV (maximum)

9.2.2.2 Detailed Design Procedure

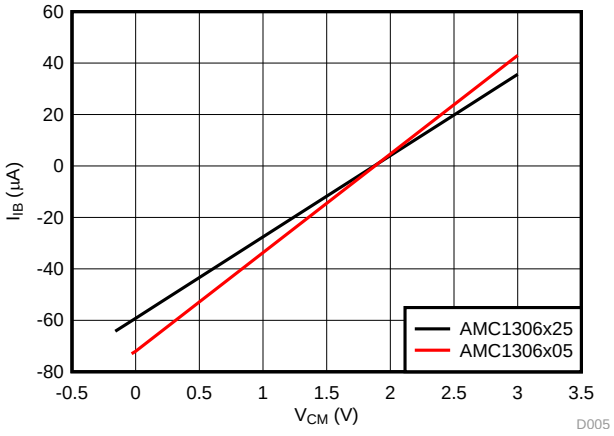
As indicated in Figure 55, the output of the integrated differential amplifier is internally biased to a common-mode voltage of 1.9 V. This voltage results in a bias current I_{IB} through the resistive network R4 and R5 (or R4' and R5') used for setting the gain of the amplifier. The value range of this current is specified in the *Electrical Characteristics* table. This bias current generates additional offset error that depends on the value of the resistor R3. Because the value of this bias current depends on the actual common-mode amplitude of the input signal (as illustrated in Figure 56), the initial system offset calibration does not minimize its effect. Therefore, in systems with high accuracy requirements, TI recommends using a series resistor at the negative input (AINN) of the AMC1303 with a value equal to the shunt resistor R3 (that is, R3' = R3 in Figure 55) to eliminate the effect of the bias current.

This additional series resistor (R3') influences the gain error of the circuit. The effect is calculated using Equation 5 with R5 = R5' = 50 kΩ and R4 = R4' = 12.5 kΩ for the AMC1303x25x.

$$E_G(\%) = \left(1 - \frac{R4}{R4' + R3'}\right) \times 100\% \tag{5}$$

9.2.2.3 Application Curve

Figure 56 shows the dependency of the input bias current on the common-mode voltage at the input of the AMC1303x25x.



AMC1303x25x

Figure 56. Input Current vs Input Common-Mode Voltage

9.2.3 Do's and Don'ts

Do not leave the inputs of the AMC1303 unconnected (floating) when the device is powered up. If both modulator inputs are left floating, the input bias current drives these inputs to the output common-mode voltage of the differential amplifier of approximately 1.9 V. If that voltage is above the specified input common-mode range, the gain of the differential amplifier diminishes and the modulator outputs a bitstream resembling a zero differential input voltage.

10 Power Supply Recommendations

In a typical frequency-inverter application, the high-side power supply (AVDD) for the device is directly derived from the floating power supply of the upper gate driver. For lowest system-level cost, a Zener diode can be used to limit the voltage to 5 V or 3.3 V (±10%). Alternatively a low-cost low-drop regulator (LDO), for example the LM317-N, can be used to adjust the supply voltage level and minimize noise on the power supply node. A low-ESR decoupling capacitor of 0.1 µF is recommended for filtering this power-supply path. Place this capacitor (C2 in Figure 57) as close as possible to the AVDD pin of the AMC1303 for best performance. Further, an additional capacitor with a value in the range of 2.2 µF to 10 µF is recommended.

The floating ground reference (AGND) is derived from the end of the shunt resistor, which is connected to the negative input (AINN) of the device. If a four-pin shunt is used, the device inputs are connected to the inner leads and AGND is connected to one of the outer leads of the shunt.

For decoupling of the digital power supply on the controller side, TI recommends using a 0.1-µF capacitor assembled as close to the DVDD pin of the AMC1303 as possible, followed by an additional capacitor in the range of 2.2 µF to 10 µF.

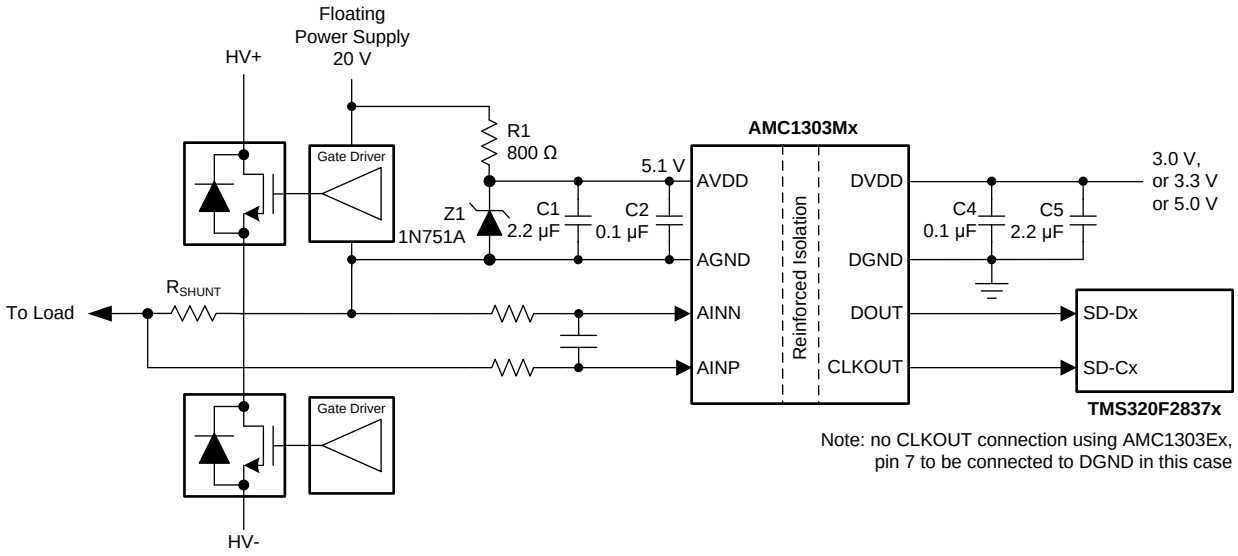


Figure 57. Decoupling the AMC1303

11 Layout

11.1 Layout Guidelines

Figure 58 shows a layout recommendation detailing the critical placement of the decoupling capacitors (as close as possible to the AMC1303) and placement of the other components required by the device. For best performance, place the shunt resistor and the antialiasing filter components as close as possible to the AINP and AINN inputs of the AMC1303 and keep the layout of both connections symmetrical.

11.2 Layout Example

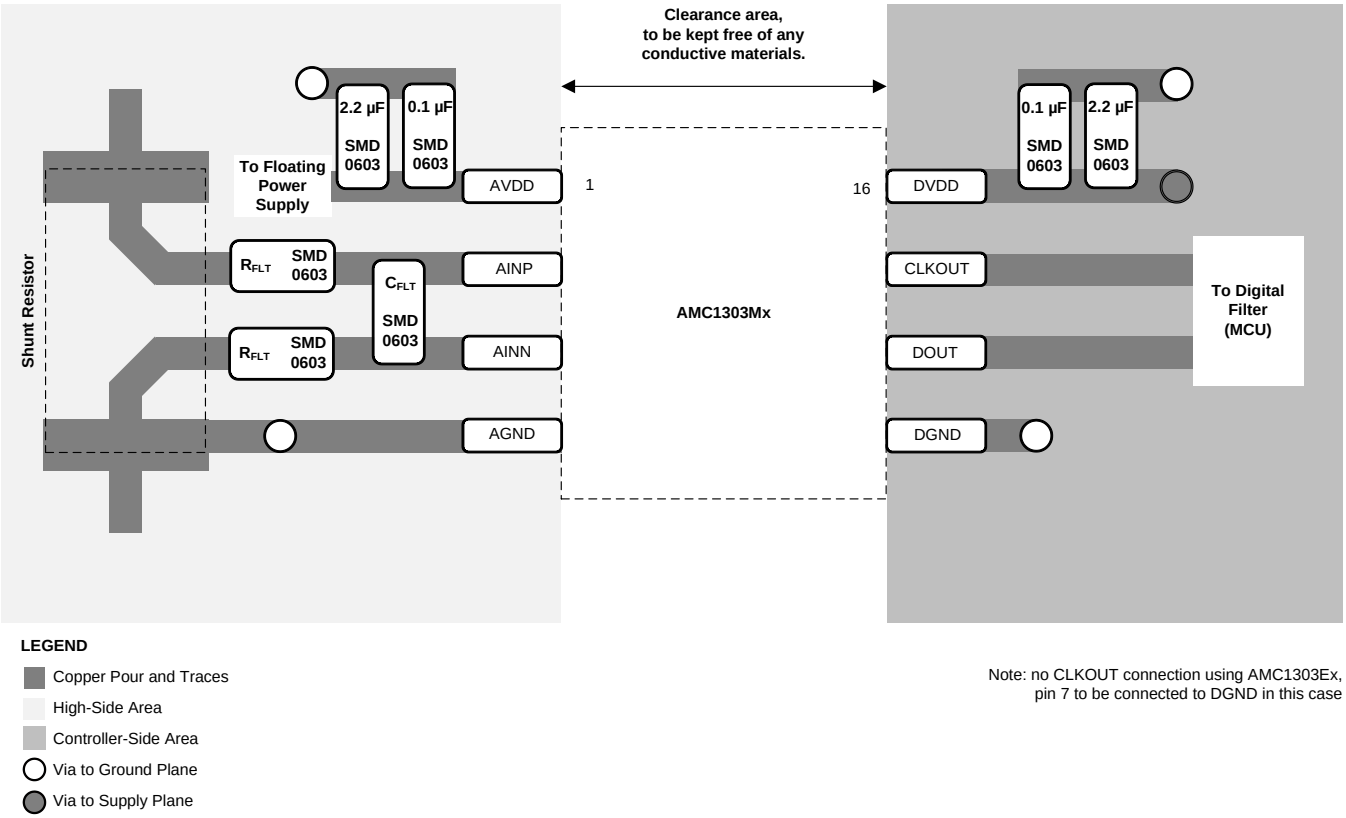


Figure 58. Recommended Layout of the AMC1303

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

12.1.1.1 Isolation Glossary

See the *Isolation Glossary*

12.2 Documentation Support

12.2.1 Related Documentation

- *AMC1210 Quad Digital Filter for 2nd-Order Delta-Sigma Modulator*
- *MSP430F677x Polyphase Metering SoCs*
- *TMS320F2807x Piccolo™ Microcontrollers*
- *TMS320F2837xD Dual-Core Delfino™ Microcontrollers*
- *ISO72x Digital Isolator Magnetic-Field Immunity*
- *Combining ADS1202 with FPGA Digital Filter for Current Measurement in Motor Control Applications*

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 3. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
AMC1303E0510	Click here	Click here	Click here	Click here	Click here
AMC1303M0510	Click here	Click here	Click here	Click here	Click here
AMC1303E0520	Click here	Click here	Click here	Click here	Click here
AMC1303M0520	Click here	Click here	Click here	Click here	Click here
AMC1303E2510	Click here	Click here	Click here	Click here	Click here
AMC1303M2510	Click here	Click here	Click here	Click here	Click here
AMC1303E2520	Click here	Click here	Click here	Click here	Click here
AMC1303M2520	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1303E0510DWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1303E051	Samples
AMC1303E0510DWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1303E051	Samples
AMC1303E0520DWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1303E052	Samples
AMC1303E0520DWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1303E052	Samples
AMC1303E2510DWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1303E251	Samples
AMC1303E2510DWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1303E251	Samples
AMC1303E2520DWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1303E252	Samples
AMC1303E2520DWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1303E252	Samples
AMC1303M0510DWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1303M051	Samples
AMC1303M0510DWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1303M051	Samples
AMC1303M0520DWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1303M052	Samples
AMC1303M0520DWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1303M052	Samples
AMC1303M2510DWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1303M251	Samples
AMC1303M2510DWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1303M251	Samples
AMC1303M2520DWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1303M252	Samples
AMC1303M2520DWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1303M252	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

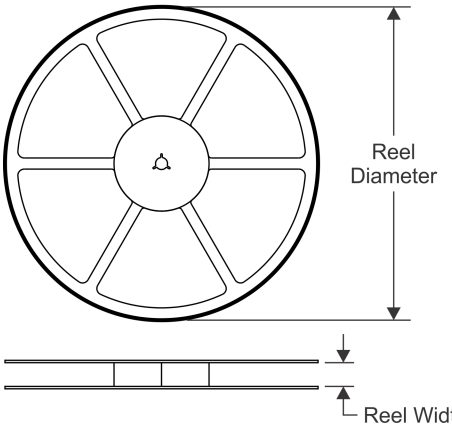
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

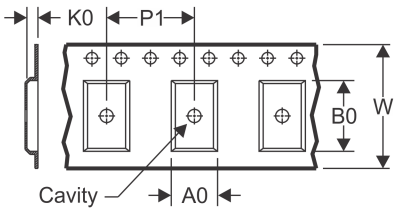
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

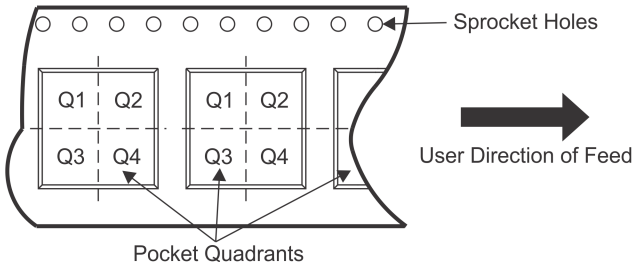


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

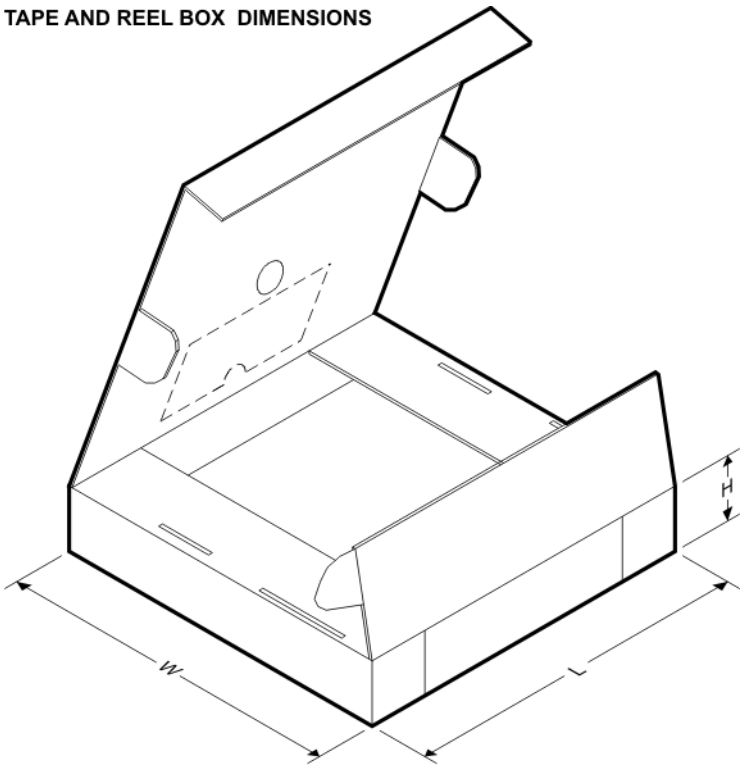
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

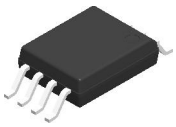
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1303E0510DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1303E0520DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1303E2510DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1303E2520DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1303M0510DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1303M0520DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1303M2510DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1303M2520DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

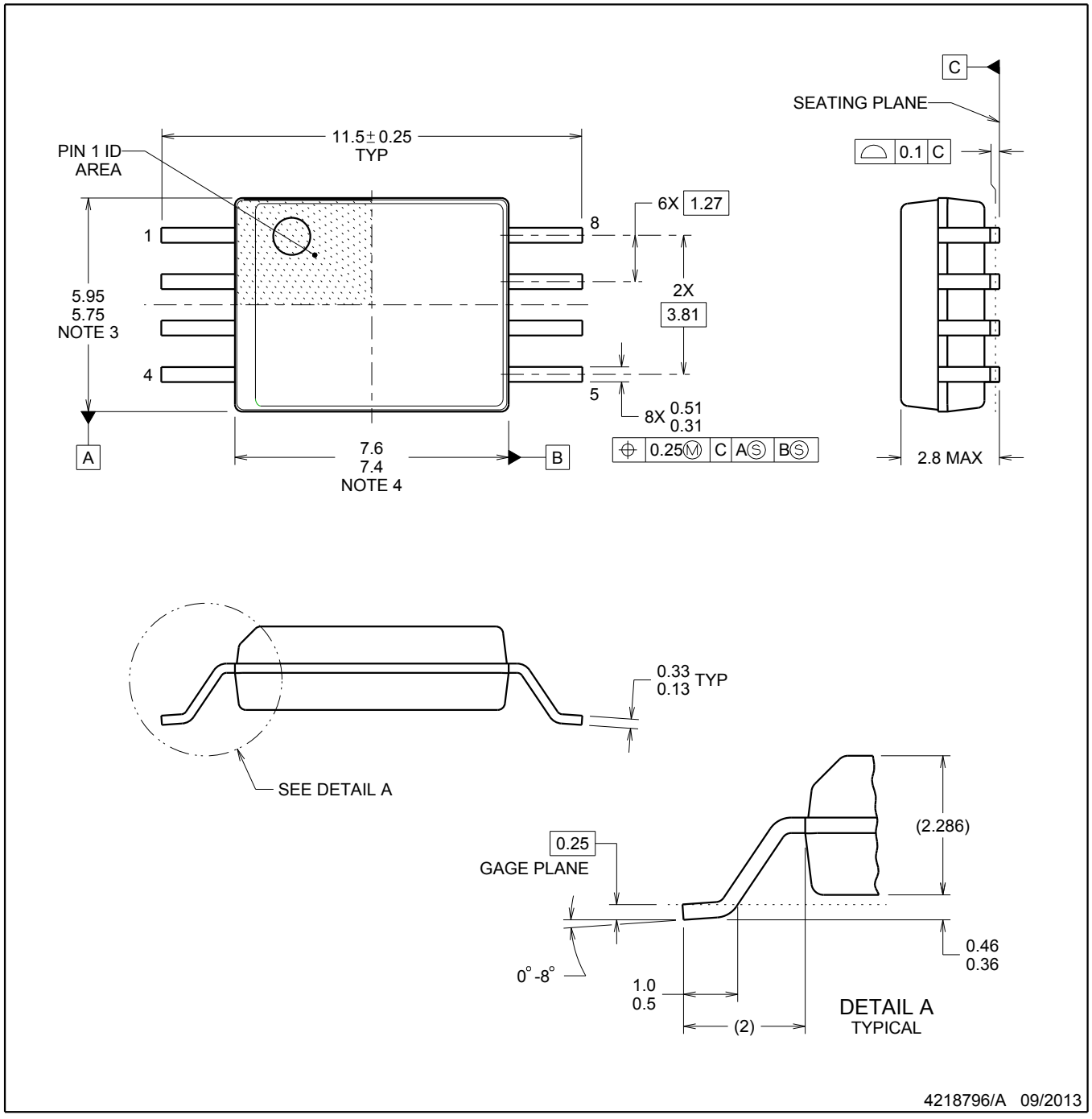
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1303E0510DWVR	SOIC	DWV	8	1000	367.0	367.0	38.0
AMC1303E0520DWVR	SOIC	DWV	8	1000	367.0	367.0	38.0
AMC1303E2510DWVR	SOIC	DWV	8	1000	367.0	367.0	38.0
AMC1303E2520DWVR	SOIC	DWV	8	1000	367.0	367.0	38.0
AMC1303M0510DWVR	SOIC	DWV	8	1000	367.0	367.0	38.0
AMC1303M0520DWVR	SOIC	DWV	8	1000	367.0	367.0	38.0
AMC1303M2510DWVR	SOIC	DWV	8	1000	367.0	367.0	38.0
AMC1303M2520DWVR	SOIC	DWV	8	1000	367.0	367.0	38.0



DWV0008A

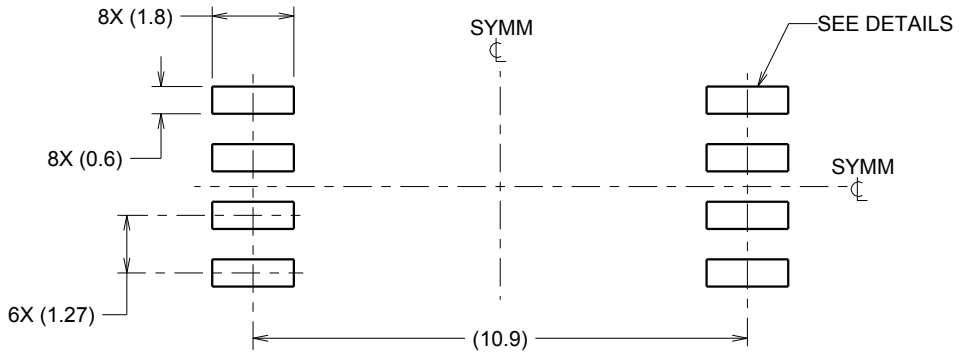
SOIC - 2.8 mm max height

SOIC

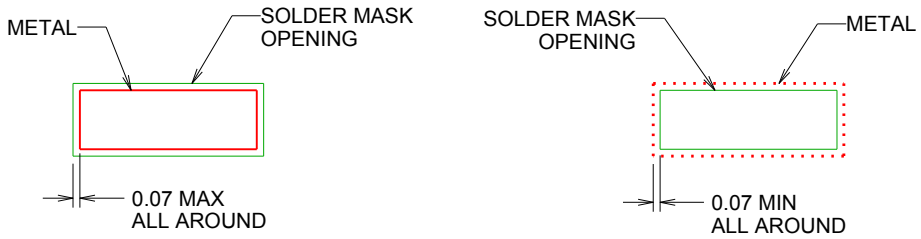


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

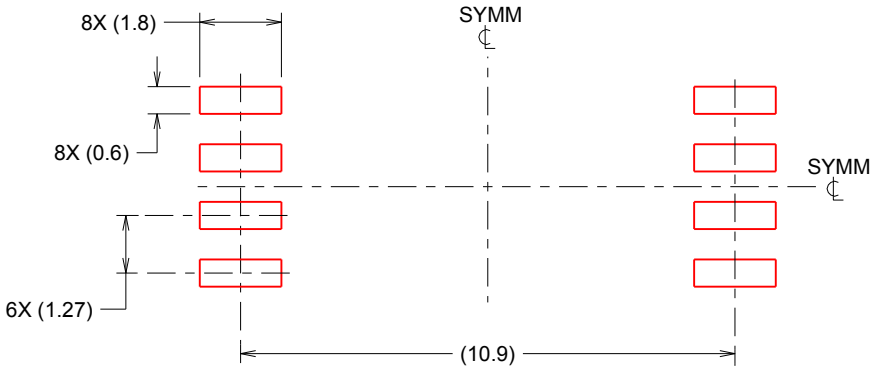
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265