TEXAS INSTRUMENTS

HD3SS3415

SLAS840C –MARCH 2012–REVISED OCTOBER 2015

HD3SS3415 4-Channel High-Performance Differential Switch

1 Features

- Compatible with Multiple Interface Standards Operating up to 12 Gbps Including PCI Express Gen III and USB 3.0
- Wide –3-dB Differential BW of over 8 GHz
- Excellent Dynamic Characteristics (at 4 GHz)
  - Crosstalk = –35 dB
  - Off Isolation = –19 dB
  - Insertion Loss = –1.5 dB
  - Return Loss = –11 dB
- VDD Operating Range 3.3 V ±10%
- Small 3.5 mm × 9 mm, 42-Pin WQFN Package
- Common Industry Standard Pinout

2 Applications

- Desktop and Notebook PCs
- Server/Storage Area Networks
- PCI Express Backplanes
- Shared I/O Ports

3 Description

The HD3SS3415 is a high-speed passive switch capable of switching four differential channels, including applications such as two full PCI Express x1 lanes from one source to one of two target locations in a PC/server application. With its bidirectional capability the HD3SS3415 will also support applications that allow connections between one target and two source devices, such as a shared peripheral between two platforms. The HD3SS3415 has a single control line (SEL Pin) which can be used to control the signal path between Port A and either Port B or Port C.
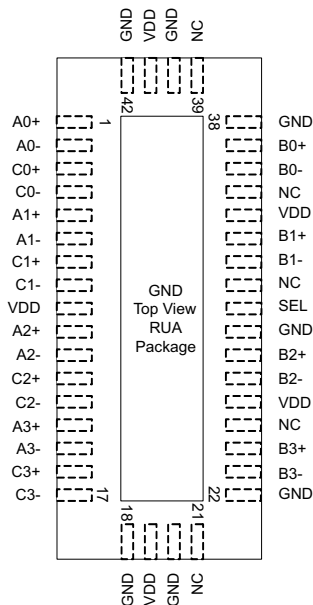
The HD3SS3415 is offered in an industry standard 42-pin WQFN package available in a common footprint shared by several other vendors. The device is specified to operate from a single supply voltage of 3.3 V over the full temperature range of 0°C to 70°C

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
HD3SS3415	WQFN (42)	9.00 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

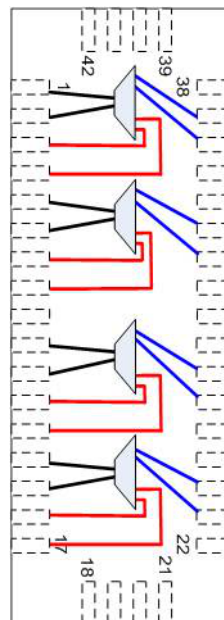**HD3SS3415 Pinout**

HD3SS3415 Switch Flow Through Routing

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2015) to Revision C **Page**

- Changed the *HD3SS3415 Pinout* and *HD3SS3415 Switch Flow Through Routing* images 1
- Changed temperature From: industrial temperature range of –40°C to 85°C To: industrial temperature range of 0°C to 70°C in the *Overview* section 12

Changes from Revision A (July 2015) to Revision B **Page**

- Changed the Storage temperature MIN value From: 65 To: –65 in the *Absolute Maximum Ratings*[(1)(2)] table 6

Changes from Original (February 2012) to Revision A **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Deleted the word "industrial" from *Description* section 1
- Changed the second paragraph of the *Description* -40 to 0 and 85 to 70°C 1
- Changed T_A spec values from –40°C MIN and 85°C MAX to 0°C MIN and 70°C MAX in the *Recommended Operating Conditions* table. 6

5 Description continued

The HD3SS3415 is a generic 4-CH high-speed mux/demux type of switch that can be used for routing high-speed signals between two different locations on a circuit board. Although it was designed specifically to address PCI Express Gen III applications, the HD3SS3415 will also support several other high-speed data protocols with a differential amplitude of < 1800 mVpp and a common mode voltage of < 2 V, as with USB 3.0 and DisplayPort 1.2. The one select input (SEL) pin of the device can easily be controlled by an available GPIO pin within a system or from a microcontroller.

6 Pin Configuration and Functions

RUA Package
42-Pin WQFN
Top View
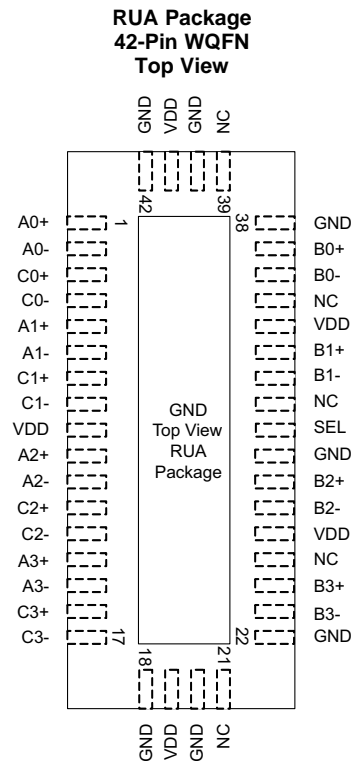
Pin Functions

PIN		I/O	DESCRIPTION
NAME	**NO.**		
SWITCH PORT A			
A0+	1		Port A, Channel 0, High Speed Positive Signal
A0–	2		Port A, Channel 0, High Speed Negative Signal
A1+	5		Port A, Channel 1, High Speed Positive Signal
A1–	6		Port A, Channel 1, High Speed Negative Signal
A2+	10	I/O	Port A, Channel 2, High Speed Positive Signal
A2–	11		Port A, Channel 2, High Speed Negative Signal
A3+	14		Port A, Channel 3, High Speed Positive Signal
A3–	15		Port A, Channel 3, High Speed Negative Signal
SWITCH PORT B			
B0+	37		Port B, Channel 0, High Speed Positive Signal
B0–	36		IPort B, Channel 0, High Speed Negative Signal
B1+	33		Port B, Channel 1, High Speed Positive Signal
B1–	32		Port B, Channel 1, High Speed Negative Signal
B2+	28	I/O	Port B, Channel 2, High Speed Positive Signal
B2–	27		Port B, Channel 2, High Speed Negative Signal
B3+	24		Port B, Channel 3, High Speed Positive Signal
B3–	23		Port B, Channel 3, High Speed Negative Signal

Product Folder Links: *HD3SS3415*

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SWITCH PORT C			
C0+	3	I/O	Port C, Channel 0, High Speed Positive Signal
C0–	4		Port C, Channel 0, High Speed Negative Signal
C1+	7		Port C, Channel 1, High Speed Positive Signal
C1–	8		Port C, Channel 1, High Speed Negative Signal
C2+	12		Port C, Channel 2, High Speed Positive Signal
C2–	13		Port C, Channel 2, High Speed Negative Signal
C3+	16		Port C, Channel 3, High Speed Positive Signal
C3–	17		Port C, Channel 3, High Speed Negative Signal
CONTROL, SUPPLY, AND NO CONNECT			
GND	18, 20, 22, 29, 38, 40, 42, Center Pad	Supply	Negative power supply voltage
NC	21, 25, 31, 35, 39	–	Electrically not connected
SEL	30	I	Select between port B or port C. Internally tied to GND via 100kΩ resistor
VDD	9, 19, 26, 34, 41	Supply	Positive power supply voltage

7 Specifications

7.1 Absolute Maximum Ratings[1][2]

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage (V_{DD})	Absolute minimum/maximum supply voltage range	−0.5	4	V
Voltage	Differential I/O	−0.5	4	V
	Control pin (SEL)	−0.5	VDD+0.5	
Storage temperature (T_{stg})		−65	150	ºC

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Typical values for all parameters are at V_{DD} = 3.3V and T_A = 25°C. (Temperature limits are specified by design)

			MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage		3.0	3.3	3.6	V
V_{IH}	Input high voltage (SEL Pin)		2.0		VDD	V
V_{IL}	Input low voltage (SEL Pin)		−0.1		0.8	V
V_{I/O_Diff}	Differential voltage (differential pins)	Switch I/O diff voltage	0		1.8	VPP
V_{I/O_CM}	Common voltage (differential pins)	Switch I/O common mode voltage	0		2.0	V
T_A	Operating free-air temperature	Ambient temperature	0		70	°C

7.4 Thermal Information

THERMAL METRIC[1]		HD3SS3415	UNIT
		TQFN (RUA)	
		42 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	27.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

R_{SC} and R_{LOAD} = 50 Ω and C_L = 50 pF, over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE PARAMETERS						
I_{IH}	Input High Voltage (SEL)	V_{DD} = 3.6 V; V_{IN} = VDD			95	µA
I_{IL}	Input Low Voltage (SEL)	V_{DD} = 3.6 V; V_{IN} = GND			1	µA
I_{LK}	Leakage Current (Differential I/O pins)	V_{DD} = 3.6 V; V_{IN} = 0 V; V_{OUT} = 2 V (I_{LK} On OPEN outputs) [Ports B and C]			130	µA
		V_{DD} = 3.6 V, V_{IN} = 2 V; V_{OUT} = 0 V (I_{LK} On OPEN outputs) [Port A]			4	
I_{DD}	Supply Current	V_{DD} = 3.6 V; SEL = V_{DD}/GND; Outputs Floating		4.7	6	mA
C_{ON}	Outputs ON Capacitance	V_{IN} = 0 V; Outputs Open; Switch ON		1.5		pF
C_{OFF}	Outputs OFF Capacitance	V_{IN} = 0 V; Outputs Open, Switch OFF		1		pF
R_{ON}	Output ON resistance	V_{DD} = 3.3 V; V_{CM} = 0.5 V to 1.5 V ; I_O = −8 mA		5	8	Ω
ΔR_{ON}	On resistance match between channels	V_{DD} = 3.3 V ; −0.35 V ≤ V_{IN} ≤ 1.2 V; I_O = −8 mA			2	Ω
	On resistance match between pairs of the same channel	V_{DD} = 3.3 V; −0.35 V ≤ V_{IN} ≤ 1.2 V; I_O = −8 mA			0.7	Ω
R_{FLAT_ON}	On resistance flatness ($R_{ON(MAX)}$ − $R_{ON(MAIN)}$)	V_{DD} = 3.3 V; −0.35 V ≤ V_{IN} ≤ 1.2 V			1.15	Ω
t_{PD}	Switch propagation delay	Rsc and R_{LOAD} = 50 Ω			85	ps
	SEL-to-switch Ton	Rsc and R_{LOAD} = 50 Ω		70	250	ns
	SEL-to-switch Toff			70	250	
T_{SKEW_Inter}	Inter-pair output skew (CH-CH)	Rsc and R_{LOAD} = 50 Ω			20	ps
T_{SKEW_Intra}	Intra-pair output skew (bit-bit)				8	ps
R_L	Differential return loss (VCM = 0 V) See *Typical Characteristics*	f = 0.3 MHz		−28		dB
		f = 2500 MHz		−12		
		f = 4000 MHz		−11		
X_{TALK}	Differential Crosstalk(VCM = 0 V) See *Typical Characteristics*	f = 0.3 MHz		−90		dB
		f = 2500 MHz		−39		
		f = 4000 MHz		−35		
O_{IRR}	Differential Off-Isolation(VCM = 0 V) See *Typical Characteristics*	f = 0.3 MHz		−75		dB
		f = 2500 MHz		−22		
		f = 4000 MHz		−19		
I_L	Differential Insertion Loss (VCM = 0 V) See *Typical Characteristics*	f = 0.3 MHz		−0.5		dB
		f = 2500 MHz		−1.1		
		f = 4000 MHz		−1.5		
BW	Band Width	At −3 dB		8		GHz

7.6 Dissipation Ratings

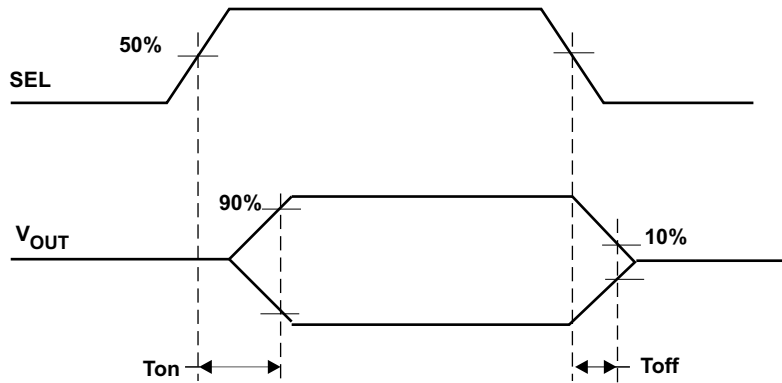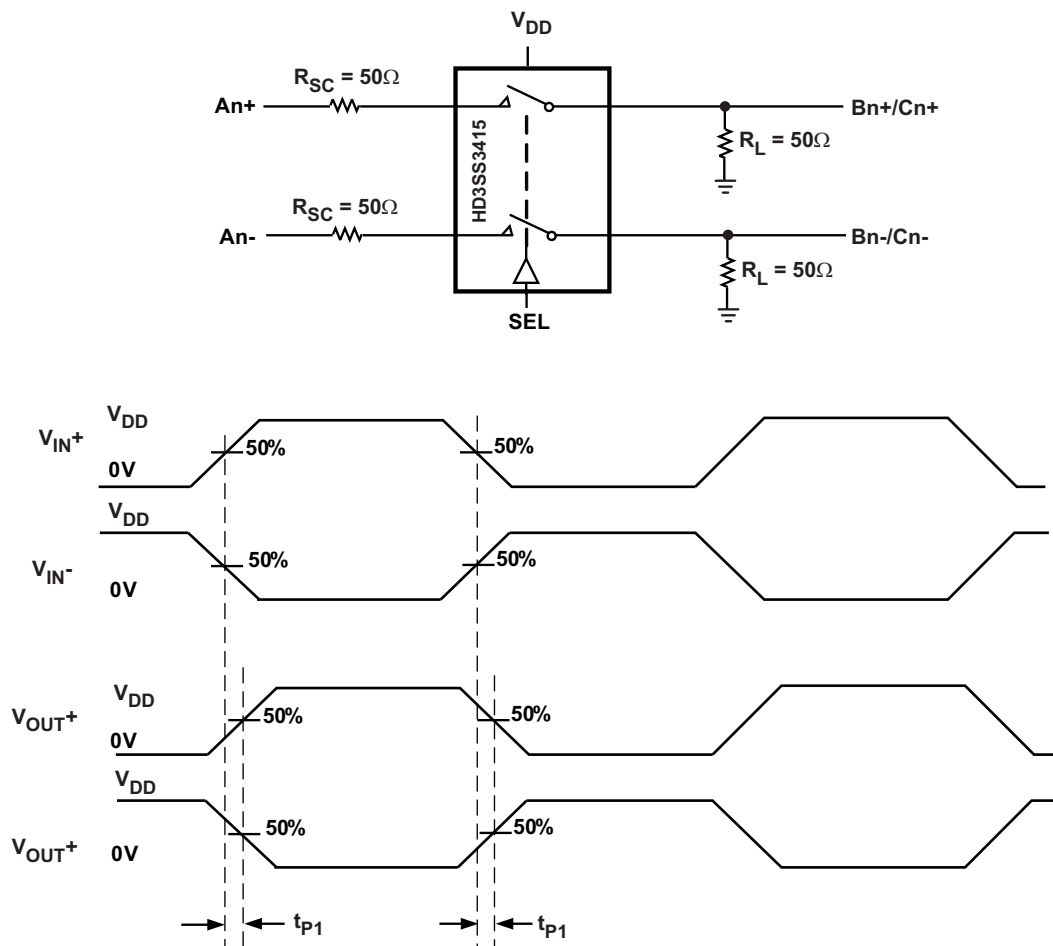|		MIN	MAX	UNIT
P_D	Power Dissipation	15.5	21.6	mW

Figure 1. Select to Switch Output On (T$_{ON}$) and Off (T$_{OFF}$) Timing Diagram

T$_{SKEWInter}$ = Difference between t$_{PD}$ for any two pairs of outputs

T$_{SKEWIntra}$ = Difference between t$_{P1}$ and t$_{P2}$ of same pair

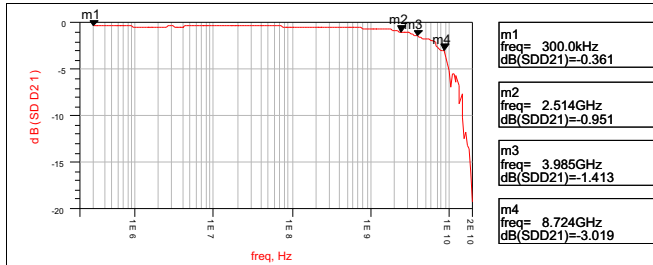**Figure 2. Propagation Delay Timing Diagram and Test Setup**

7.7 Typical Characteristics

m1	
freq=	300.0kHz
dB(SDD21)=	-0.361

m2	
freq=	2.514GHz
dB(SDD21)=	-0.951

m3	
freq=	3.985GHz
dB(SDD21)=	-1.413

m4	
freq=	8.724GHz
dB(SDD21)=	-3.019

Figure 3. Differential Insertion Loss

m5	
freq=	300.0kHz
dB(SDD11)=	-28.295

m6	
freq=	2.514GHz
dB(SDD11)=	-13.591

m7	
freq=	3.985GHz
dB(SDD11)=	-10.275
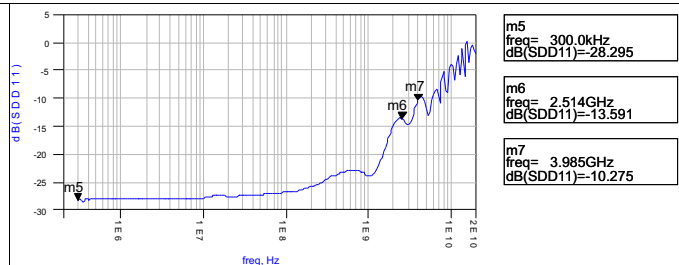
Figure 4. Differential Return Loss

m1	
freq=	300.0kHz
dB(SDD21)=	-86.588

m2	
freq=	2.514GHz
dB(SDD21)=	-33.793

m3	
freq=	3.985GHz
dB(SDD21)=	-29.900
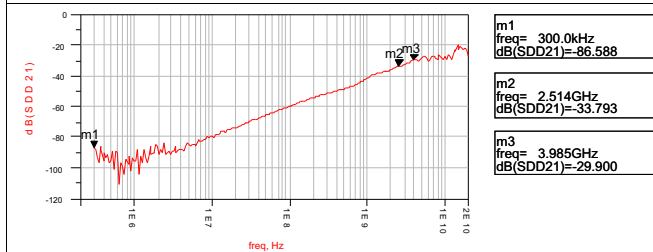
Figure 5. Differential Crosstalk

m1	
freq=	300.0kHz
dB(SDD21)=	-78.265

m2	
freq=	2.514GHz
dB(SDD21)=	-22.547

m3	
freq=	3.985GHz
dB(SDD21)=	-19.244
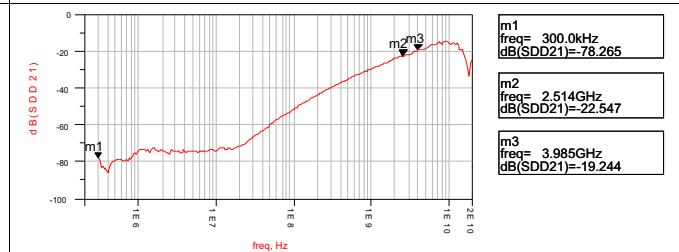
Figure 6. Differential Off Isolation

Product Folder Links: *HD3SS3415*
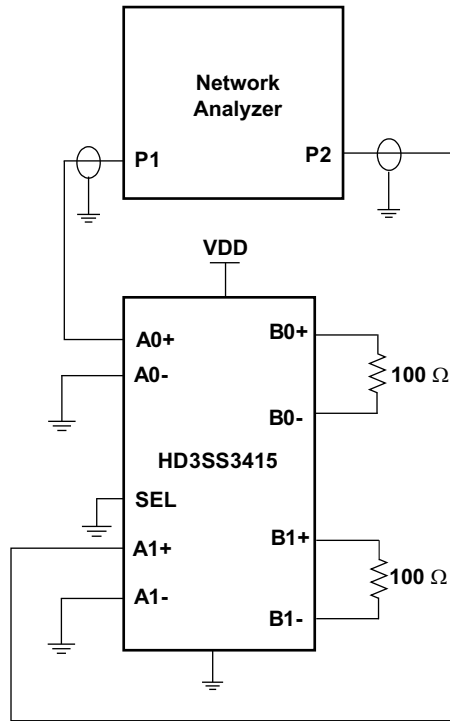
8 Parameter Measurement Information
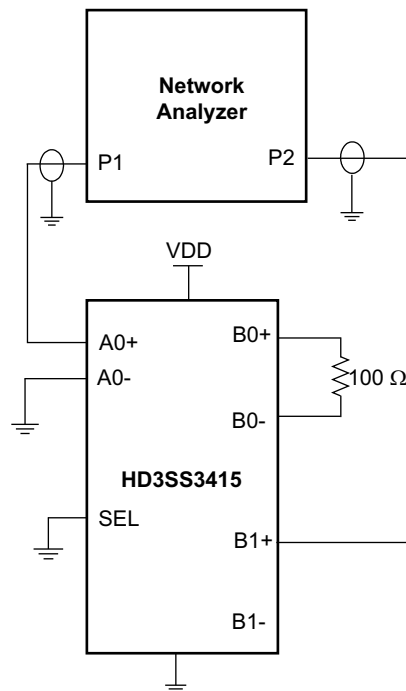

Figure 7. Cross Talk Measurement Setup

Figure 8. Off Isolation Measurement Setup
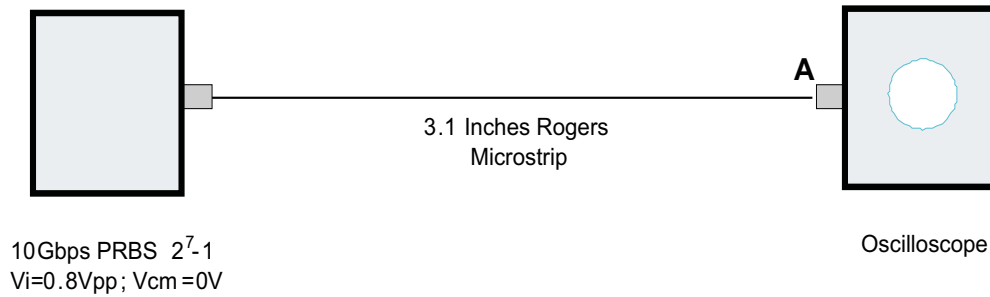
Parameter Measurement Information (continued)

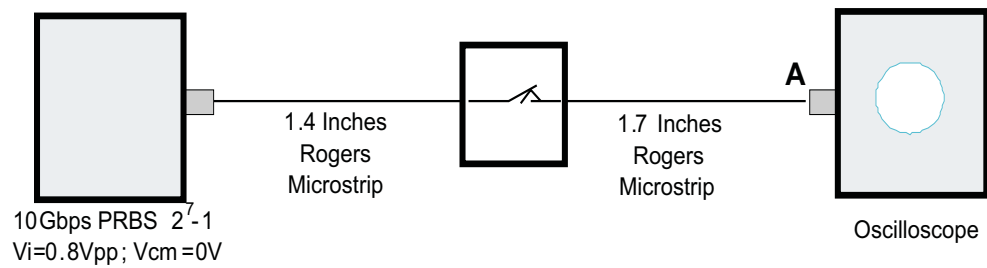
Figure 9. Source Eye Diagram Test Setup

**Figure 10. Output Eye Diagram Test Setup**

Product Folder Links: *HD3SS3415*

9 Detailed Description

9.1 Overview

The HD3SS3415 is a high-speed passive switch offered in an industry standard 42-pin WQFN package available in a common footprint shared by several other vendors. The device is specified to operate from a single supply voltage of 3.3 V over the full industrial temperature range of 0°C to 70°C. The HD3SS3415 is a generic 4-CH high-speed mux/demux type of switch that can be used for routing high-speed signals between two different locations on a circuit board. Although it was designed specifically to address PCI Express Gen III applications, the HD3SS3415 will also support several other high-speed data protocols with a differential amplitude of < 1800 mVpp and a common-mode voltage of < 2.0 V, as with USB 3.0 and DisplayPort 1.2.

9.2 Functional Block Diagram
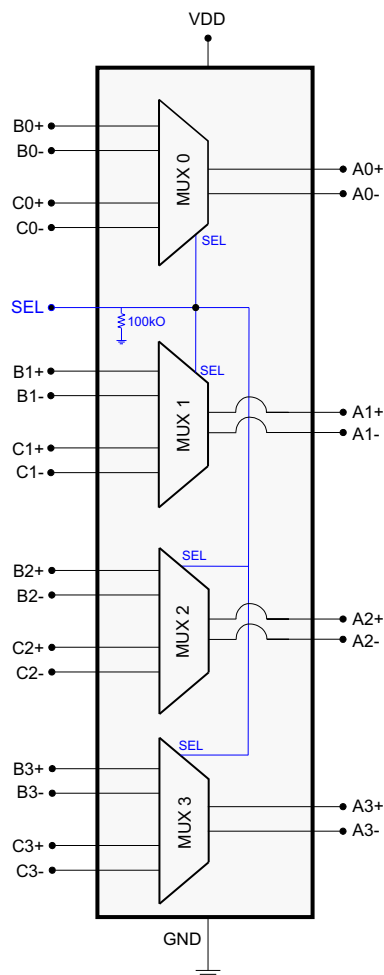
9.3 Feature Description

The HD3SS3415 has a single control line (SEL Pin) which can be used to control the signal path between Port A and either Port B or Port C. Theone select input (SEL) pin of the device can easily be controlled by an available GPIO pin within a system or from a microcontroller.

Table 1. MUX Pin Connections[1]

PORT A CHANNEL	PORT B OR PORT C CHANNEL CONNECTED TO PORT A CHANNEL	
	SEL = L	SEL = H
A0+	B0+	C0+
A0–	B0–	C0–
A1+	B1+	C1+
A1–	B1–	C1–
A2+	B2+	C2+
A2–	B2–	C2–
A3+	B3+	C3+
A3–	B3–	C3–

(1) The HD3SS3415 can tolerate polarity inversions for all differential signals on Ports A, B and C. Care should be taken to ensure the same polarity is maintained on Port A vs. Port B/C.

9.4 Device Functional Modes

Table 2 lists the functional modes for the HD3SS3415.

Table 2. HD3SS3415 Control Logic

CONTROL PIN (SEL)	PORT A TO PORT B CONNECTION STATUS	PORT A TO PORT C CONNECTION STATUS
L (Default State)	Connected	Disconnected
H	Disconnected	Connected

10 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 AC Coupling Caps

Many interfaces require AC coupling between the transmitter and receiver. The 0402 capacitors are the preferred option to provide AC coupling, and the 0603 size capacitors also work. The 0805 size capacitors and C-packs should be avoided. When placing AC coupling capacitors symmetric placement is best. A capacitor value of 0.1 µF is best and the value should be match for the ± signal pair. The placement should be along the TX pairs on the system board, which are usually routed on the top layer of the board.

There are several placement options for the AC coupling capacitors. Because the switch requires a bias voltage, the capacitors must only be placed on one side of the switch. If they are placed on both sides of the switch, a biasing voltage should be provided. A few placement options are shown below. In Figure 11, the coupling capacitors are placed between the switch and endpoint. In this situation, the switch is biased by the system/host controller.

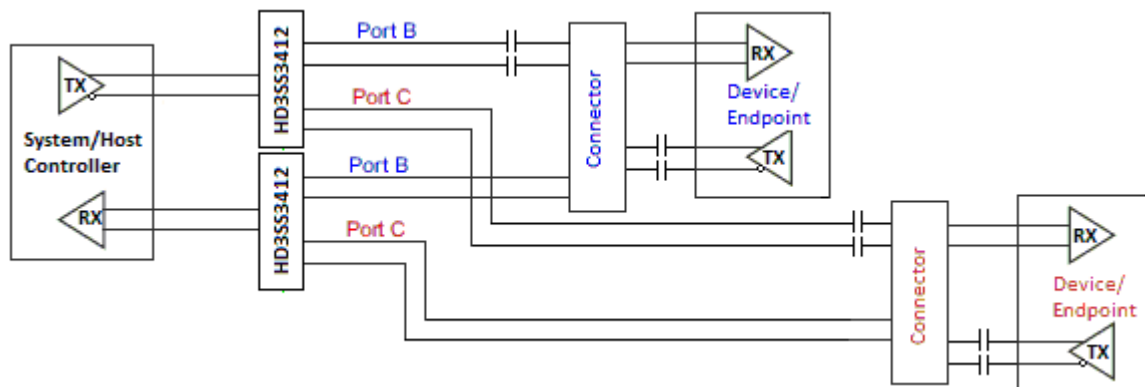**Figure 11. AC Coupling Capacitors Between Switch Tx and Endpoint Tx**

In Figure 12, the coupling capacitors are placed on the host transmit pair and endpoint transmit pair. In this situation, the switch on the top is biased by the endpoint and the lower switch is biased by the host controller.
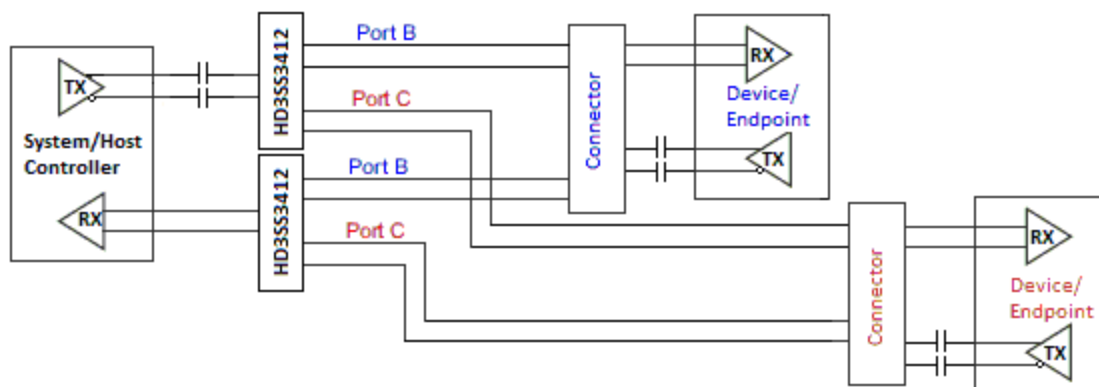
Figure 12. AC Coupling Capacitors on Host Tx and Endpoint Tx

Product Folder Links: *HD3SS3415*

Application Information (continued)

If the common-mode voltage in the system is higher than 2 V, the coupling capacitors are placed on both sides of the switch (shown in Figure 13). A biasing voltage of less than 2 V is required in this case.

Figure 13. AC Coupling Capacitors on Both Sides of Switch

10.2 Typical Application

Figure 14. Typical Application Schematic

Product Folder Links: *HD3SS3415*

Typical Application (continued)

10.2.1 Design Requirements

Table 3 lists the design parameters of this example.

Table 3. Design Parameters

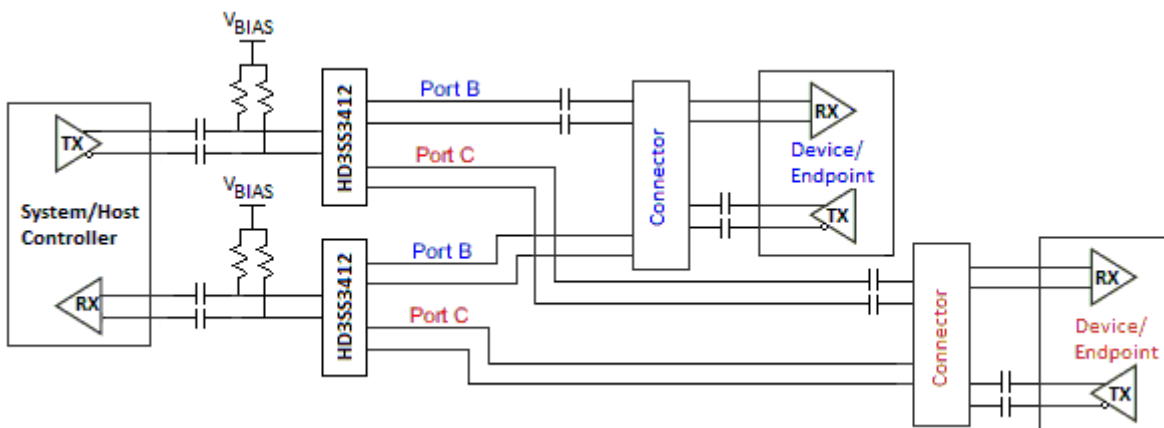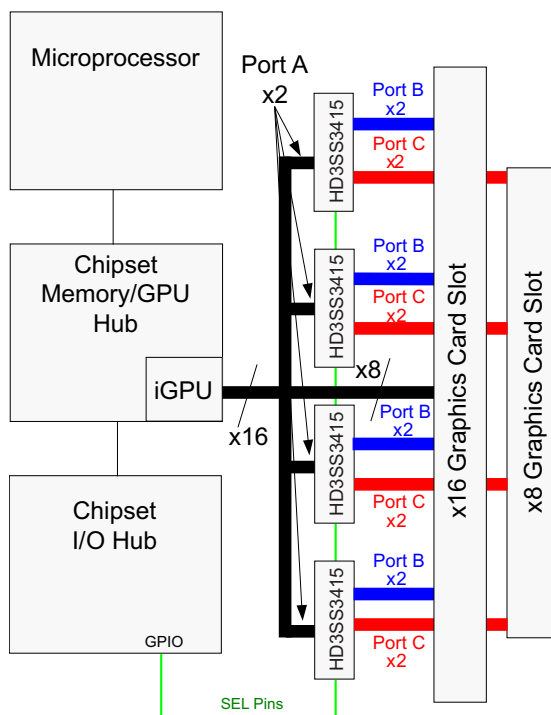| DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	3.3 V
Decoupling capacitors	0.1 µF
AC Capacitors	75 nF - 200 nF (100 nF shown) USBSS TX p and n lines require AC capacotprs. Alternate mode signals may or may not require AC capacitors

10.2.2 Detailed Design Procedure

- Connect VDD and GND pins to the power and ground planes of the printed circuit board, with a 0.1-uF bypass capacitor.
- Use +3.3-V TTL/CMOS logic level at SEL
- Use controlled-impedance transmission media for all the differential signals
- Ensure the received complimentary signals are with a differential amplitude of <1800 mVpp and a common-mode voltage of <2 V

10.2.3 Application Curves

Figure 15. 10 Gbps Source Eye Diagram at A: V_{ID} = 800 mVpp; 2^7-1 PRBS; V_{CM} = 0 V

Figure 16. 10 Gbps Output Eye Diagram at A: V_{ID} = 800 mVpp; 2^7-1 PRBS; V_{CM} = 0 V; V_{DD} = 3.3 V; SEL = 0 V

Product Folder Links: *HD3SS3415*
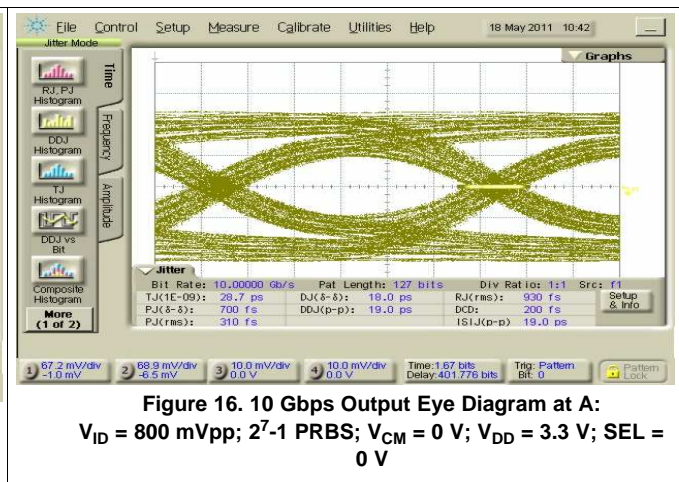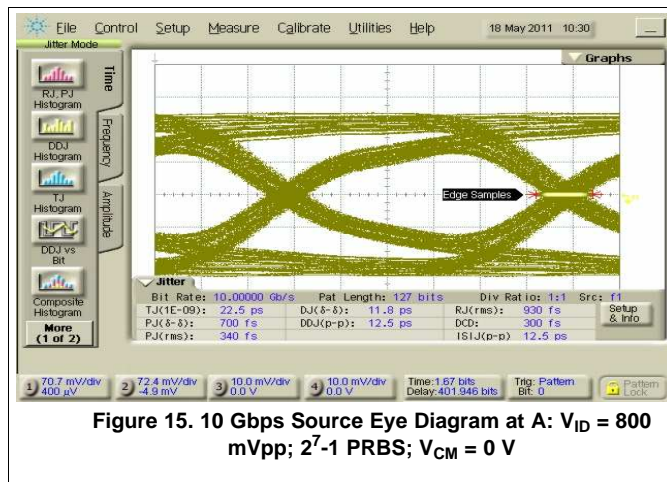
11 Power Supply Recommendations

The HD3SS3415 requires +3.3-V digital power sources. VDD 3.3 supply must have 0.1-µF bypass capacitors to VSS (ground) for proper operation. TI recommends one capacitor for each power terminal. Place the capacitor as close as possible to the terminal on the device and keep trace length to a minimum. Smaller value capacitors such as 0.01-µF are also recommended on the digital supply terminals.

12 Layout

12.1 Layout Guidelines

- Decoupling caps should be placed next to each power terminal on the HD3SS3415. Take care to minimize the stub length of the trace connecting the capacitor to the power pin.
- Avoid sharing vias between multiple decoupling caps.
- Place vias as close as possible to the decoupling cap solder pad.
- Widen VDD/GND planes to reduce effect of static and dynamic IR drop.
- The VBUS traces/planes must be wide enough to carry maximum of 2 A current
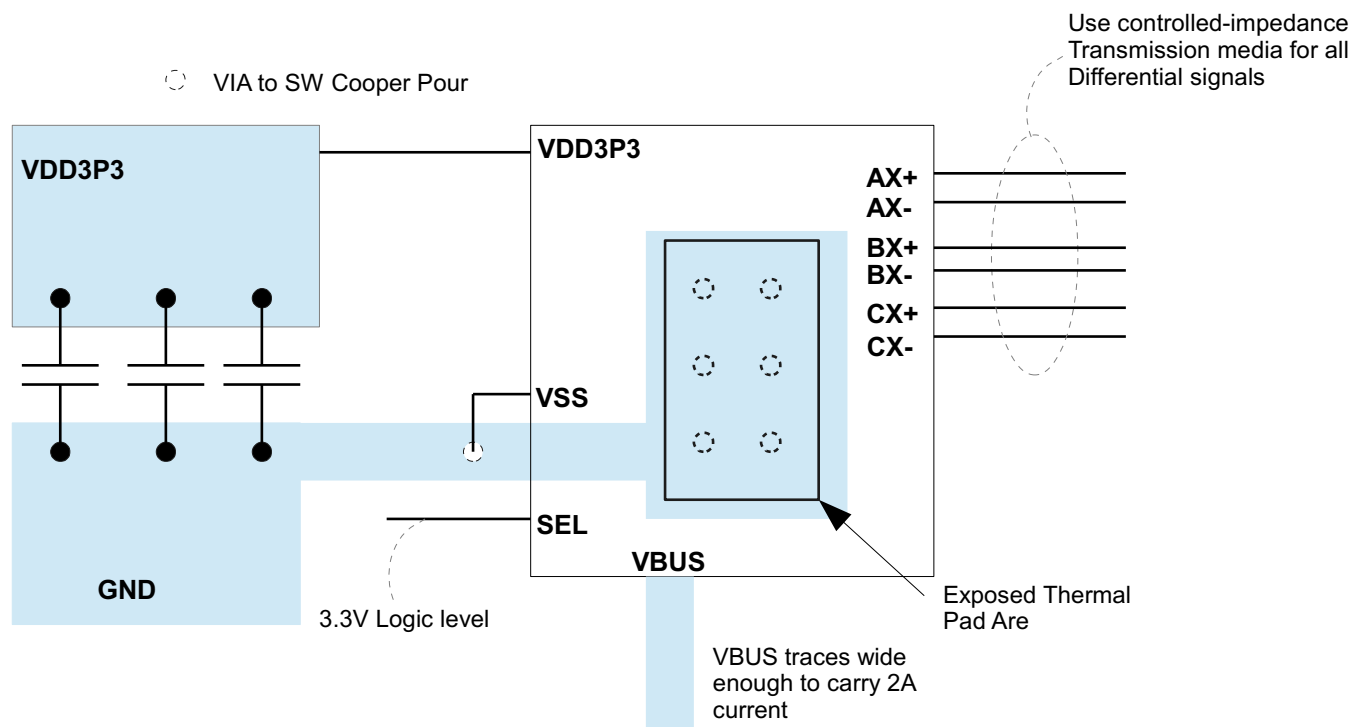
12.2 Layout Example

Figure 17. Layout Example

13 Device and Documentation Support

13.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HD3SS3415RUAR	ACTIVE	WQFN	RUA	42	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	HD3SS3415	Samples
HD3SS3415RUAT	ACTIVE	WQFN	RUA	42	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	HD3SS3415	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

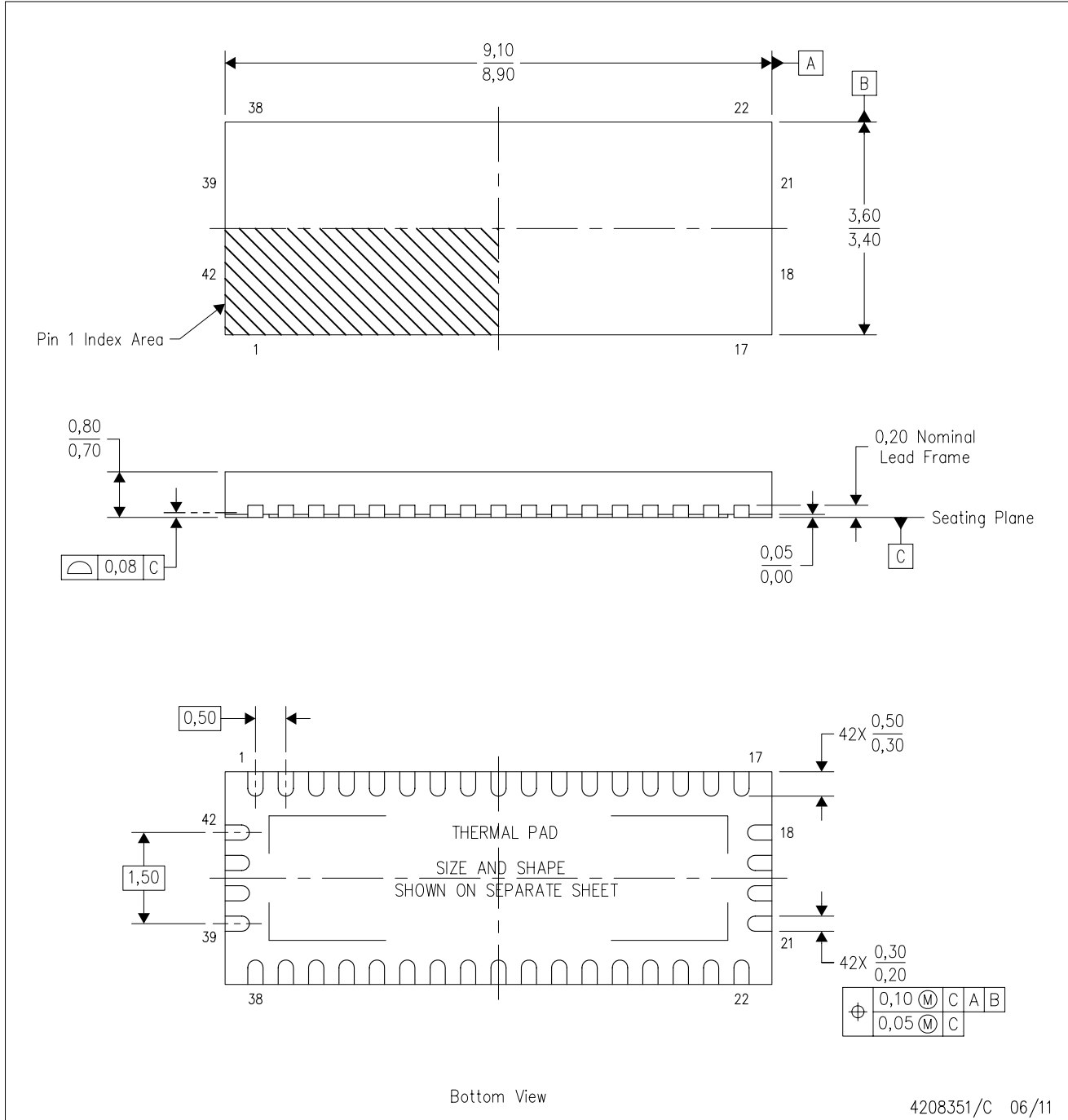| Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS3415RUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
HD3SS3415RUAT	WQFN	RUA	42	250	180.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS3415RUAR	WQFN	RUA	42	3000	367.0	367.0	38.0
HD3SS3415RUAT	WQFN	RUA	42	250	210.0	185.0	35.0

RUA (R−PWQFN−N42)   PLASTIC QUAD FLATPACK NO−LEAD

Pin 1 Index Area

0,20 Nominal
Lead Frame

Seating Plane

THERMAL PAD
SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

Bottom View

4208351/C 06/11

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   QFN (Quad Flatpack No−Lead) package configuration.
         D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

TEXAS
INSTRUMENTS
www.ti.com

RUA (R−PWQFN−N42)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Exposed
Thermal Pad

1   17

42   18

2,05±0,10

39   21

38   22

7,55±0,10

Bottom View
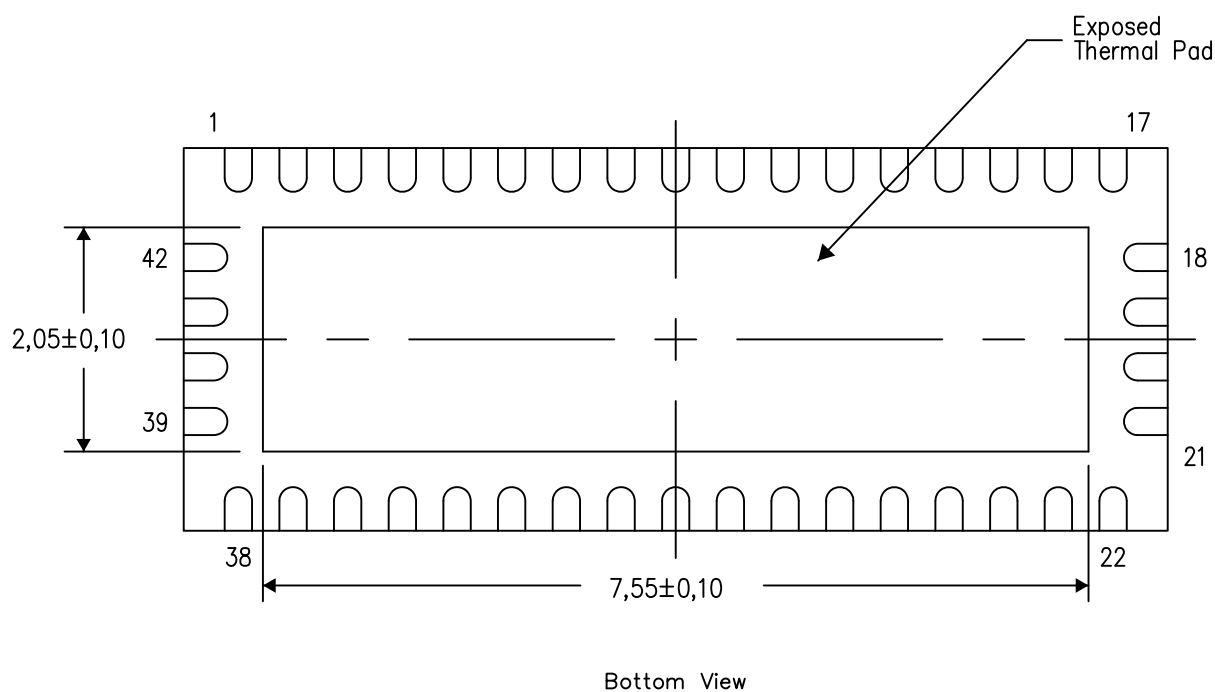
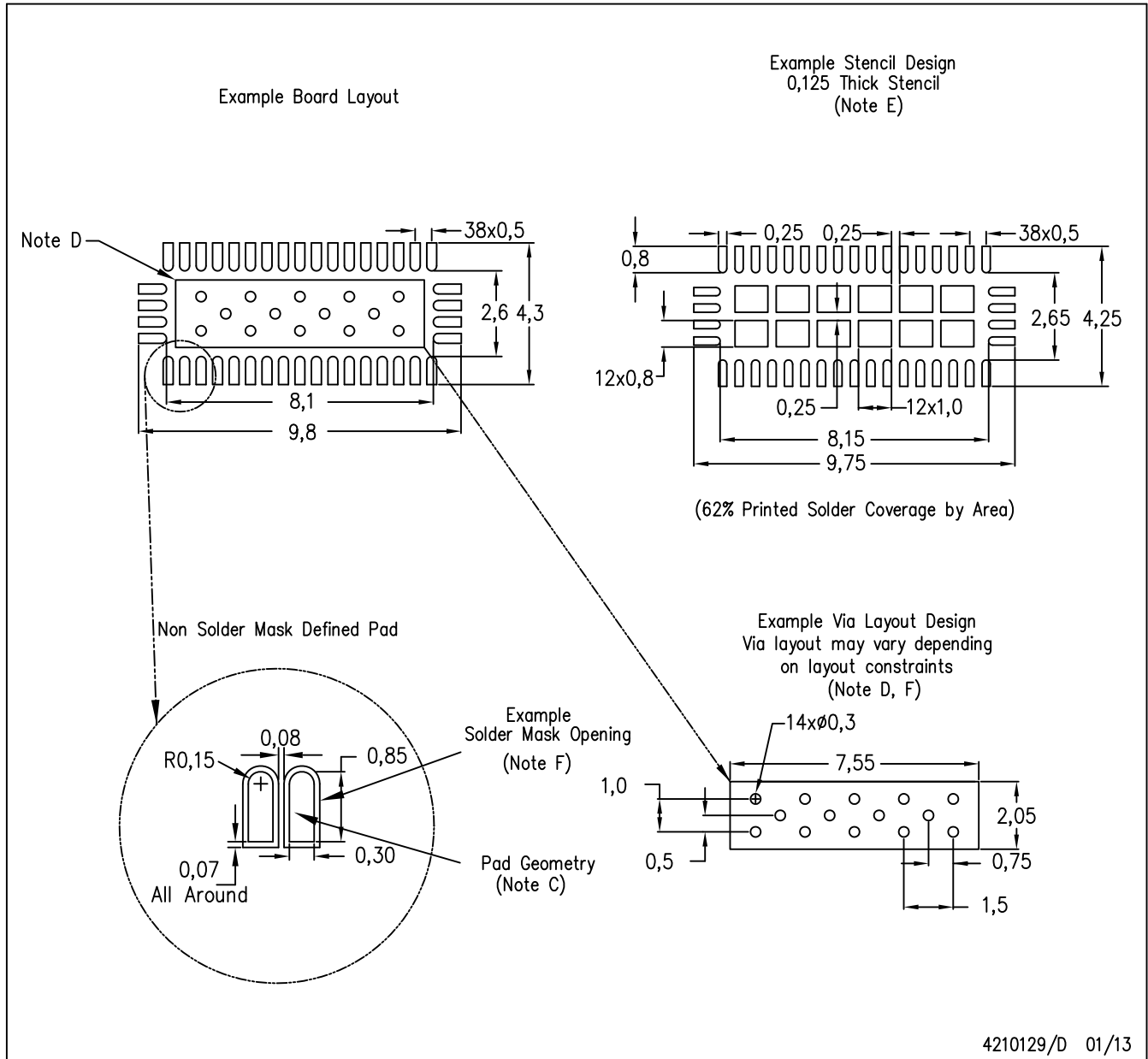Exposed Thermal Pad Dimensions

4208352/E 01/13

NOTE: All linear dimensions are in millimeters

RUA (R−PWQFN−N42)   PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout

Example Stencil Design
0,125 Thick Stencil
(Note E)

Note D

38x0,5

2,6 4,3

8,1

9,8

0,25 0,25

38x0,5

0,8

2,65 4,25

12x0,8

0,25

12x1,0

8,15

9,75

(62% Printed Solder Coverage by Area)

Non Solder Mask Defined Pad

Example Via Layout Design
Via layout may vary depending
on layout constraints
(Note D, F)

R0,15

0,08

0,85

Example
Solder Mask Opening
(Note F)

14x∅0,3

7,55

1,0

2,05

0,07
All Around

0,30

Pad Geometry
(Note C)

0,5

0,75

1,5

4210129/D 01/13

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack
            Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout. These documents are available at
            www.ti.com <http://www.ti.com>.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting
            recommendations for vias placed in the thermal pad.

TEXAS
INSTRUMENTS
www.ti.com

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		