ADS7924 2.2 V, 12-Bit, 4-Channel, MicroPOWER Analog-to-Digital Converter With I²C Interface

1 Features

- Intelligent Monitoring:
  - Auto-Sequencing of 4-Channel Multiplexer
  - Individual Alarm Thresholds for Each Channel
  - Programmable Scan Rate
- MicroPOWER™ Monitoring:
  - Four-Channel Scanning:
    - Every 1 ms → 25 µW
    - Every 10 ms → 5 µW
    - < 1 µA of Power-Down Current
  - Programmable Interrupt Pin Controls Shutdown/Wakeup of the Microcontroller
  - Auto Power-Down Control
  - PWRCON Pin Allows Shutdown of External Operational Amplifiers
- Wide Supply Range:
  - Analog Supply: 2.2 V to 5.5 V
  - Digital Supply: 1.65 V to 5.5 V
- Small Footprint: 3-mm × 3-mm QFN

2 Applications

- Portable and Battery-Powered Systems:
  - Medical, Communications, Remote Sensor Signal Monitoring, Power-Supply Monitoring
- Energy Harvesting

3 Description

The ADS7924 is a four-channel, 12-bit, analog-to-digital converter (ADC) with an I²C™ interface. With its low-power ADC core, support for low-supply operation, and a flexible measurement sequencer that essentially eliminates power consumption between conversions, the ADS7924 forms a complete monitoring system for power-critical applications such as battery-powered equipment and energy harvesting systems.

The ADS7924 features dedicated data registers and onboard programmable digital threshold comparators for each input. Alarm conditions can be programmed that generate an interrupt. The combination of data buffering, programmable threshold comparisons, and alarm interrupts minimize the host microcontroller time needed to supervise the ADS7924.

The four-channel input multiplexer (MUX) is routed through external pins to allow a common signal conditioning circuit to be used between the MUX and ADC, thereby reducing overall component count. The low-power ADC uses the analog supply as its reference and can acquire and convert signals in only 10 µs. An onboard oscillator eliminates the need to supply a master clock.

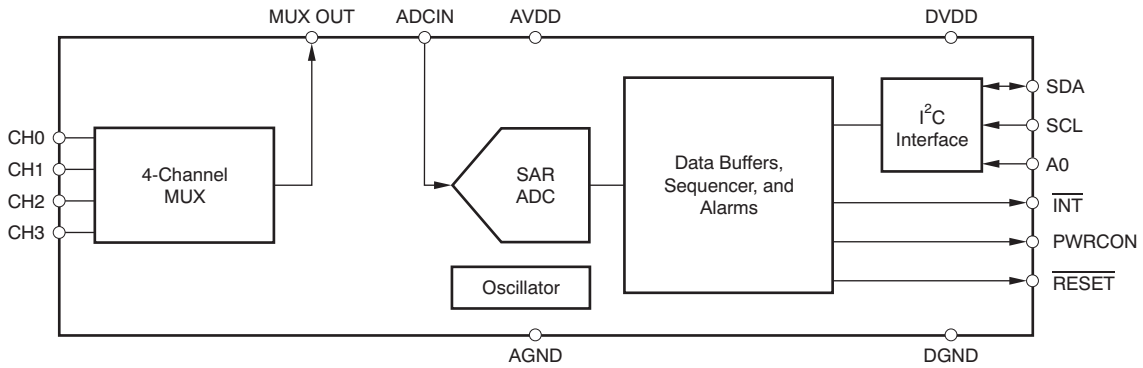
The ADS7924 is offered in a small 3-mm × 3-mm QFN and is fully specified for operation over the industrial temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS7924	WQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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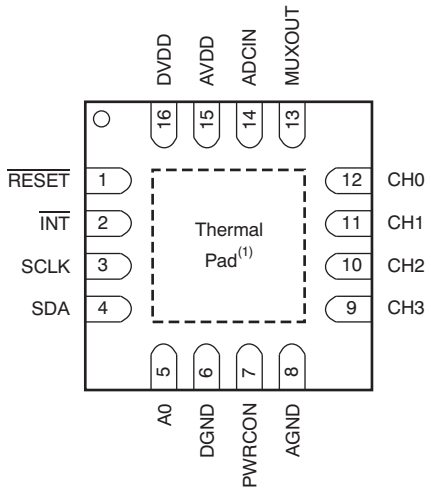
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2010) to Revision B	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

RTE Package
16-Pin WQFN
Top View



(1) Connect to AGND.

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{\text{RESET}}$	Digital input	External reset, active low
2	$\overline{\text{INT}}$	Digital output	Interrupt pin, active low; generated when input voltage is beyond programmed threshold
3	SCLK	Digital input	Serial clock input
4	SDA	Digital input/output	Serial data
5	A0	Digital input	I^2C address selection
6	DGND	Digital	Digital ground
7	PWRCON	Digital output	Power control pin to control shutdown/power-up of external operational amplifier
8	AGND	Analog	Analog ground
9	CH3	Analog input	Input channel 3
10	CH2	Analog input	Input channel 2
11	CH1	Analog input	Input channel 1
12	CH0	Analog input	Input channel 0
13	MUXOUT	Analog output	Multiplexer output
14	ADCIN	Analog input	ADC input
15	AVDD	Analog	Analog supply
16	DVDD	Digital	Digital supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

	MIN	MAX	UNIT
Supply voltage, AVDD to AGND	–0.3	6	V
Supply voltage, DVDD to DGND	–0.3	6	V
Supply voltage, DVDD to AVDD	AVDD ≥ DVDD		V
AGND to DGND	–0.3	0.3	V
Analog input voltage	AGND – 0.3	0.3	V
Digital input voltage with respect to DGND (SCL and SDA)	DGND – 0.3	6	V
Digital input voltage with respect to DGND (A0, $\overline{\text{RESET}}$)	DGND – 0.3	DVDD + 0.3	V
Input current to all pins except supply pins	–10	10	mA
Maximum operating temperature		125	°C
Storage temperature	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog Supply Voltage	2.2		5.5	V
DVDD	Digital Supply Voltage	1.65		AVDD	V

6.4 Thermal Information

THERMAL METRIC(1)		ADS7924 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	47.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	0.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

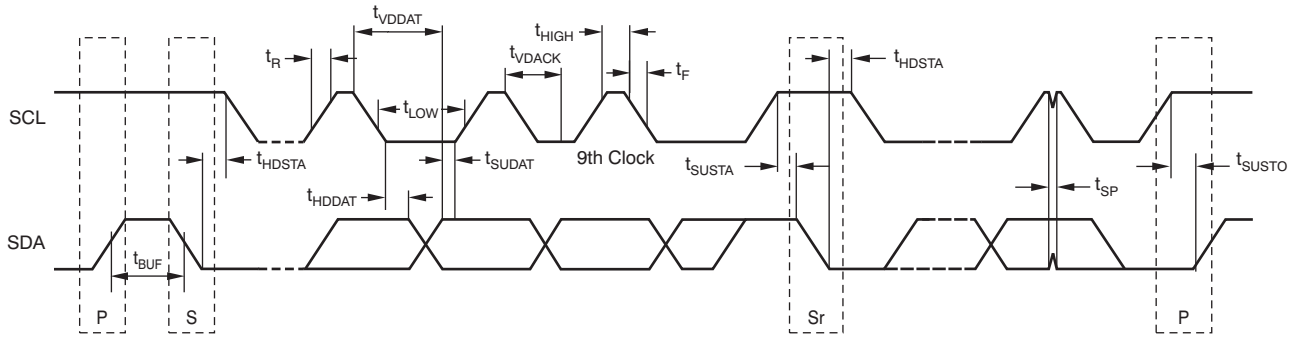
Minimum and maximum specifications are at T_A = –40°C to 85°C, 1.65 V < DVDD < 5.5 V, and 2.2 V < AVDD < 5.5 V. Typical specifications are at T_A = 25°C, AVDD = 5 V, and DVDD = 5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
Full-scale input span		(CHX – AGND)	0		AVDD	V
Input capacitance(1)				4	10	pF
ADC sampling capacitance				15		pF
MUX resistance				60		Ω
Input channel crosstalk				85		dB
SYSTEM PERFORMANCE						
Resolution				12		Bits
No missing codes			12			Bits
Integral linearity			–1.5	±0.5	1.5	LSBs
Differential linearity			–1	±0.6	1.5	LSBs
Offset error			–5		5	LSBs
Offset error drift				0.01		LSB/°C
Gain error			–0.2%	–0.01%	0.2%	
Gain error drift				0.6		ppm/°C
Noise (rms)				0.125		LSB
SAMPLING DYNAMICS						
Monitoring time/channel(2)				10		µs
CLOCK						
Internal clock frequency variation				±20%		
DIGITAL INPUT/OUTPUT						
Logic family				CMOS		
Logic level:						
V_{IH} (SDA, SCL, A0, $\overline{RESET}$)			0.8 DVDD		DVDD + 0.3	V
V_{IL} (SDA, SCL, A0, $\overline{RESET}$)			DGND – 0.3		0.4	V
Input current	I_I	V_I = DVDD or DGND	–10		10	µA
V_{OH} (PWRCON, $\overline{INT}$)		I_{OH} = 100 µA, $\overline{INT}$ pin	0.8 DVDD		DVDD	V
		I_{OH} = 100 µA, PWRCON pin	0.8 AVDD		AVDD	V
V_{OL} (PWRCON, $\overline{INT}$, SDA)		I_{OL} = 100 µA	DGND		0.4	V
Low-level output current	I_{OL}	SDA pin, V_{OL} = 0.6 V			3	mA
Load capacitance	C_B	SDA pin			400	pF
Data format				Straight binary		
POWER-SUPPLY REQUIREMENTS						
Power-supply voltage:						
DVDD(3)			1.65		5.5	V
AVDD			2.2		5.5	V
I_{AVDD}(4)		t_{CYCLE} = 2.5 ms, AVDD = 2.2 V		5	8	µA
I_{PWRD}, power-down current				<1		µA
TEMPERATURE RANGE						
Specified performance			–40		85	°C

(1) CH0 to CH3 input pin capacitance.
(2) Rate at which channels can be scanned. This is the minimum acquisition time (6 µs) and conversion time (4 µs).
(3) DVDD cannot exceed AVDD.
(4) See Figure 3 and Figure 4 for more information.

6.6 I²C Timing Requirements

		MIN	MAX	UNIT
f_{SCL}	SCL operating frequency	0	0.4	MHz
t_{BUF}	Bus free time between START and STOP condition	1.3		µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock is generated.	600		ns
t_{SUSTA}	Repeated START condition setup time	600		ns
t_{SUSTO}	Stop condition setup time	600		ns
t_{HDDAT}	Data hold time	0		ns
t_{SUDAT}	Data setup time	100		ns
t_{LOW}	SCL clock low period	1300		ns
t_{HIGH}	SCL clock high period	600		ns
t_F	Clock/data fall time		300	ns
t_R	Clock/data rise time		300	ns
t_{VDDAT}	Data valid time		0.9	µs
t_{VDACK}	Data valid acknowledge time		0.9	µs
t_{SP}	Pulse width of spike that must be suppressed by the input filter	0	50	ns



NOTE: S = Start, Sr = Repeated Start, and P = Stop.

Figure 1. I²C Timing Diagram

6.7 Typical Characteristics

At T_A = 25°C, unless otherwise noted.

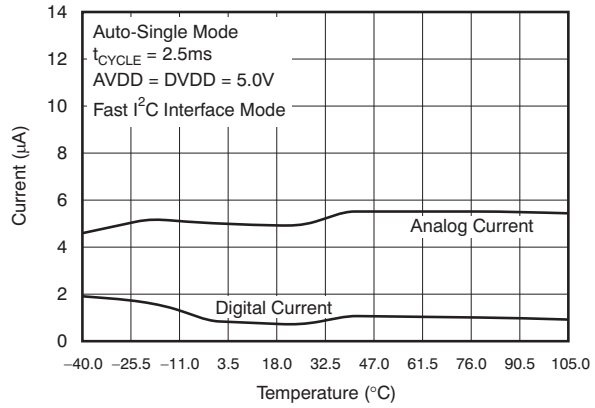


Figure 2. Current vs Temperature

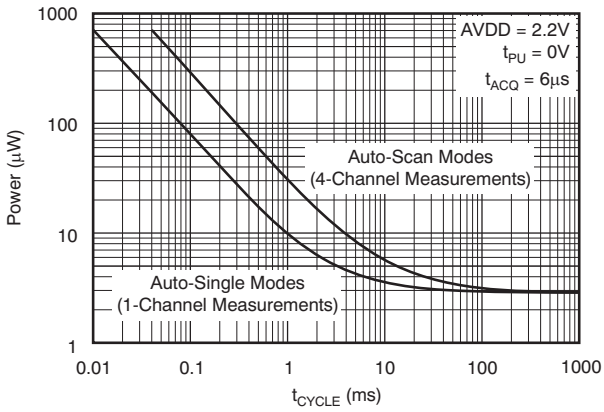


Figure 3. Average Power Dissipation vs Cycle Time

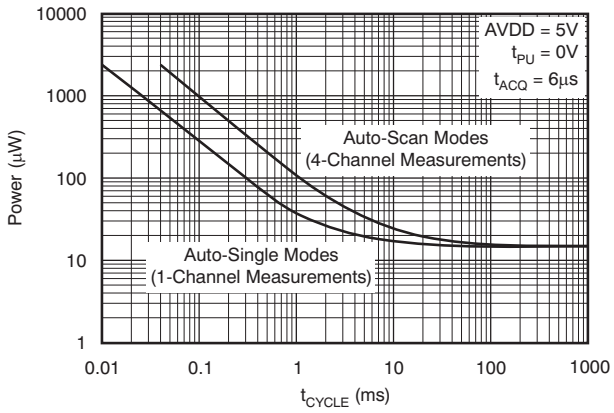


Figure 4. Average Power Dissipation vs Cycle Time

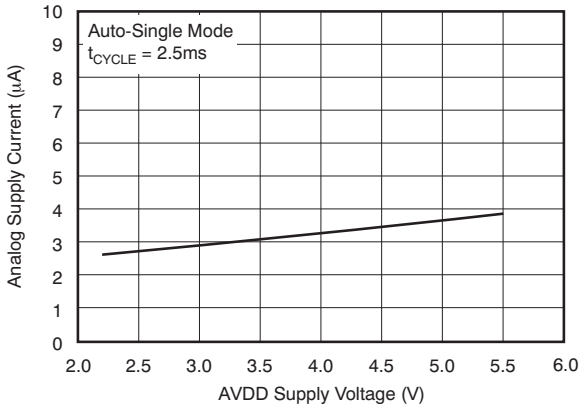


Figure 5. Analog Supply Current vs Supply Voltage

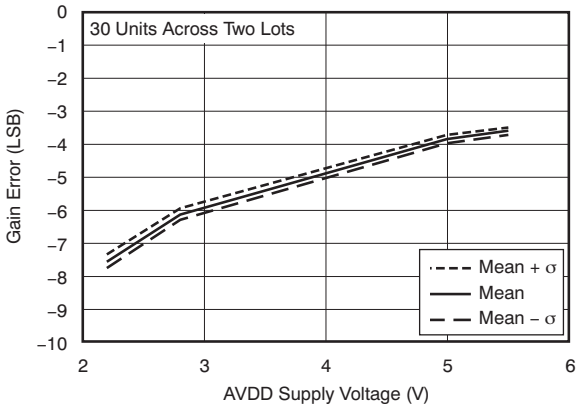


Figure 6. Typical Gain Error vs AVDD Voltage

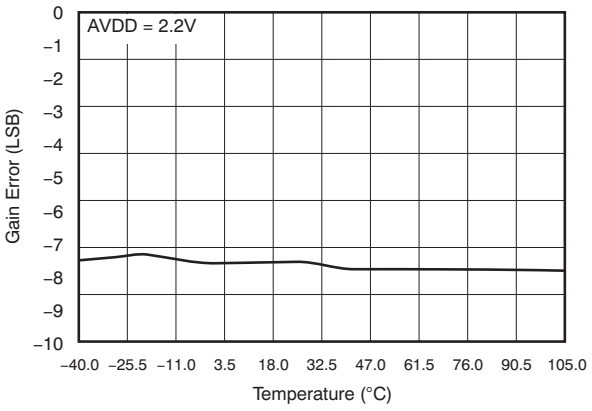


Figure 7. Gain Error Drift

Typical Characteristics (continued)

At T_A = 25°C, unless otherwise noted.

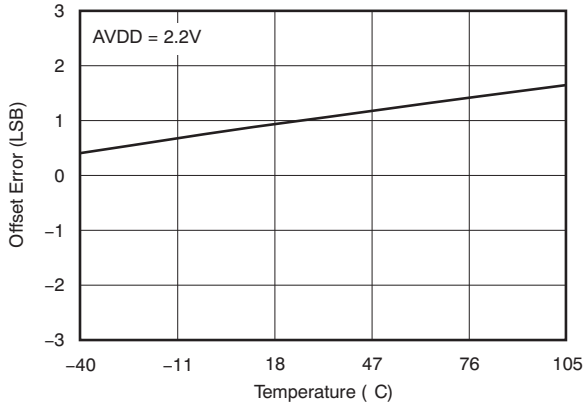


Figure 8. Offset Error Drift, Typical

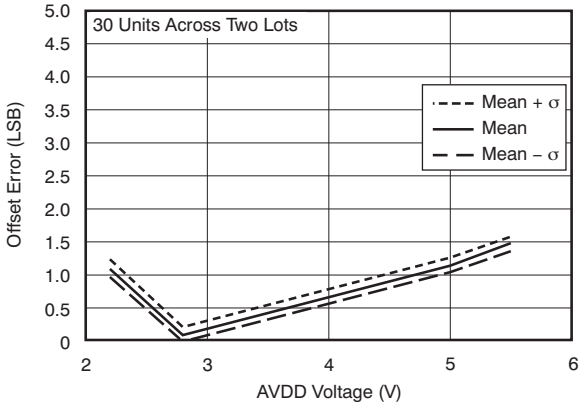


Figure 9. Typical Offset Error vs AVDD Voltage

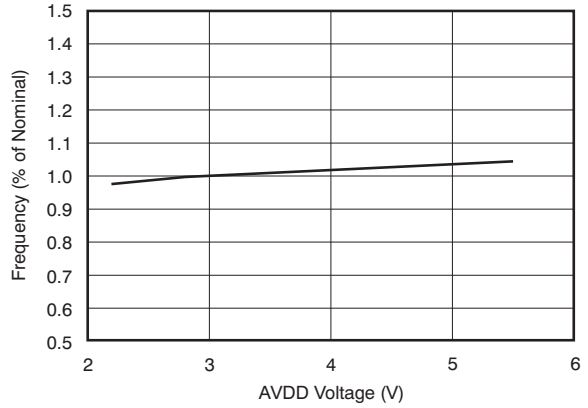


Figure 10. Internal Oscillator Frequency vs Voltage

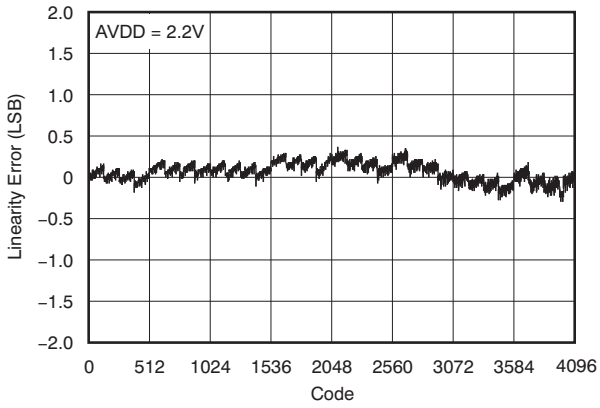


Figure 11. Integral Nonlinearity

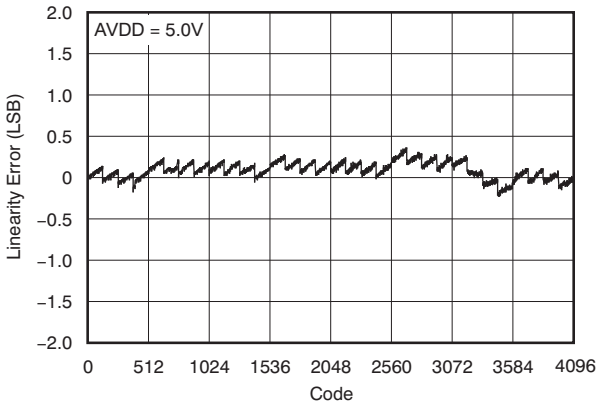


Figure 12. Integral Nonlinearity

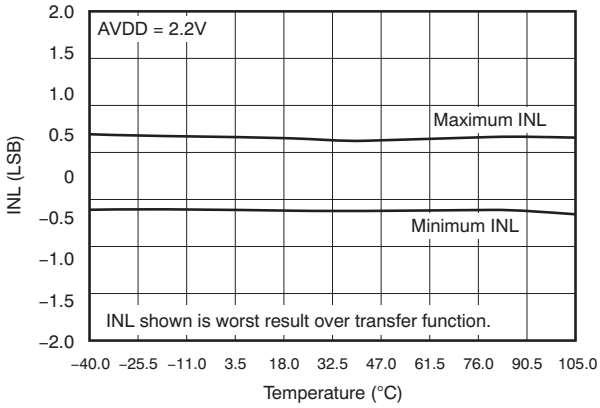


Figure 13. Integral Linearity Error Drift

Typical Characteristics (continued)

At T_A = 25°C, unless otherwise noted.

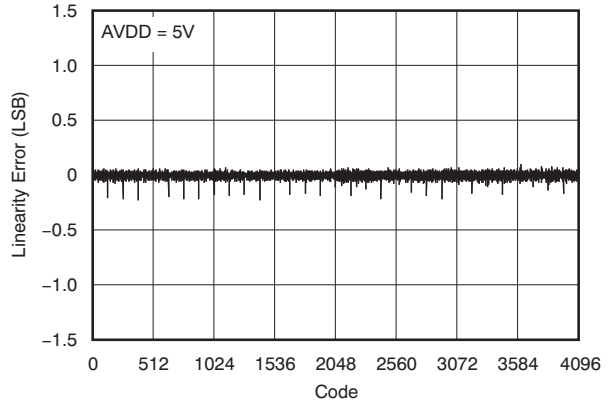


Figure 14. Differential Nonlinearity

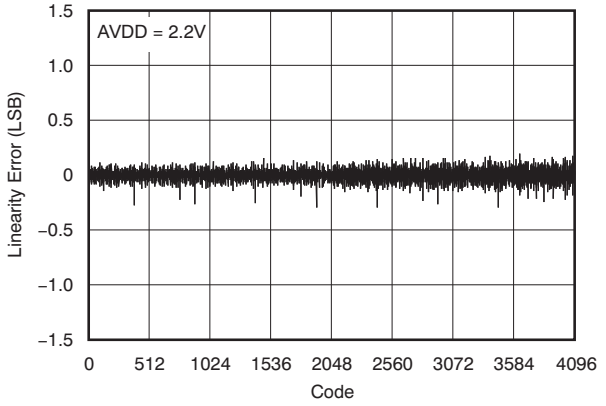


Figure 15. Differential Nonlinearity

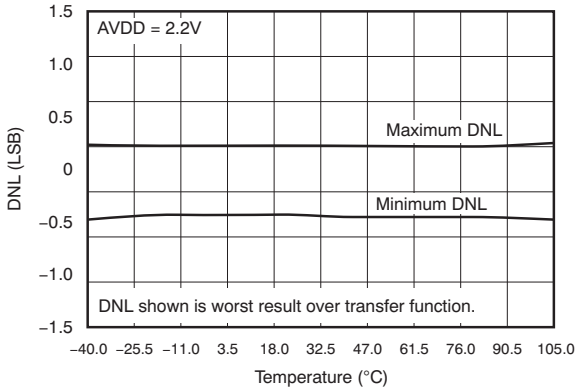


Figure 16. Differential Nonlinearity vs Temperature

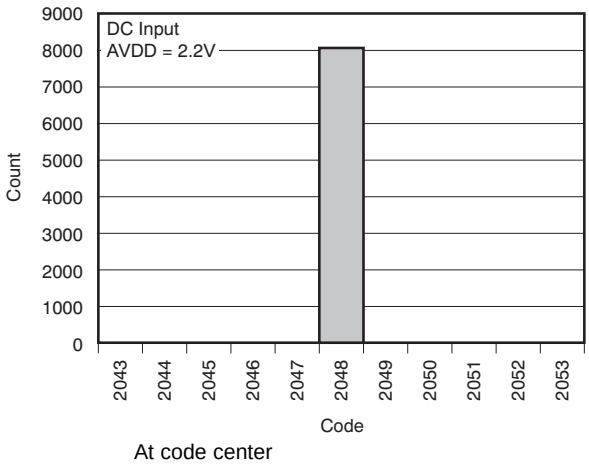


Figure 17. Noise Histogram (1)

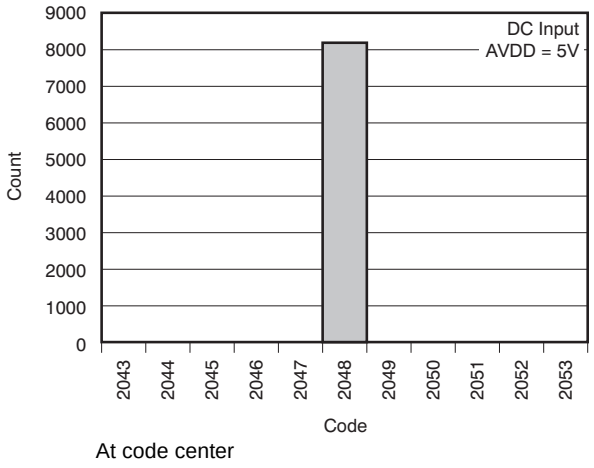


Figure 18. Noise Histogram

(1) At code center.

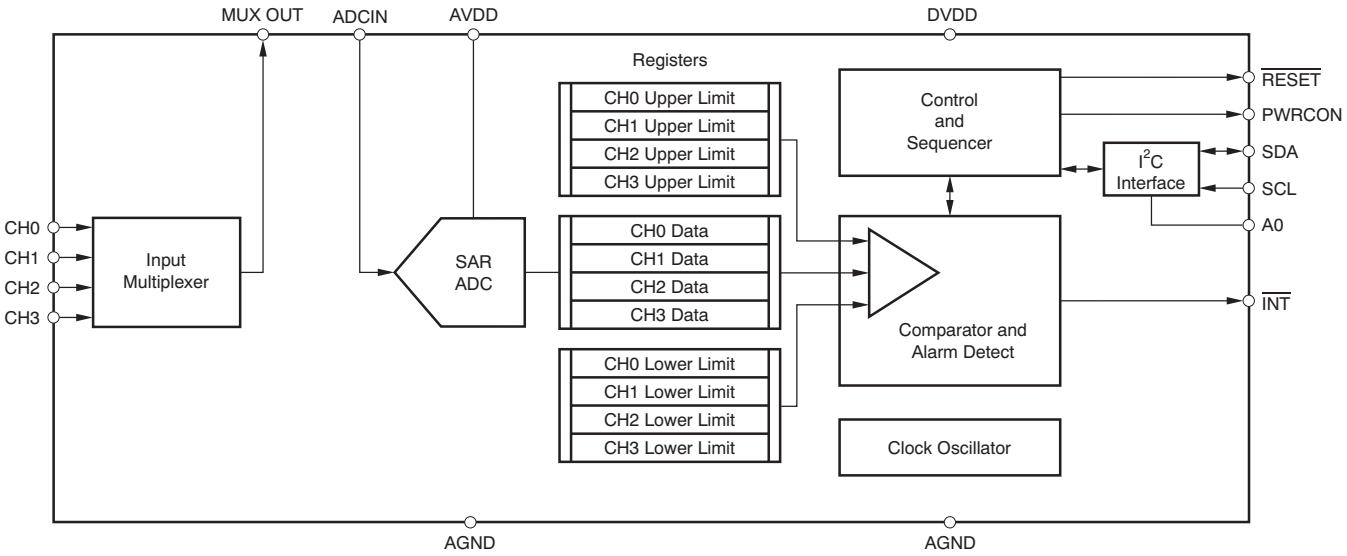
7 Detailed Description

7.1 Overview

The ADS7924 is a miniature, four-channel, multiplexed, 12-bit, analog-to-digital converter (ADC) with an I^2C serial interface. Functional Block Diagram shows a block diagram. The four-channel input multiplexer is routed through external pins to allow a common signal conditioning block to be used for all four channels. The PWRCON digital output can be used to shut down active circuitry used in the signal conditioning; see the *Application and Implementation* section for additional details.

The successive-approximation-register (SAR) ADC performs a no-latency conversion on the selected input channel and stores the data in a dedicated register. A digital threshold comparator with programmable upper and lower limits can be enabled and used to create an alarm monitor. A dedicated interrupt output pin ($\overline{INT}$) indicates when an alarm occurs. Two I^2C addresses are available and are selected with the dedicated digital input pin A0. Both standard and fast mode formats for I^2C are supported.

7.2 Functional Block Diagram

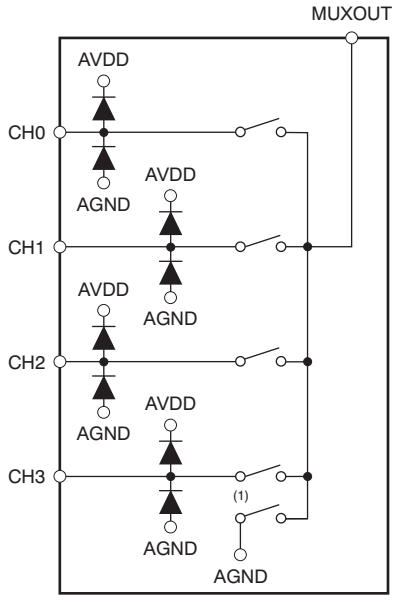


7.3 Feature Description

7.3.1 Multiplexer

The ADS7924 has a four-channel, single-ended input multiplexer. As Figure 19 shows, ESD diodes protect the inputs. Make sure these diodes do not turn on by staying within the absolute input voltage range specification. The MUXOUT pin can be connected to AGND within the multiplexer (for example, to provide a test signal of 0 V or as part of a calibration procedure). See the *Figure 55* register in the *Register Map* section for more details

Feature Description (continued)



(1) See the *Figure 55* register in the *Register Map* section.

Figure 19. ADS7924 Multiplexer

7.3.2 ADC Input

The ADC Input (ADCIN) pin provides a single-ended input to the 12-bit successive approximation register (SAR) ADC. This pin is protected with ESD diodes in the same way as the multiplexer inputs. While acquiring the signal during the t_{ACQ} interval, the ADC sampling capacitor is connected to the ADCIN pin. While converting during the t_{CONV} interval, the sampling capacitor is disconnected from the ADCIN pin, and the conversion process determines the voltage that was sampled.

7.3.3 Reference

The analog supply voltage (AVDD) is used as the reference. Power to the ADS7924 should be clean and well bypassed. A 0.1-µF ceramic capacitor must be placed as close as possible to the ADS7924 package. In addition, a 1-µF to 10-µF capacitor and a 5-Ω to 10-Ω series resistor may be used to low-pass filter a noisy supply.

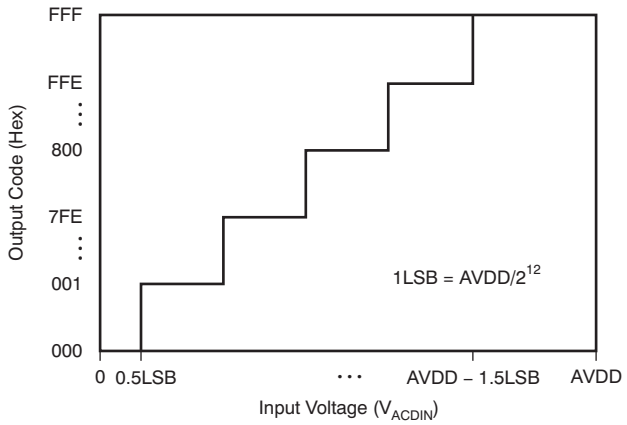
7.3.4 Clock

The ADS7924 uses an internal clock. The clock speed determines the various timing settings such as conversion time, acquisition time, and so forth.

7.3.5 Data Format

The ADS7924 provides 12 bits of data in unipolar format. The positive full-scale input produces an output code of FFFh and a zero input produces an output code of 0h. The output clips at these codes for signals that either exceed full-scale or go below '0'. Figure 20 shows code transitions versus input voltage.

Feature Description (continued)



(1) Excludes the effects of noise, INL, offset, and gain errors.

Figure 20. ADS7924 Code Transition Diagram(1)

7.3.6 ADC Conversion Timing

The ADS7924 provides a flexible timing arrangement to support a wide variety of measurement needs. Three user-controlled timings include power up (t_{PU}), acquisition (t_{ACQ}), and sleep (t_{SLEEP}) plus a fixed conversion time (t_{CONV}).

7.3.6.1 Power-Up Time

The power-up time is allowed to elapse whenever the device has been shutdown in idle mode. Power-up time can allow external circuits, such as an operational amplifier, between the MUXOUT and ADCIN pins to turn on. The nominal time programmed by the PUTIME[4:0] register bits is given by Equation 1:

$$t_{PU} = \text{PWRUPTIME[4:0]} \times 2\ \mu s \quad (1)$$

For example, if PWRUPTIME is set to 25 ('011001') then 50 µs is allowed to elapse before beginning the acquisition time. If a power-up time is not required, set the bits to '0' to effectively bypass.

7.3.6.2 Acquisition Time

The acquisition time is allowed to elapse before beginning a conversion. During this time, the ADC acquires the signal. The minimum acquisition time is 6 µs. The nominal time programmed by the ACQTIME[4:0] register bits is given by Equation 2:

$$t_{ACQ} = (\text{ACQTIME[4:0]} \times 2\ \mu s) + 6\ \mu s \quad (2)$$

For example, if ACQTIME is set to 30 ('011110') then 66 µs is allowed to acquire the input signal. If an acquisition time greater than 6 µs is not required, set the bits to '0'.

7.3.6.3 Conversion Time

The conversion time is always 4 µs and cannot be programmed by the user.

7.3.6.4 Sleep Time

The sleep time is allowed to elapse after conversions in the Auto-Single with Sleep, Auto-Scan with Sleep, and Auto-Burst Scan with Sleep modes. The nominal time programmed by the SLPTIME registers can be increased by a factor of eight using the SLPMULT8 bit or decreased by a factor of four using the SLPDIV4 bit.

7.3.7 Interrupt Output ($\overline{\text{INT}}$)

The ADS7924 offers a dedicated output pin ($\overline{\text{INT}}$) for signaling an interrupt condition. The $\overline{\text{INT}}$ pin can be configured to activate when the ADC is busy with a conversion, when data are ready for retrieval, or when an alarm condition occurs; see the *Figure 52* register in the *Register Map* section.

Feature Description (continued)

To clear an interrupt from an alarm condition, read the INTCONFIG register (12h). To clear an interrupt from data ready, read the data registers. The interrupt clears when the lower four bits are retrieved.

The $\overline{\text{INT}}$ pin can be configured to generate a static output (useful for a host controller monitoring for a level) or a pulse output (useful for a host controller monitoring for a edge transition). When a pulse output is selected, the nominal pulse width is 250 ns. The Interrupt Control Register should be read to clear the interrupt.

7.3.8 PWRCON

The PWRCON pin allows the user to synchronize the shutdown/wakeup of an external operational amplifier with the ADC conversion cycle. This feature provides further power reduction and can be useful in applications where the time difference between consecutive signal captures is large. The PWRCON pin can drive up to 3 mA of current and its output voltage is the same as AVDD. This pin is controlled by the PWRCONFIG register.

7.3.9 Alarm

The ADS7924 offers an independent alarm function for each input channel. An 8-bit window comparator can be enabled to test the ADC conversion result against an upper limit set by the ULR register and against a lower limit set by the LLR register. If the conversion result is less than or equal to the LLR threshold value or greater than or equal to the ULR threshold value, the comparator is tripped. There are separate upper and lower registers for each input channel.

A programmable counter determines how many comparator trips it takes to generate an alarm. A separate counter is used for each channel and is incremented whenever the comparator trips, either for the upper or lower thresholds. That is, an ADC conversion result on channel 1 that exceeds the ULR threshold or falls below the LLR threshold increments the counter for that channel. Figure 21 shows a conceptual diagram of the window comparator and alarm circuitry.

When an alarm occurs, the $\overline{\text{INT}}$ pin can be configured to generate an interrupt. The channel that generated the alarm can be read from the registers. A read of the Interrupt Control register clears the alarm register and also resets the alarm counter.

7.4 Device Functional Modes

7.4.1 ADC Operating Modes

The ADS7924 offers multiple operating modes to support a variety of monitoring needs. Conversions can either be started manually or set to automatically continue. The mode is set by writing to the MODE register, and changes take effect as soon as the write completes. Table 1 gives a brief description of each mode.

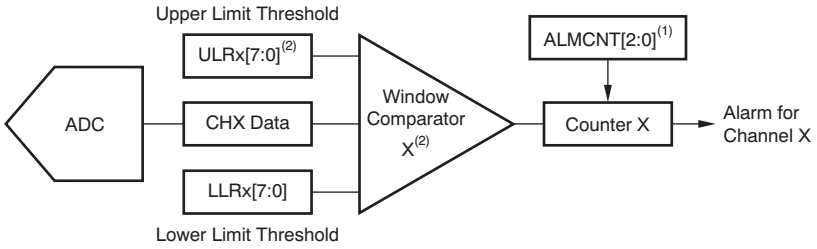
7.4.1.1 Idle Mode

Use this mode to save power when not converting. All circuits are shut down.

7.4.1.2 Awake Mode

All circuits are operating in this mode and the ADC is ready to convert. When switching between modes, be sure to first select the Awake mode and then switch to the desired mode. This procedure ensures the internal control logic is properly synchronized.

Device Functional Modes (continued)



(1) The same ALMCNT value is used for all four window comparators.

(2) X = 0 to 3.

Figure 21. Window Comparator and Alarm Conceptual Block Diagram

Table 1. Mode Descriptions

MODE	DESCRIPTION
Idle	All circuits shutdown; lowest power setting
Awake	All circuits awake and ready to convert
Manual-Single	Select input channel is converted once
Manual-Scan	All input channels are converted once
Auto-Single	One input channel is continuously converted
Auto-Scan	All input channels are continuously converted
Auto-Single with Sleep	One input channel is continuously converted with programmable sleep time between conversions
Auto-Scan with Sleep	All input channels are continuously converted with programmable sleep time between conversions
Auto-Burst Scan with Sleep	All input channels are converted with minimal delay followed by a programmable sleep time

7.4.1.3 Manual-Single Mode

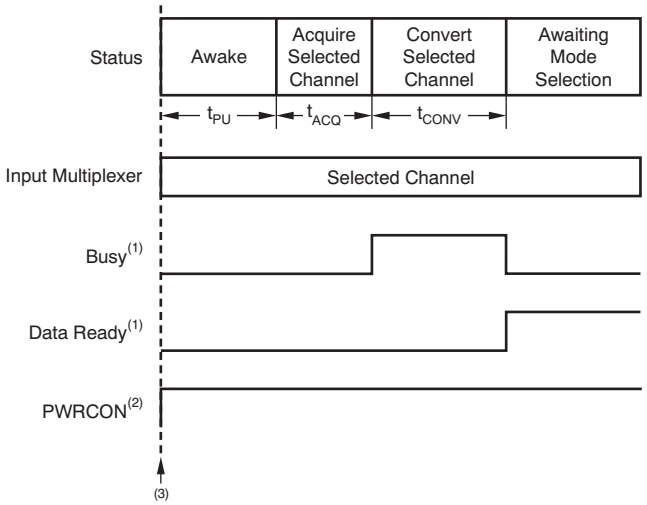
This mode converts the selected channel once, as shown in Figure 22. After the ADC Mode Control register is written, the power-up time (t_{PU}) and acquisition time (t_{ACQ}) are allowed to elapse. t_{PU} can be set to '0' to effectively bypass if not needed. t_{ACQ} time is programmable through the ACQCONFIG register, bits[4:0]. Sleep time (t_{SLEEP}) is not used in this mode.

After the conversion completes, the device waits for a new mode to be set. This mode can be set to Idle to save power. When t_{PU} and t_{ACQ} are very short, the very short conversion time needed allows a read register operation to be issued on the I^2C bus immediately after the write operation that initiates this mode.

NOTE

t_{PU} only applies to the first manual-single command.

If multiple conversions are needed, the manual-single mode can be reissued without requiring the awake mode to be issued in between. Consecutive manual-single commands have no t_{PU} period.



(1) Busy and data ready are internal signals shown as active high that can be routed to the $\overline{INT}$ pin for external monitoring.

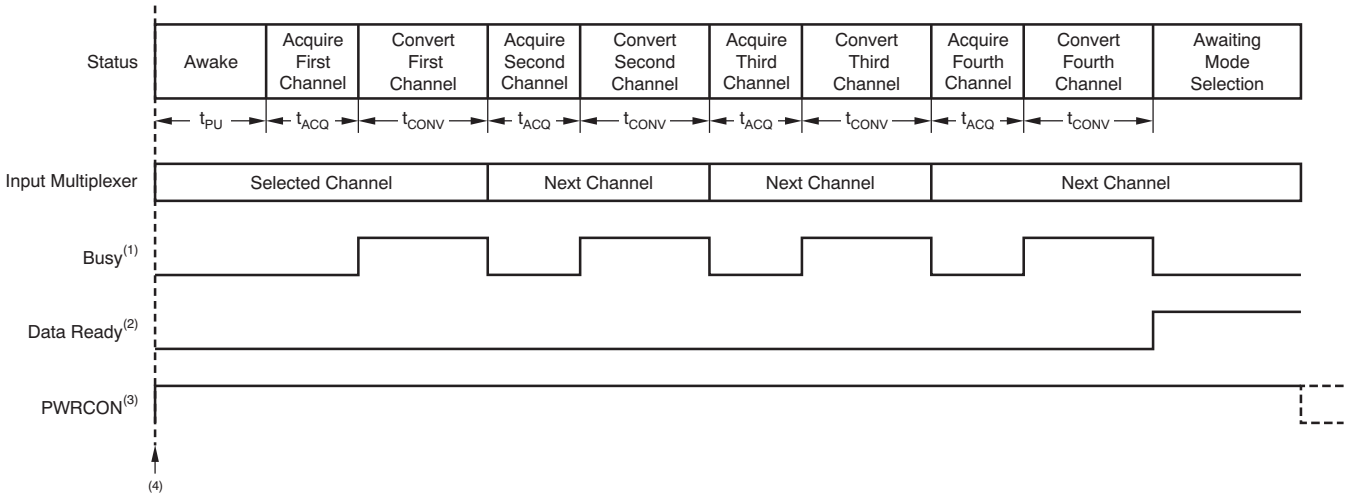
(2) PWRCON is shown enabled and active high.

(3) The mode begins on the trailing edge of the I^2C acknowledge after writing to the MODECNTL register.

Figure 22. Manual-Single Operation Example

7.4.1.4 Manual-Scan Mode

This mode converts all of the channels once, starting with the selected channel, as illustrated in Figure 23. After the ADC Mode Control register is written, the power-up time (t_{PU}) is allowed to elapse. This value can be set to '0' to effectively bypass if not needed. Before each conversion, an acquisition time (t_{ACQ}) is allowed to elapse. t_{ACK} time is programmable through the ACQCONFIG register, bits[4:0]. Sleep time (t_{SLEEP}) is not used in this mode. The input multiplexer is automatically incremented as the conversions complete. If, for example, the initial selected channel is CH2, the conversion order is CH2, CH3, CH0, and CH1. Data from the conversions are always put into the data register that corresponds to a particular channel. For example, CH2 data always goes in register DATA2_H and DATA2_L regardless of conversion order. After all four conversions complete, the device waits for a new mode to be set. This mode can be set to Idle afterwards to save power. The $\overline{INT}$ pin can be configured to indicate the completion of each individual conversion or it can wait until all four finish. In either case, the appropriate data register is updated after each conversion. These registers can be read at any time afterwards. If multiple scan are needed, the manual-scan mode can be reissued without requiring the Awake mode to be issued in between.



(1) Busy is an internal signal shown as active high that can be routed to the $\overline{INT}$ pin for external monitoring.

(2) Data ready is an internal signal shown as active high and is enabled when all conversions are complete. It can be routed to the $\overline{INT}$ pin for external monitoring.

(3) PWRCON is shown enabled and active high.

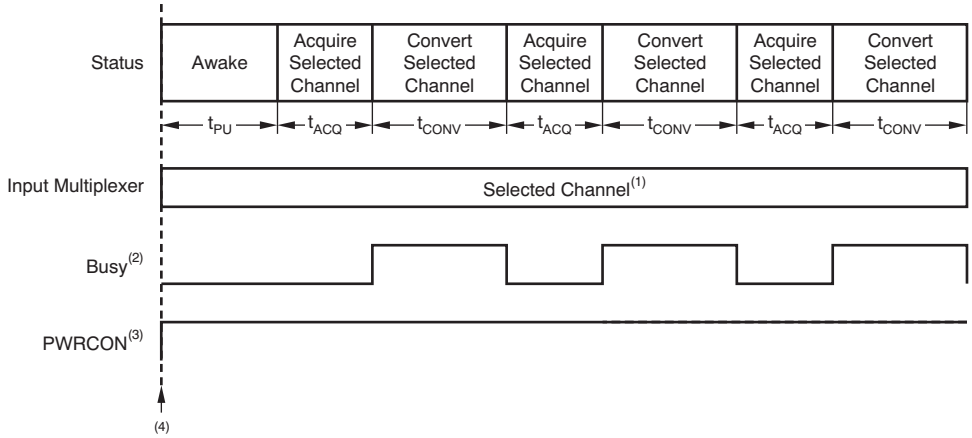
(4) The mode begins on the trailing edge of the I^2C acknowledge after writing to the MODECNTL register.

Figure 23. Manual-Scan Operation Example

7.4.1.5 Auto-Single Mode

This mode automatically converts the selected channel continuously, as shown in Figure 24. After the ADC Mode Control register is written, the power-up time (t_{PU}) is allowed to elapse. This value can be set to '0' to effectively bypass if not needed. Before the conversion, an acquisition time (t_{ACQ}) is allowed to elapse. t_{ACQ} time is programmable through the ACQCONFIG register, bits[4:0]. Sleep time (t_{SLEEP}) is not used in this mode. After the conversion completes the cycle is repeated.

This mode can be used with the onboard digital comparator to monitor the status of an input signal with little support needed from a host microcontroller. The conversion time is less than the I^2C data retrieval time. TI suggests stopping this mode by setting the mode to Idle or stopping the conversion by configuring the alarm to do so, before retrieving data. The alarm can also be configured to continue the conversion even after an interrupt is generated.



(1) Same channel is continuously converted.

(2) Busy is an internal signal shown as active high that can be routed to the $\overline{INT}$ pin for external monitoring.

(3) PWRCON is shown enabled and active high.

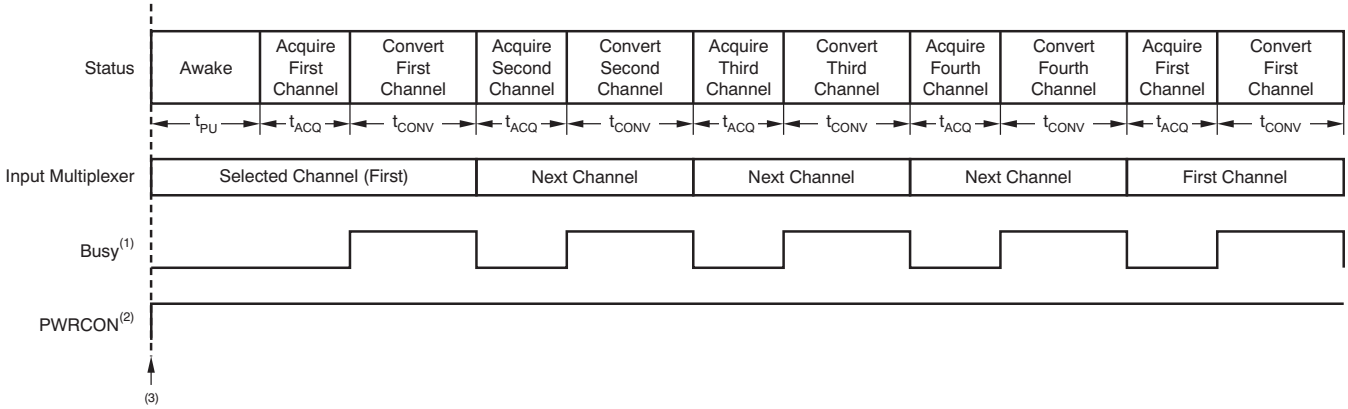
(4) The mode begins on the trailing edge of the I^2C acknowledge after writing to the MODECNTL register.

Figure 24. Example of Auto-Single Operation

7.4.1.6 Auto-Scan Mode

This mode automatically converts all the channels continuously, starting with the selected channel, as illustrated in Figure 25. After the ADC Mode Control register is written, the power-up time (t_{PU}) is allowed to elapse. This value can be set to '0' to effectively bypass if not needed. Before the conversion, an acquisition time (t_{ACQ}) is allowed to elapse. t_{ACQ} time is programmable through the ACQCONFIG register, bits[4:0]. Sleep time (t_{SLEEP}) is not used in this mode. The input multiplexer is automatically incremented as the conversions complete. If, for example, the initial selected channel is CH2, the conversion order is CH2, CH3, CH0, CH1, CH2, CH3, and so forth. until the mode is stopped. Data from the conversions are always put into the data register that corresponds to a particular channel. For example, CH2 data always go in register DATA2_H and DATA2_L regardless of conversion order.

This mode can be used with the onboard digital comparator to monitor the status of the input signals with little support needed from a host microcontroller. TI suggests interrupting this mode and stopping the automatic conversions, either by setting the mode to Idle or configuring the alarm to do so, before retrieving data.



(1) Busy is an internal signal shown as active high that can be routed to the $\overline{INT}$ pin for external monitoring.

(2) PWRCON is shown enabled and active high.

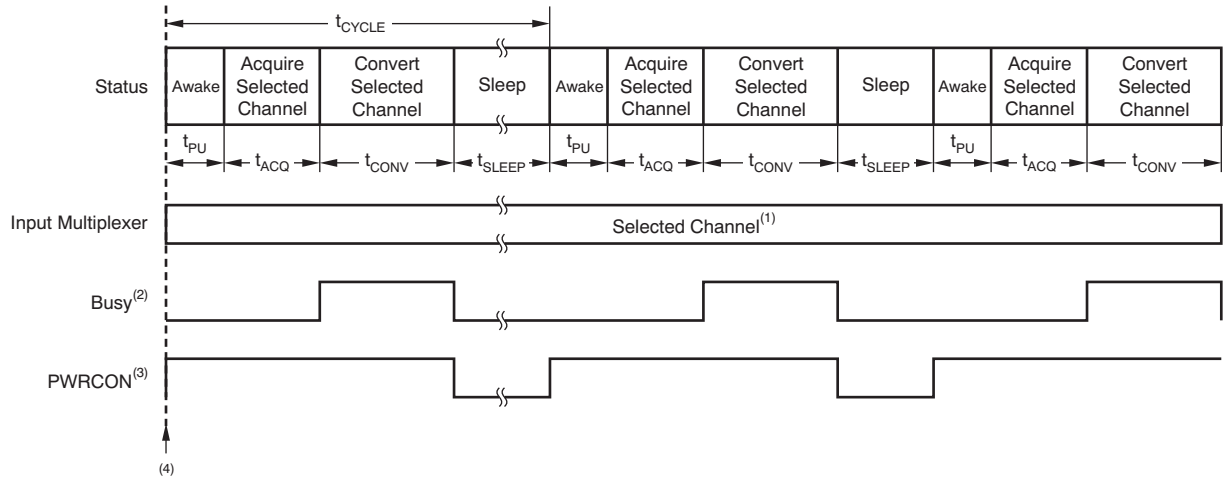
(3) The mode begins on the trailing edge of the I^2C acknowledge after writing to the MODECNTL register.

Figure 25. Auto-Scan Operation Example

7.4.1.7 Auto-Single With Sleep Mode

This mode automatically converts the selected channel repeatedly with a sleep interval between conversions, as shown in Figure 26. After the ADC Mode Control register is written, the power-up time (t_{PU}) is allowed to elapse. This value can be set to '0' to effectively bypass if not needed. Before the conversion, an acquisition time (t_{ACQ}) is allowed to elapse. t_{ACQ} time is programmable through the ACQCONFIG register, bits[4:0]. After the conversion, sleep time (t_{SLEEP}) is allowed to elapse and then the cycle repeats. The length of the sleep time is controlled by register bits. During the sleep mode, power dissipation is minimal and the PWRCON output is always disabled.

This mode can be used with the onboard digital comparator to periodically monitor the status of an input signal while saving power between conversions. Little support is needed from a host microcontroller. It is suggested to stop this mode by setting the mode to Idle or stopping the conversion by configuring the alarm to do so, before retrieving data. The length in time of the cycle (t_{CYCLE}) sets the average power dissipation, as shown in Figure 3 or Figure 4.



(1) Same channel is continuously converted.

(2) Busy is an internal signal shown as active high that can be routed to the $\overline{INT}$ pin for external monitoring.

(3) PWRCON is shown enabled and active high.

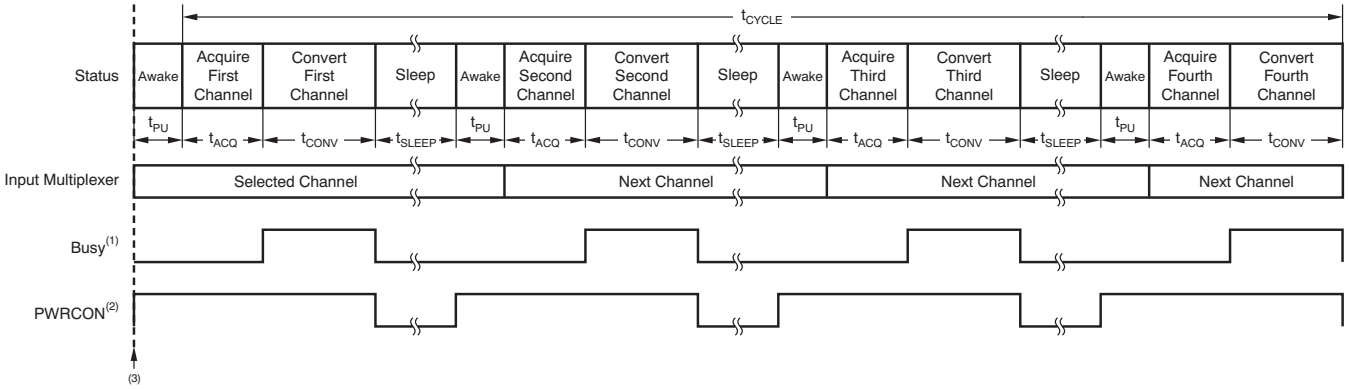
(4) The mode begins on the trailing edge of the I^2C acknowledge after writing to the MODECNTL register.

Figure 26. Auto-Single With Sleep Operation Example

7.4.1.8 Auto-Scan With Sleep Mode

This mode automatically converts all the channels repeatedly with a sleep interval between conversions, as illustrated in Figure 27. After the ADC Mode Control register is written, the power-up time (t_{PU}) is allowed to elapse. This value can be set to '0' to effectively bypass if not needed. Before the first conversion of the selected input, an acquisition time (t_{ACQ}) is allowed to elapse. t_{ACQ} time is programmable through the ACQCONFIG register, bits[4:0]. After the conversion, a sleep time (t_{SLEEP}) is allowed to elapse and then the cycle repeats. The length of the sleep time is controlled by register bits. During the sleep mode, power dissipation is minimal and the PWRCON output is always disabled. The input multiplexer is automatically incremented as the conversions complete. If, for example, the initial selected channel is CH2, the conversion order is CH2, CH3, CH0, CH1, CH2, CH3, and so forth until the mode is stopped. Data from the conversions are always put into the data register that corresponds to a particular channel. For example, CH2 data always goes in register DATA2_H and DATA2_L regardless of conversion order.

This mode can be used with the onboard digital comparator to periodically monitor the status of the input signals while saving power between conversions. Little support is needed from a host microcontroller. TI suggests stopping this mode by setting it to Idle or stopping the conversion by configuring the alarm to do so, before retrieving data. The length in time of the cycle (t_{CYCLE}) sets the average power dissipation, as shown in Figure 3 or Figure 4.



(1) Busy is an internal signal shown as active high that can be routed to the $\overline{INT}$ pin for external monitoring.

(2) PWRCON is shown enabled and active high.

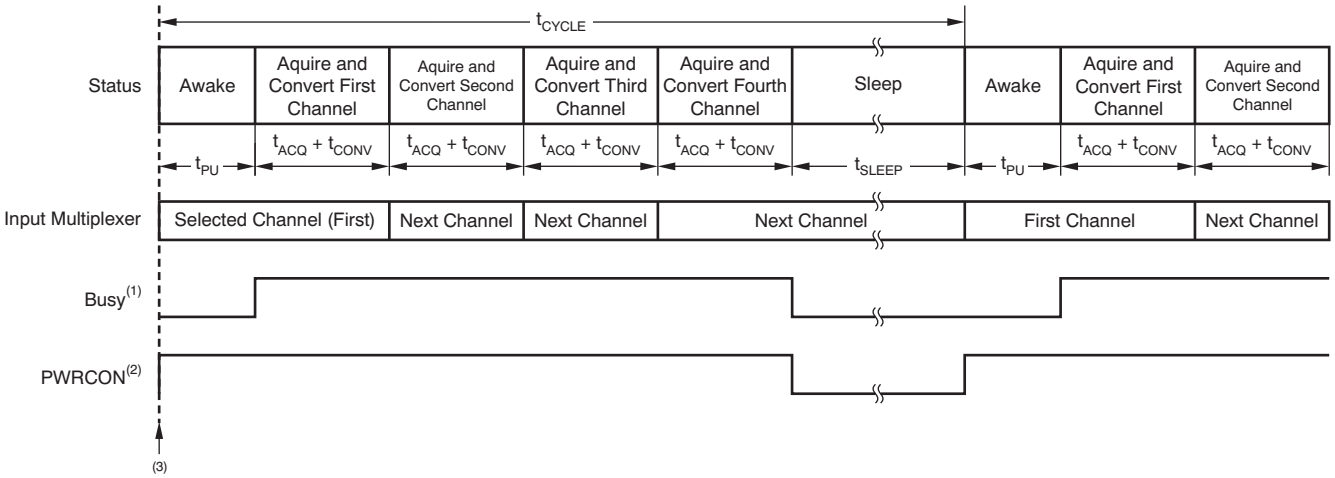
(3) The mode begins on the trailing edge of the I^2C acknowledge after writing to the MODECNTL register.

Figure 27. Auto-Scan With Sleep Operation Example

7.4.1.9 Auto-Burst Scan With Sleep Mode

This mode automatically converts all the channels without delay followed by a sleep interval before the cycle repeats, as shown in Figure 28. After the ADC Mode Control register is written, the power-up time (t_{PU}) is allowed to elapse. This value can be set to '0' to effectively bypass if not needed. Before the first conversion of the selected input, an acquisition time (t_{ACQ}) is allowed to elapse. t_{ACQ} time is programmable through the ACQCONFIG register, bits[4:0]. Afterwards, all four inputs are measured without delay. The input multiplexer is automatically incremented as the conversions complete. If, for example, the initial selected channel is CH2, the conversion order is CH2, CH3, CH0, and CH1. After the four conversions, a sleep time (t_{SLEEP}) is allowed to elapse and then the cycle repeats. The length of the sleep time is controlled by register bits. During the sleep mode, power dissipation is minimal and the PWRCON output is always disabled. Data from the conversions are always put into the data register that corresponds to a particular channel. For example, CH2 data always goes in register DATA2_H and DATA2_L regardless of conversion order.

This mode can be used with the onboard digital comparator to periodically monitor the status of the input signals while saving power between conversions. Little support is needed from a host microcontroller. TI suggests interrupting this mode and stop the automatic conversions, either by setting the mode to Idle or configuring the alarm to do so, before retrieving data. The length in time of the cycle (t_{CYCLE}) sets the average power, as shown in Figure 3 or Figure 4.



(1) Busy is an internal signal shown as active high that can be routed to the $\overline{INT}$ pin for external monitoring.

(2) PWRCON is shown enabled and active high.

(3) The mode begins on the trailing edge of the I²C acknowledge after writing to the MODECNTL register.

Figure 28. Auto-Burst Scan With Sleep Operation Example

7.5 Programming

7.5.1 I²C Interface

The ADS7924 communicates through an I²C interface. I²C is a two-wire, open-drain interface that supports multiple devices and masters on a single bus. Devices on the I²C bus only drive the bus lines low by connecting them to ground; they never drive the bus lines high. Instead, the bus wires are pulled high by pullup resistors, so the bus wires are high when no device is driving them low. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I²C bus always takes place between two devices, one acting as the master and the other as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I²C devices can act as masters or slaves, but the ADS7924 can only act as a slave device.

An I²C bus consists of two lines, SDA and SCL. SDA carries data; SCL provides the clock. All data are transmitted across the I²C bus in groups of eight bits. To send a bit on the I²C bus, the SDA line is driven to the appropriate level while SCL is low (a low on SDA indicates the bit is zero; a high indicates the bit is one). Once the SDA line settles, the SCL line is brought high, then low. This pulse on SCL clocks the SDA bit into the receiver shift register. If the I²C bus is held idle for more than 25 ms, the bus times out.

The I²C bus is bidirectional: the SDA line is used for both transmitting and receiving data. When the master reads from a slave, the slave drives the data line; when the master sends to a slave, the master drives the data line. The master always drives the clock line. The ADS7924 never drives SCL, because it cannot act as a master. On the ADS7924, SCL is an input only.

Most of the time the bus is idle; no communication occurs, and both lines are high. When communication is taking place, the bus is active. Only master devices can start a communication and initiate a START condition on the bus. Normally, the data line is only allowed to change state while the clock line is low. If the data line changes state while the clock line is high, it is either a START condition or a STOP condition. A START condition occurs when the clock line is high and the data line goes from high to low. A STOP condition occurs when the clock line is high and the data line goes from low to high.

After the master issues a START condition, it sends a byte that indicates which slave device it wants to communicate with. This byte is called the *address byte*. Each device on an I²C bus has a unique 7-bit address to which it responds. The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Programming (continued)

Every byte transmitted on the I^2C bus, whether it is address or data, is acknowledged with an *acknowledge* bit. When the master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA low. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when the master has finished reading a byte, it pulls SDA low to acknowledge this to the slave. It then sends a clock pulse to clock the bit. (The master always drives the clock line.)

A *not-acknowledge* is performed by simply leaving SDA high during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it receives a not-acknowledge because no device is present at that address to pull the line low.

When the master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. The master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

See the *Figure 1* section for a timing diagram showing the ADS7924 I^2C transaction.

7.5.2 I^2C Address Selection

The ADS7924 has one address pin, A0, that sets the I^2C address. This pin can be connected to ground or VDD, allowing two addresses to be selected with one pin as shown in Table 2. The state of the address pin A0 is sampled continuously.

Table 2. A0 Pin Connection and Corresponding Slave Address

A0 PIN	SLAVE ADDRESS
Ground	1001000
DVDD	1001001

7.5.3 I^2C Speed Modes

The ADS7924 supports the I^2C standard and fast modes. Standard mode allows a clock frequency of up to 100 kHz and fast mode permits a clock frequency of up to 400 kHz.

7.5.4 Slave Mode Operations

The ADS7924 can act as either slave receivers or slave transmitters. As a slave device, the ADS7924 cannot drive the SCL line.

7.5.4.1 Receive Mode

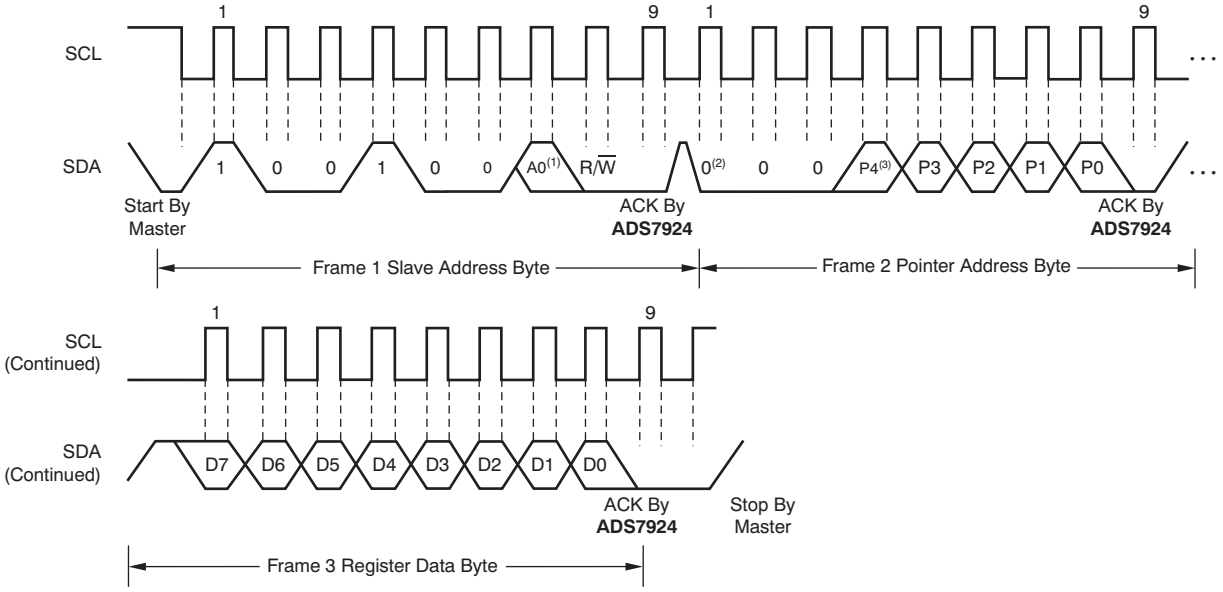
In slave receive mode, the first byte transmitted from the master to the slave is the address with the R/$\overline{W}$ bit low. This byte allows the slave to be written to. The next byte transmitted by the master is the register pointer byte. The ADS7924 then acknowledges receipt of the register pointer byte. The next two bytes are written to the address given by the register pointer. The ADS7924 acknowledges each byte sent. Register bytes are sent with the most significant byte first, followed by the least significant byte.

7.5.4.2 Transmit Mode:

In slave transmit mode, the first byte transmitted by the master is the 7-bit slave address followed by the high R/$\overline{W}$ bit. This byte places the slave into transmit mode and indicates that the ADS7924 is being read from. The next byte transmitted by the slave is the most significant byte of the register that is indicated by the register pointer. This byte is followed by an acknowledgment from the master. The remaining least significant byte is then sent by the slave and is followed by an acknowledgment from the master. The master may terminate transmission after any byte by not acknowledging or issuing a START or STOP condition.

7.5.5 Writing the Registers

To access a write register from the ADS7924, the master must first write the appropriate value to the Pointer address. The Pointer address is written directly after the slave address byte, low R/$\overline{W}$ bit, and a successful slave acknowledgment. After the Pointer address is written, the slave acknowledges and the master issues a STOP or a repeated START condition. The MSB of the pointer address is the increment (INC) bit. When set to '1', the register address is automatically incremented after every register write which allows convenient writing of multiple registers. Set INC to '0' when writing a single register. Figure 29 and Figure 30 show timing examples.

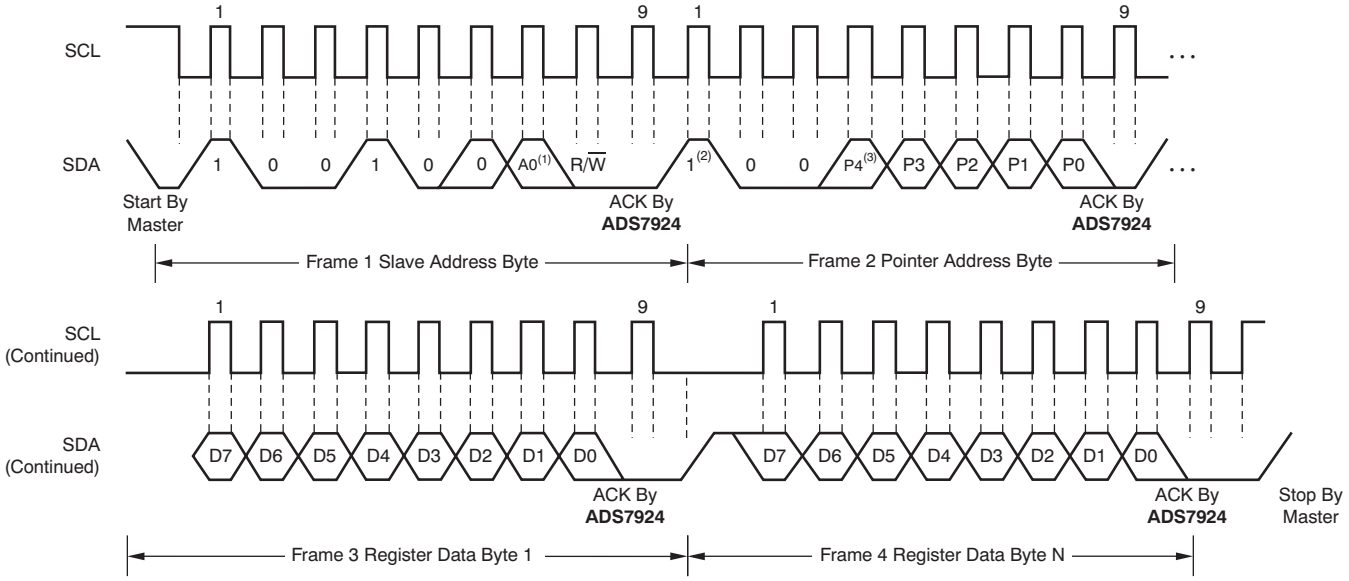


(1) The value of A0 is determined by the A0 pin.

(2) When INC is set to '0', the address pointer remains unchanged after a read.

(3) Bits P[4:0] point to the register to be written.

Figure 29. Writing a Single Register Timing Diagram



(1) The value of A0 is determined by the A0 pin.

(2) When INC is set to '1', the address pointer automatically increments for multiple register writes.

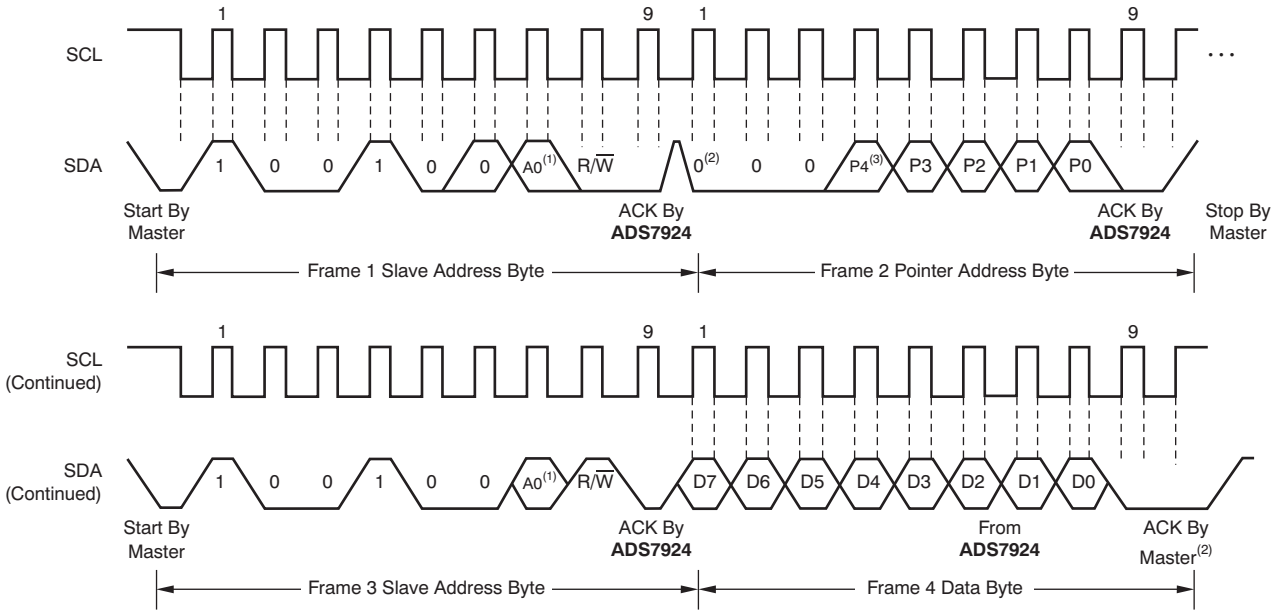
(3) Bits P[4:0] point to the storing register to be written.

Figure 30. Writing Multiple Registers Timing Diagram

7.5.6 Reading the Registers

To read a specific register from the ADS7924, the master must first write the appropriate value to the pointer address. The pointer address is written directly after the slave address byte, low R/$\overline{W}$ bit, and a successful slave acknowledgment. The MSB of the pointer address is the INC bit. When set to '1', the register address is automatically incremented after every register read which allows convenient reading of multiple registers. Set INC to '0' when reading a single register.

The master may issue a START condition and send the slave address byte with the R/$\overline{W}$ bit high to begin the read. If the previously selected register is to be read again, then updating the pointer address is unnecessary. Figure 31 to Figure 33 show examples of register reads.

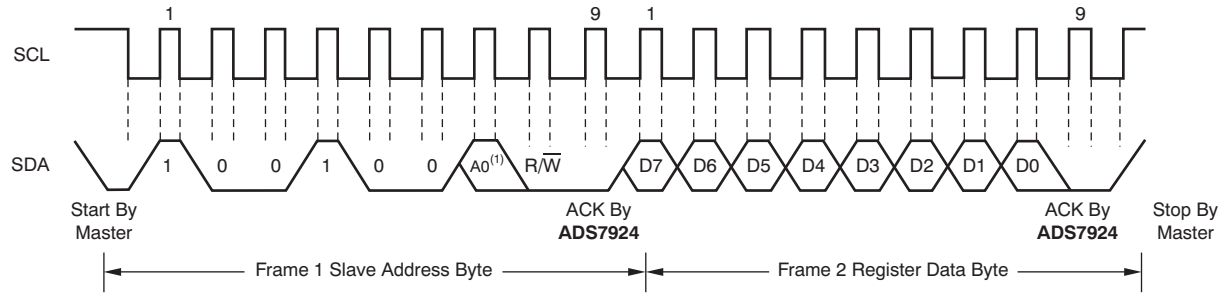


(1) The value of A0 is determined by the A0 pin.

(2) When INC is set to '0', the address pointer remains unchanged after a read.

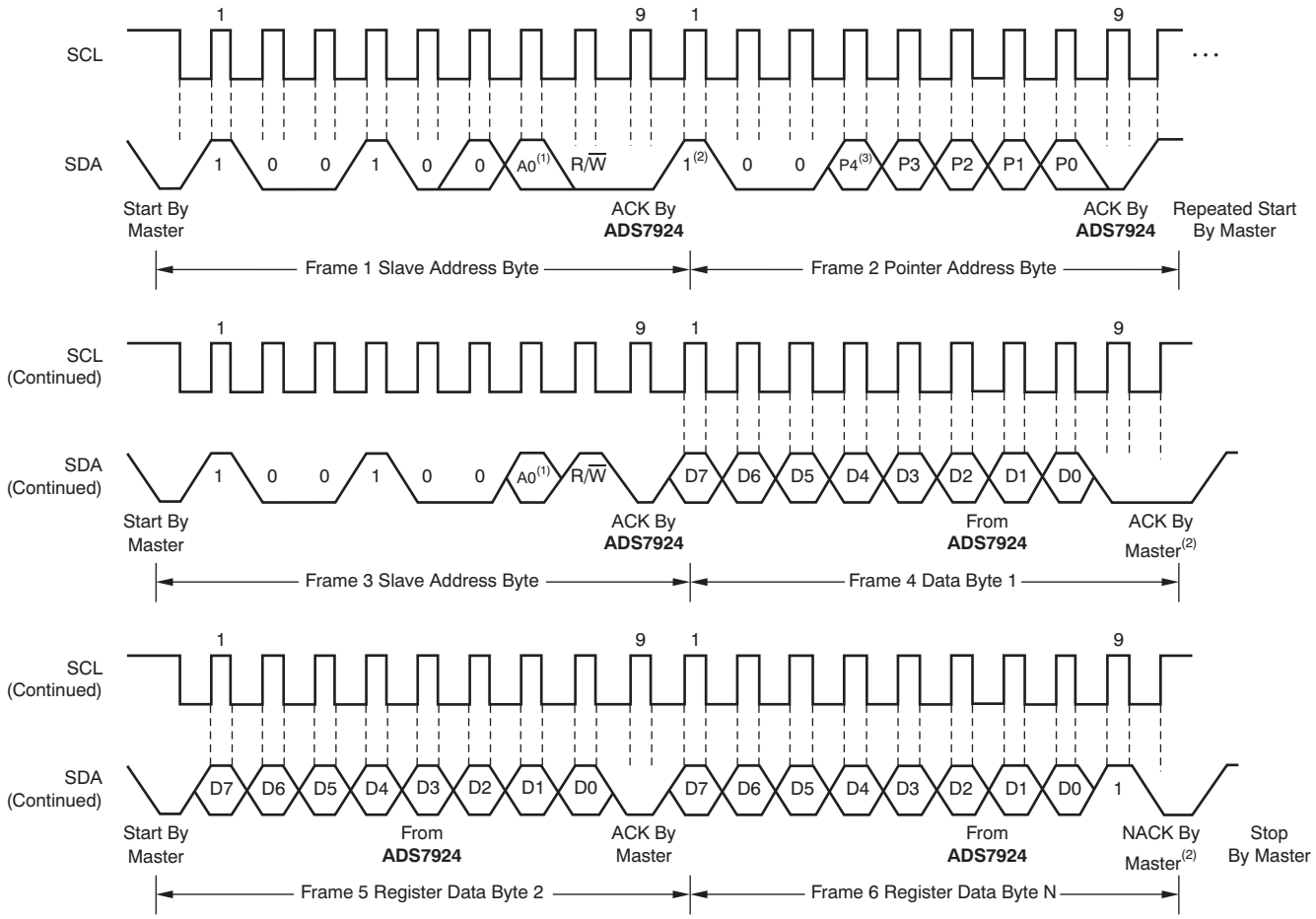
(3) Bits P[4:0] point to the register to be read.

Figure 31. Reading a Single Register Timing Diagram



(1) The value of A0 is determined by the A0 pin.

Figure 32. Reading a Previously Addressed Register Timing Diagram



(1) The value of A0 is determined by the A0 pin.

(2) When INC is set to '1', the address pointer automatically increments for multiple register reads.

(3) Bits P[4:0] point to the register to be read.

Figure 33. Reading Multiple Registers Timing Diagram

7.6 Register Map

The ADS7924 operation is controlled through a set of registers. Collectively, the registers contain all the information needed to configure the part. Table 3 shows the register map.

Table 3. Register Map

ADDRESS	REGISTER	RESET VALUE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	MODECNTRL	00h	MODE5	MODE4	MODE3	MODE2	MODE1	MODE0	SEL/ID1	SEL/ID0
01h	INTCNTRL	X0h	ALRM_ST3	ALRM_ST2	ALRM_ST1	ALRM_ST0	AEN/ST3	AEN/ST2	AEN/ST1	AEN/ST0
02h	DATA0_U	XXh	DATA0[11]	DATA0[10]	DATA0[9]	DATA0[8]	DATA0[7]	DATA0[6]	DATA0[5]	DATA0[4]
03h	DATA0_L	XXh	DATA0[3]	DATA0[2]	DATA0[1]	DATA0[0]	0	0	0	0
04h	DATA1_U	XXh	DATA1[11]	DATA1[10]	DATA1[9]	DATA1[8]	DATA1[7]	DATA1[6]	DATA1[5]	DATA1[4]
05h	DATA1_L	XXh	DATA1[3]	DATA1[2]	DATA1[1]	DATA1[0]	0	0	0	0
06h	DATA2_U	XXh	DATA2[11]	DATA2[10]	DATA2[9]	DATA2[8]	DATA2[7]	DATA2[6]	DATA2[5]	DATA2[4]
07h	DATA2_L	XXh	DATA2[3]	DATA2[2]	DATA2[1]	DATA2[0]	0	0	0	0
08h	DATA3_U	XXh	DATA3[11]	DATA3[10]	DATA3[9]	DATA3[8]	DATA3[7]	DATA3[6]	DATA3[5]	DATA3[4]
09h	DATA3_L	XXh	DATA3[3]	DATA3[2]	DATA3[1]	DATA3[0]	0	0	0	0
0Ah	ULR0	XXh	ULR0[7]	ULR0[6]	ULR0[5]	ULR0[4]	ULR0[3]	ULR0[2]	ULR0[1]	ULR0[0]
0Bh	LLR0	XXh	LLR0[7]	LLR0[6]	LLR0[5]	LLR0[4]	LLR0[3]	LLR0[2]	LLR0[1]	LLR0[0]
0Ch	ULR1	XXh	ULR1[7]	ULR1[6]	ULR1[5]	ULR1[4]	ULR1[3]	ULR1[2]	ULR1[1]	ULR1[0]
0Dh	LLR1	XXh	LLR1[7]	LLR1[6]	LLR1[5]	LLR1[4]	LLR1[3]	LLR1[2]	LLR1[1]	LLR1[0]
0Eh	ULR2	XXh	ULR2[7]	ULR2[6]	ULR2[5]	ULR2[4]	ULR2[3]	ULR2[2]	ULR2[1]	ULR2[0]
0Fh	LLR2	XXh	LLR2[7]	LLR2[6]	LLR2[5]	LLR2[4]	LLR2[3]	LLR2[2]	LLR2[1]	LLR2[0]
10h	ULR3	XXh	ULR3[7]	ULR3[6]	ULR3[5]	ULR3[4]	ULR3[3]	ULR3[2]	ULR3[1]	ULR3[0]
11h	LLR3	XXh	LLR3[7]	LLR3[6]	LLR3[5]	LLR3[4]	LLR3[3]	LLR3[2]	LLR3[1]	LLR3[0]
12h	INTCONFIG	E0h	AIMCNT2	AIMCNT1	AIMCNT0	INTCNFG1	INTCNFG0	BUSY/$\overline{\text{INT}}$	INTPOL	INTTRIG
13h	SLPCONFIG	00h	0	CONVCTRL	SLPDIV4	SLPMULT8	0	SLPTIME2	SLPTIME1	SLPTIME0
14h	ACQCONFIG	00h	0	0	0	ACQTIME4	ACQTIME3	ACQTIME2	ACQTIME1	ACQTIME0
15h	PWRCONFIG	00h	CALCNTL	PWRCONPOL	PWRCONEN	PWRUPTIME4	PWRUPTIME3	PWRUPTIME2	PWRUPTIME1	PWRUPTIME0
16h	RESET	18h (A0 = 0) 19h (A0 = 1)	RST/ID7	RST/ID6	RST/ID5	RST/ID4	RST/ID3	RST/ID2	RST/ID1	RST/ID0

Figure 34. MODECNTRL: ADC Mode Control Register (Address = 00h)

7	6	5	4	3	2	1	0
MODE5	MODE4	MODE3	MODE2	MODE1	MODE0	SEL/ID1	SEL/ID0

Bits[7:2] **MODE[5:0]: Mode control**

000000 = Idle mode (default)
100000 = Awake mode
110000 = Manual-Single mode
110010 = Manual-Scan mode
110001 = Auto-Single mode
110011 = Auto-Scan mode
111001 = Auto-Single with Sleep mode
111011 = Auto-Scan with Sleep mode
111111 = Auto-Burst Scan with Sleep mode

Bits[1:0] **SEL/ID[1:0]: Channel selection**

When read, these bits indicate the last channel converted.
When writing to these bits, select which input appears on MUXOUT:
00 = Channel 0 is selected
01 = Channel 1 is selected
10 = Channel 2 is selected
11 = Channel 3 is selected (unless the CALCNTRL bit is set to '1')

Figure 35. INTCNTRL: Interrupt Control Register (Address = 01h)

7	6	5	4	3	2	1	0
ALRM_ST3	ALRM_ST2	ALRM_ST1	ALRM_ST0	AEN/ST3	AEN/ST2	AEN/ST1	AEN/ST0

Bits[7:4] **ALRM_ST[3:0]: Alarm status (read-only)**

Reading these bits indicates the alarm status for the channels. These bits are never masked—they always report the alarm status even when the alarm is not enabled by the corresponding AEN/ST bits.
Bit 7 = Channel 3 alarm status, '1' indicates an alarm condition
Bit 6 = Channel 2 alarm status, '1' indicates an alarm condition
Bit 5 = Channel 1 alarm status, '1' indicates an alarm condition
Bit 4 = Channel 0 alarm status, '1' indicates an alarm condition

Bits[3:0] **AEN/ST[3:0]: Alarm enable**

Writing to these bits enables the alarm for the corresponding channel.
Reading these bits returns the status of the alarm for the corresponding channel when enabled. Reading returns a '0' when the alarm in not enabled.
Bit 3 = Channel 3 alarm enable, 1 = enabled (default = 0)
Bit 2 = Channel 2 alarm enable, 1 = enabled (default = 0)
Bit 1 = Channel 1 alarm enable, 1 = enabled (default = 0)
Bit 0 = Channel 0 alarm enable, 1 = enabled (default = 0)

Each input channel has individual registers to buffer the conversion data. The 12 bits are stored in two registers: the upper register stores the eight most significant bits; the lower register stores the lower four least significant bits. The data registers are always updated with the corresponding input channel regardless of the order of conversion. For example, DATA0_U and DATA0_L always contain the results of the latest conversion of CH0.

Figure 36. DATA0_U: Conversion Data for Channel 0, Upper Bits Register (Address = 02h)

7	6	5	4	3	2	1	0
DATA0[11] (MSB)	DATA0[10]	DATA0[9]	DATA0[8]	DATA0[7]	DATA0[6]	DATA0[5]	DATA0[4]

Figure 37. DATA0_L: Conversion Data for Channel 0, Lower Bits Register (Address = 03h)

7	6	5	4	3	2	1	0
DATA0[3]	DATA0[2]	DATA0[1]	DATA0[0] (LSB)	0	0	0	0

Figure 38. DATA1_U: Conversion Data for Channel 1, Upper Bits Register (Address = 04h)

7	6	5	4	3	2	1	0
DATA1[11] (MSB)	DATA1[10]	DATA1[9]	DATA1[8]	DATA1[7]	DATA1[6]	DATA1[5]	DATA1[4]

Figure 39. DATA1_L: Conversion Data for Channel 1, Lower Bits Register (Address = 05h)

7	6	5	4	3	2	1	0
DATA1[3]	DATA1[2]	DATA1[1]	DATA1[0] (LSB)	0	0	0	0

Figure 40. DATA2_U: Conversion Data for Channel 2, Upper Bits Register (Address = 06h)

7	6	5	4	3	2	1	0
DATA2[11] (MSB)	DATA2[10]	DATA2[9]	DATA2[8]	DATA2[7]	DATA2[6]	DATA2[5]	DATA2[4]

Figure 41. DATA2_L: Conversion Data for Channel 2, Lower Bits Register (Address = 07h)

7	6	5	4	3	2	1	0
DATA2[3]	DATA2[2]	DATA2[1]	DATA2[0] (LSB)	0	0	0	0

Figure 42. DATA3_U: Conversion Data for Channel 3, Upper Bits Register (Address = 08h)

7	6	5	4	3	2	1	0
DATA3[11] (MSB)	DATA3[10]	DATA3[9]	DATA3[8]	DATA3[7]	DATA3[6]	DATA3[5]	DATA3[4]

Figure 43. DATA3_L: Conversion Data for Channel 3, Lower Bits Register (Address = 09h)

7	6	5	4	3	2	1	0
DATA3[3]	DATA3[2]	DATA3[1]	DATA3[0] (LSB)	0	0	0	0

Input channel has individual upper and lower threshold registers. Each register is eight bits with the least significant bit weight equal to AVDD/256. The comparator is tripped when the input signal exceeds the value of the upper limit register or falls below the lower limit register.

Figure 44. ULR0: Upper Limit Threshold for Channel 0 Comparator Register (Address = 0ah)

7	6	5	4	3	2	1	0
ULR0[7] (MSB)	ULR0[6]	ULR0[5]	ULR0[4]	ULR0[3]	ULR0[2]	ULR0[1]	ULR0[0] (LSB)

Figure 45. LLR0: Lower Limit Threshold for Channel 0 Comparator Register (Address = 0bh)

7	6	5	4	3	2	1	0
LLR0[7] (MSB)	LLR0[6]	LLR0[5]	LLR0[4]	LLR0[3]	LLR0[2]	LLR0[1]	LLR0[0] (LSB)

Figure 46. ULR1: Upper Limit Threshold for Channel 1 Comparator Register (Address = 0ch)

7	6	5	4	3	2	1	0
ULR1[7] (MSB)	ULR1[6]	ULR1[5]	ULR1[4]	ULR1[3]	ULR1[2]	ULR1[1]	ULR1[0] (LSB)

Figure 47. LLR1: Lower Limit Threshold for Channel 1 Comparator Register (Address = 0dh)

7	6	5	4	3	2	1	0
LLR1[7] (MSB)	LLR1[6]	LLR1[5]	LLR1[4]	LLR1[3]	LLR1[2]	LLR1[1]	LLR0[0] (LSB)

Figure 48. ULR2: Upper Limit Threshold for Channel 2 Comparator Register (Address = 0eh)

7	6	5	4	3	2	1	0
ULR2[7] (MSB)	ULR2[6]	ULR2[5]	ULR2[4]	ULR2[3]	ULR2[2]	ULR2[1]	ULR2[0] (LSB)

Figure 49. LLR2: Lower Limit Threshold for Channel 2 Comparator Register (Address = 0fh)

7	6	5	4	3	2	1	0
LLR2[7] (MSB)	LLR2[6]	LLR2[5]	LLR2[4]	LLR2[3]	LLR2[2]	LLR2[1]	LLR2[0] (LSB)

Figure 50. ULR3: Upper Limit Threshold for Channel 3 Comparator Register (Address = 10h)

7	6	5	4	3	2	1	0
ULR3[7] (MSB)	ULR3[6]	ULR3[5]	ULR3[4]	ULR3[3]	ULR3[2]	ULR3[1]	ULR3[0] (LSB)

Figure 51. LLR3: Lower Limit Threshold for Channel 3 Comparator Register (Address = 11h)

7	6	5	4	3	2	1	0
LLR3[7] (MSB)	LLR3[6]	LLR3[5]	LLR3[4]	LLR3[3]	LLR3[2]	LLR3[1]	LLR3[0] (LSB)

Figure 52. INTCONFIG: Interrupt Configuration Register (Address = 12h)

7	6	5	4	3	2	1	0
ALMCNT2	ALMCNT1	ALMCNT0	INTCNFG2	INTCNFG1	INTCNFG0	INTPOL	INTTRIG

Bits[7:5] **ALMCNT[2:0]: Alarm count**

These bits set the number of times the comparator threshold limit (either upper or lower) must be exceeded to generate an alarm.
000 = Every conversion generates an alarm
010 = Exceeding the threshold limit 1 time generates an alarm condition
100 = Exceeding the threshold limit 2 times generates an alarm condition
110 = Exceeding the threshold limit 3 times generates an alarm condition
111 = Exceeding the threshold limit 4 times generates an alarm condition
101 = Exceeding the threshold limit 5 times generates an alarm condition
110 = Exceeding the threshold limit 6 times generates an alarm condition
111 = Exceeding the threshold limit 7 times generates an alarm condition

Bits[4:2] **INTCNFG[2:0]: $\overline{\text{INT}}$ output pin configuration**

These bits determine which signal is output on $\overline{\text{INT}}$. They also select the conversion control event; see the CONVCTRL bit in the SLPCONFIG register. The configuration of these bits is shown in Table 4.

Table 4. $\overline{\text{INT}}$ Pin Configuration

BIT SETTING	$\overline{\text{INT}}$ PIN CONFIGURATION	CONVERSION CONTROL EVENT
000	Alarm	Alarm
001	Busy	Alarm
010	Data ready: one conversion completed	Data ready: one conversion complete
011	Busy	Data ready: one conversion complete
100	Do not use	—
101	Do not use	—
110	Data ready: all four conversions complete	Data ready: four conversions complete
111	Busy	Data ready: four conversions complete

Bit 1 **INTPOL: $\overline{\text{INT}}$ pin polarity**

0 = Active low (default)
1 = Active high

Bit 0 **INTTRIG: $\overline{\text{INT}}$ output pin signaling**

0 = Static signal for use with level triggering (default)
1 = Pulse signal for use with edge triggering

Figure 53. SLPCONFIG: Sleep Configuration Register (Address = 13h)

7	6	5	4	3	2	1	0
0	CONVCTRL	SLPDIV4	SLPMULT8	0	SLPTIME2	SLPTIME1	SLPTIME0

Bit 7 **Always write '0'**

Bit 6 **CONVCTRL: Conversion control**

This bit determines the conversion status after a conversion control event; see the INTCNFG bits in the INTCONFIG register.
0 = Conversions continue, independent of the control event status (default)
1 = Conversions are stopped as soon as a control event occurs; the event must be cleared to resume conversions

Bit 5 **SLPDIV4: Sleep time 4x divider**

This bit sets the speed of the sleep clock.
0 = Sleep time divider is '1' (default)
1 = Sleep time divider is '4'

Bit 4 **SLPMULT8: Sleep time 8x multiplier**

0 = Sleep time multiplier is '1' (default)
1 = Sleep time multiplier is '8'

Bit 3 **Always write '0'**

Bits[2:0] **SLPTIME[2:0]: Sleep time setting**

000 = 2.5 ms (default)
001 = 5 ms
010 = 10 ms
011 = 20 ms
100 = 40 ms
101 = 80 ms
110 = 160 ms
111 = 320 ms

Figure 54. ACQCONFIG: Acquire Configuration Register (Address = 14h)

7	6	5	4	3	2	1	0
0	0	0	ACQTIME4	ACQTIME3	ACQTIME2	ACQTIME1	ACQTIME0

Bits[7:5] **Always write '0'**

Bits[4:0] **ACQTIME[4:0]: Signal acquire time**

These bits set the time to acquire the signal before a conversion (default = 0).
t_{ACQ} = ACQTIME[4:0] × 2 µs + 6 µs

Figure 55. PWRCONFIG: Power-Up Configuration Register (Address = 15h)

7	6	5	4	3	2	1	0
CALCNTL	PWRCONPOL	PWRCONEN	PWRUPTIME4	PWRUPTIME3	PWRUPTIME2	PWRUPTIME1	PWRUPTIME0

Bit 7 **CALCNTL: Calibration control**

0 = Setting CH3 in the Mode Control register selects the CH3 input to be routed to the MUXOUT pin. (default)
1 = Setting CH3 in the Mode Control register connects the MUXOUT pin to AGND.

Bit 6 **PWRCONPOL: PWRCON pin polarity**

0 = Active low (default)
1 = Active high

Bit 5 **PWRCONEN: PWRCON enable**

0 = The PWRCON pin is disabled (default)
1 = The PWRCON pin is always enabled

Bits[4:0] **PWRUPTIME[4:0]: Power-up time setting**

These bits set the power-up time (default = 0).
t_{PWR} = PWRUPTIME[4:0] × 2 µs.

Figure 56. Reset: Software Reset And Device Id Register (Address = 16h)

7	6	5	4	3	2	1	0
RST/ID7	RST/ID6	RST/ID5	RST/ID4	RST/ID3	RST/ID2	RST/ID1	RST/ID0

A read of this register returns the device ID when A0 determines the last bit of the device ID (0001100A0).
A write to this register of 10101010 generates a software reset of the ADS7924.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ADS7924 device provides a break-out point in the signal path between the multiplexer output and the ADC input for external signal conditioning, if desired. Typical uses include adding an operational amplifier, such as the TLV2780, along with an RC filter circuit. Different application circuits are described in following sections.

8.1.1 Using an Operational Amplifier Between Multiplexer Output and ADC Input

Adding an operational amplifier provides a high input impedance to the sensor source and buffers the capacitive ADC input from high-impedance sensor circuits, as shown in Figure 57. High-impedance input signals can be momentarily disrupted when coupled directly to a capacitive input like that of a sampling ADC. This disruption can create errors when sampling. The use of an operational amplifier is recommended in these cases.

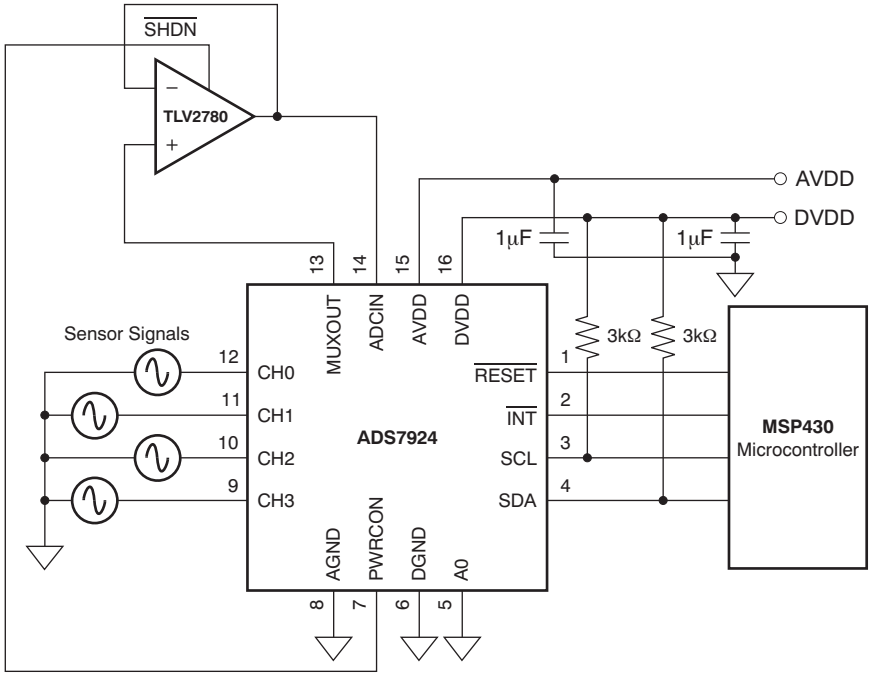


Figure 57. Sensor Data Acquisition With TLV2780 Buffer Amplifier

8.1.2 Using an Operational Amplifier and RC Filter Between Multiplexer Output and ADC Input

Placing an RC low-pass filter in the signal path allows for filtering out noise. The RC component values should allow for sufficient settling time when changing from channel to channel. The time required for a full-scale input signal to settle to within 1LSB of a 12-bit ADC is given by Equation 3:

$$\text{Settling Time} = R \times C \times \ln(2^{12}) \quad (3)$$

R_X and C form a low-pass filter for removing sensor and noise from other sources at the operational amplifier input pin. The low-pass bandwidth is given by Equation 4:

$$f_{-3dB} = 1/(2\pi RC) \quad (4)$$

The f_{-3dB} should be chosen so that the signals of interest are within half of the programmable sampling frequency. The noise bandwidth is given by Equation 5:

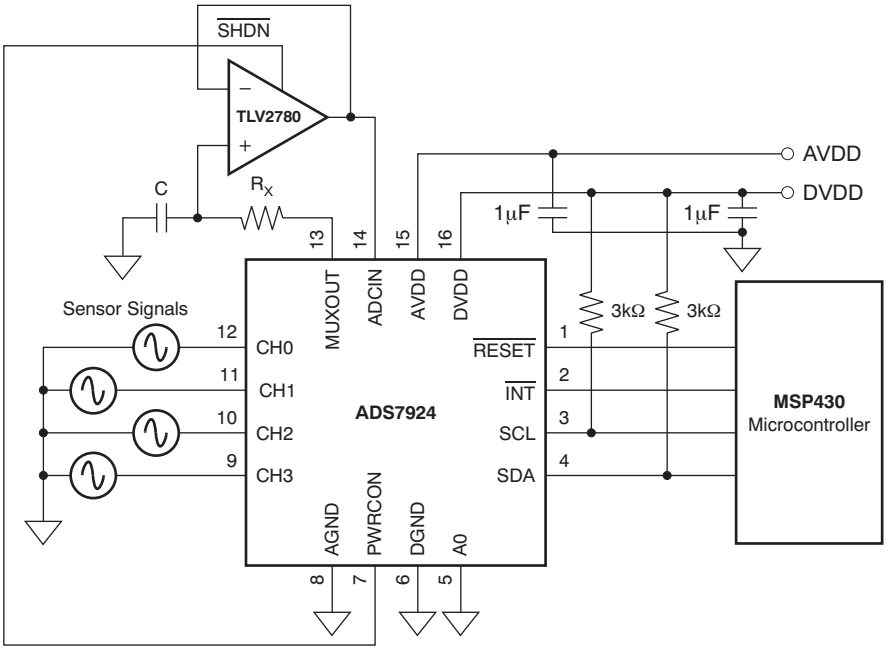
Application Information (continued)

$$f_{NB} = 1/(4RC) \quad (5)$$

This term should be set to reduce noise bandwidth but still allow for enough settling time. The ADS7924 has internal registers ACQCONFIG (address = 14h), PWRCONF (address = 15h), and SLPCONFIG (address = 13h) that can be programmed to slow down the channel-to-channel power up, acquisition, and sleep periods if needed to allow for a longer settling time requirement.

In Figure 58, *R* is the sum of the sensor output impedance R_{SENSOR}, the internal MUX resistance R_{MUX} (approximately 60 Ω), and external resistor R_X. The primary benefit of having the filter at the input of the operational amplifier is that the amplifier does not have to drive the filter, which can cause instability with large capacitor values that may be needed to filter noise to low levels.

The TLV2780 typically powers up from a shutdown state in 800 ns. This period is well within the ADS7924 minimum acquisition time of 6µs. Setting the PWRCONFIG register (address = 15h) allows for more time if another operational amplifier with a shutdown feature is used.



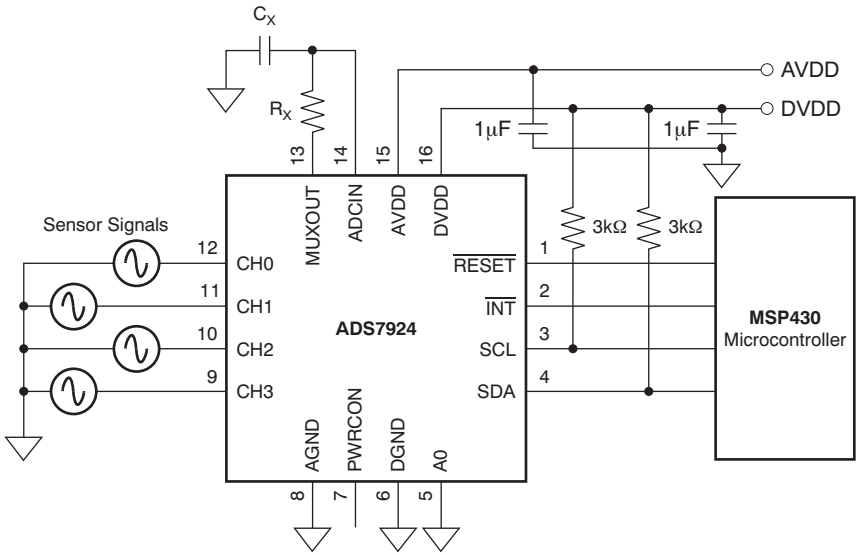
NOTE: f_{-3dB} BW = 159 kHz, R = 1 kΩ, and C = 1 nF where R = R_{MUX} + R_{SENSOR} + R_X.

Figure 58. Sensor Data Acquisition With Filter and TLV2780 Buffer Amplifier

Application Information (continued)

8.1.3 Using an RC Filter Between Multiplexer Output and ADC Input

For applications where low-output impedance signals are provided for the ADS7924 inputs, a simple RC filter may suffice, as shown in Figure 59.



NOTE: f_{-3dB} BW = 159 kHz, R = 1 kΩ, and C = 1 nF where $R = R_{MUX} + R_{SENSOR} + R_X$, $C = C_X + C_{ADCIN}$, R_{MUX} is approximately 60 Ω, and C_{ADCIN} is approximately 15 pF.

Figure 59. Sensor Data Acquisition With Filter Only

C_X should be greater than 200 pF, if possible. When coupled directly to the ADC input, using a capacitor with this value allows for faster settling when scanning between channels.

Application Information (continued)

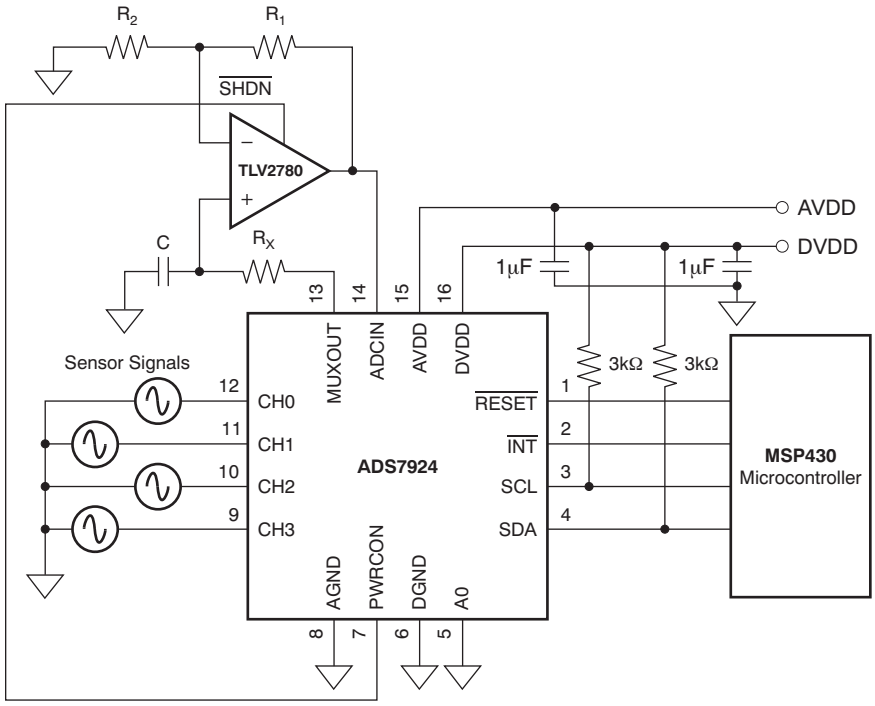
8.1.4 Operational Amplifier With Filter and Gain Option Between Multiplexer Output and ADC Input

Both filtering and gain are added in Figure 60. Gain is given by Equation 6:

$$\text{Gain} = 1 + R_1/R_2 \quad (6)$$

where

- R is the sum of the sensor output impedance R_{SENSOR}, the internal MUX resistance R_{MUX} (approximately 60 Ω), and the external resistor R_X.



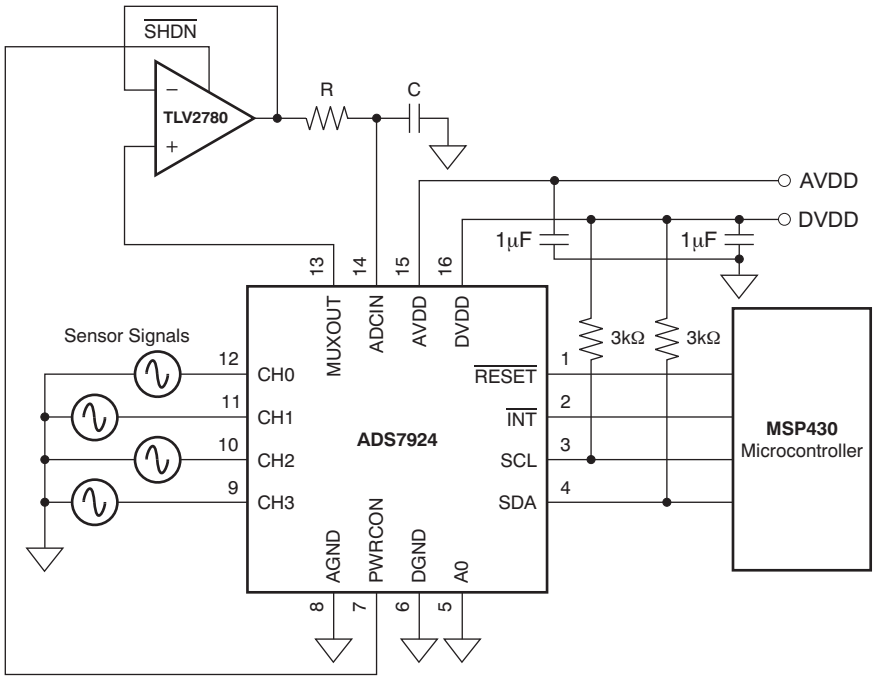
NOTE: f_{-3dB} BW = 159 kHz, R = 1 kΩ, and C = 1 nF where $R = R_{MUX} + R_{SENSOR} + R_X$, and R_{MUX} is approximately 60 Ω. Gain = $1 + R_1/R_2$.

Figure 60. Sensor Data Acquisition With Gain Set Resistors, Filter, and TLV2780 Buffer Amplifier

Application Information (continued)

8.1.5 Driving an RC Filter With an Operational Amplifier Between Multiplexer Output and ADC Input

A filter can be placed at the output of the operational amplifier, as shown in Figure 61. Ensure that the operational amplifier is capable of driving the RC filter circuit without the operational amplifier becoming unstable. One of the benefits of this circuit is that the operational amplifier noise is filtered along with sensor and other system noise right at the ADC input pin.



NOTE: C = 200 pF, R = 1 kΩ, and the capacitance at the ADCIN pin is approximately 15 pF.

Figure 61. Sensor Data Acquisition With an Operational Amplifier Driving an RC Filter

8.1.6 Average Power Consumption

With its fast conversion time and programmable sleep time with near-zero power, the ADS7924 allows periodic monitoring of the inputs with a very low average power dissipation, especially as the monitoring interval increases. The average current required can be calculated as the weighed average of the currents consumed during the power up, acquisition, converting, and sleep periods using Equation 7.

$$I_{AVERAGE} = \frac{I_{PU}t_{PU} + I_{ACQ}t_{ACQ} + I_{CONV}t_{CONV} + I_{SLEEP}t_{SLEEP}}{t_{CYCLE}} \quad (7)$$

As an example, calculate the average current in the following configuration:

- Mode programmed to Auto-Scan with Sleep
- Power-up time (t_{PU}) programmed to '0'
- Acquisition time (t_{ACQ}) programmed to 6 μs
- Sleep time (t_{SLEEP}) programmed to 2.5 ms
- AVDD = 2.2 V

Looking at Figure 27, the cycle time is seen to equal $t_{CYCLE} = 4t_{PU} + 4t_{ACQ} + 4t_{CONV} + 4t_{SLEEP} = 4(0) + 4(6\ \mu s) + 4(4\ \mu s) + 4(2.5\ ms) = 10.04$ ms.

Table 5 lists the supply current for different supply voltages and operating conditions. Using the data for 2.2 V with the calculated cycle time in Equation 7 gives the following average current:

$$I_{AVERAGE} = \frac{0 + (270\mu A)(4)(6\mu s) + (400\mu A)(4)(4\mu s) + (1.25\mu A)(4)(2.5ms)}{10.04ms} = 2.5\mu A \quad (8)$$

Application Information (continued)

Table 5. Supply Current for Various Operating Conditions

STATUS	AVDD			
	5 V	3.3 V	2.7 V	2.2 V
Idle	1 µA	1 µA	1 µA	1 µA
Awake	45 µA	25 µA	20 µA	15 µA
Acquiring	315 µA	285 µA	275 µA	270 µA
Converting	730 µA	520 µA	450 µA	400 µA
Sleeping	3 µA	2 µA	1.5 µA	1.25 µA

The acquisition, conversion, and sleep times are multiplied by 4 because these are repeated four times in one cycle when in auto-scan with sleep mode.

Average power dissipation for the previous configuration where all four inputs are monitored every 10 ms is (2.2 V)(2.5 µA) = 5.5 µW.

Figure 3 and Figure 4 plot Equation 7 to help illustrate the relationship between cycle time and average power dissipation.

8.2 Typical Application

Figure 62 shows a 0-V to 10-V Input DAQ Circuit with a DC accuracy of 0.1%.

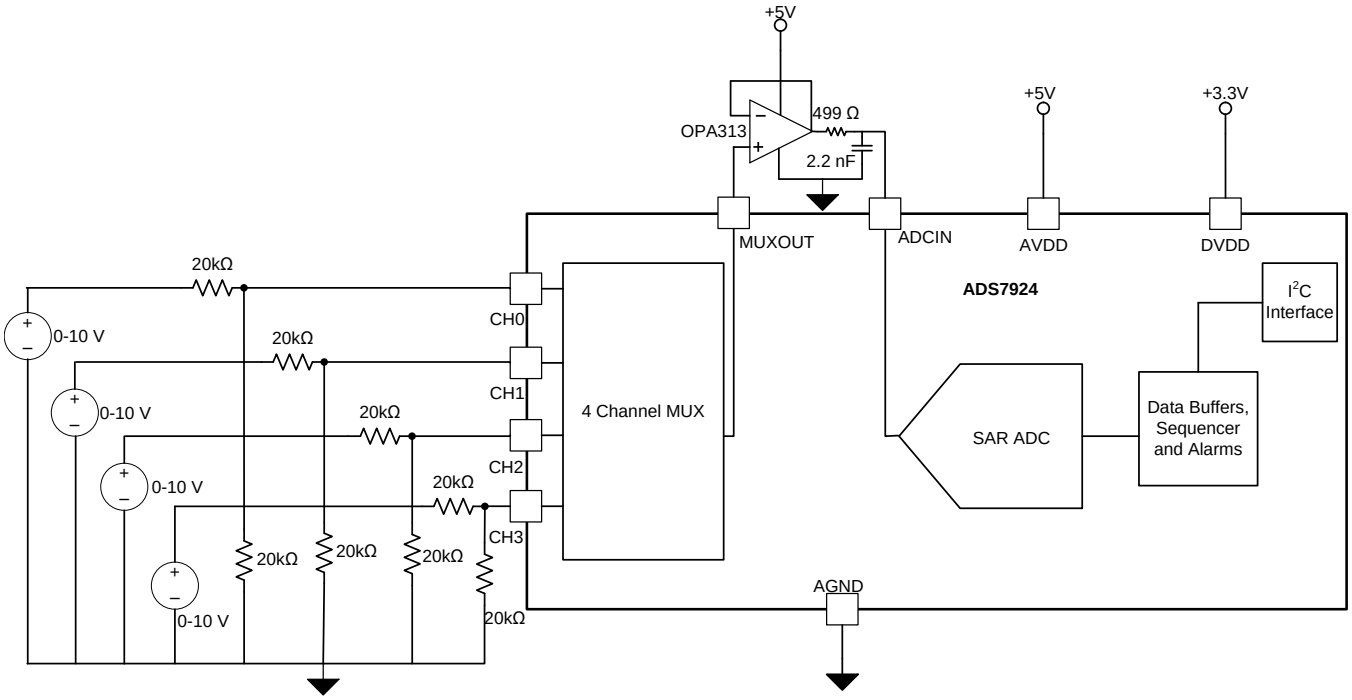


Figure 62. 0-V to 10-V Input DAQ Circuit

8.2.1 Design Requirements

Table 6 shows the design parameters for this typical application.

Table 6. Design Parameters

DESIGN PARAMETER	DESIGN GOAL
Throughput	100 SPS
DC Accuracy	0.1%
Full Scale Step Settling	20 µs
DC Noise at input of ADC	200 µV RMS
Input Impedance	40 kΩ

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Throughput

The throughput was set by selecting a sleep time of 40 ms, sleep divider of 4 and acquisition time of 6 µs.

8.2.2.2 Selecting the Operational Amplifier

The key parameters for selecting the operational amplifier for this circuit are noise, offset voltage and input bias current. The offset voltage and input bias current affect the DC accuracy whereas the noise of the amplifier increases the total noise at the input of ADC, the total noise at the input of ADC (V_n) can be calculated by Equation 9. V_n must be less than 200-µV RMS for this circuit design.

$$V_n = \sqrt{\left(\frac{V_{1/f\_AMP\_PP}}{6.6}\right)^2 + e^2_{n\_RMS} \times \frac{\pi}{2} \times f_{-3dB} + V^2_{N\_ADC}}$$

where

- e_{n_RMS} is the input voltage noise density of the amplifier.

- V_{N_ADC} is the DC noise of the ADC. For ADS7924 , DC Noise is specified as 0.125 LSB RMS.
- V_{1/f_AMP_PP} is the peak to peak low-frequency noise at the input of amplifier.
- f_{-3dB} is the bandwidth of RC filter at the output of amplifier. (9)

OPA313 is selected for this design for its low noise (25 nv/√Hz), low offset voltage (0.5 mV) and low input bias current (0.2 pA).

8.2.2.3 Selecting the RC Filter

The RC filter at the output of amplifier affect full scale settling time and noise at the input of ADC. Full scale settling time can be calculated using Equation 3 and the noise at input of ADC can be calculated using Equation 9. A value of 499 Ω and 2.2 nF is used for achieving the full scale settling time of 20 µs and total DC noise of less than 200 µV RMS.

8.2.3 Application Curves

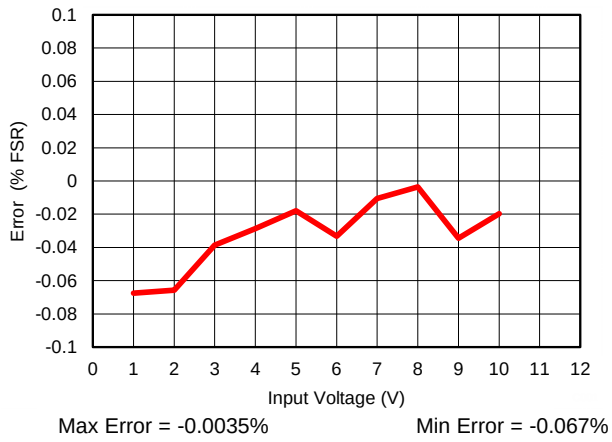


Figure 63. Error vs Input Voltage

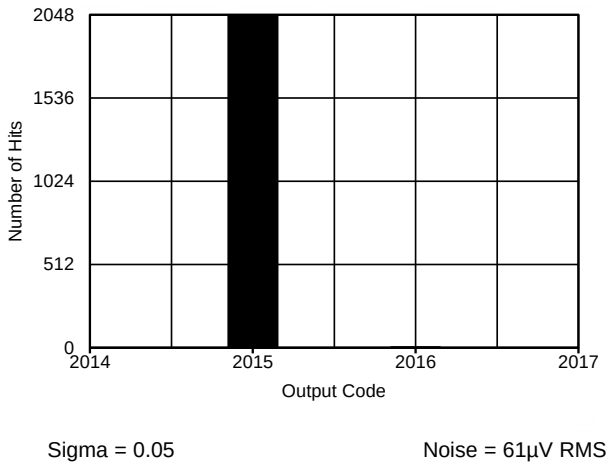


Figure 64. Number of Hits vs Output Code

9 Power Supply Recommendations

The device has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. DVDD supply voltage cannot exceed the AVDD supply voltage. The Power supply pins of the device must be decoupled with 1-µF ceramic bypass capacitors. The AVDD supply also defines the full-scale input range of the device. Always set the AVDD supply to be greater than or equal to the maximum input signal to avoid saturation of codes.

10 Layout

10.1 Layout Guidelines

Figure 65 provides an example layout for the device. Use a ground plane underneath the device and partition the PCB into analog and digital sections. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. In Figure 65, the analog signals are routed on the rightside of the device and the digital signals are routed on the left side of the device.

The power sources to the device must be clean and well-bypassed. Use 1-µF ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect all ground pins to the ground plane using short, low-impedance paths. The AVDD supply voltage for the device also functions as a reference for the device. Place the decoupling capacitor for AVDD close to the device AVDD pin and connect this capacitor to the device pins with thick copper tracks.

10.2 Layout Example

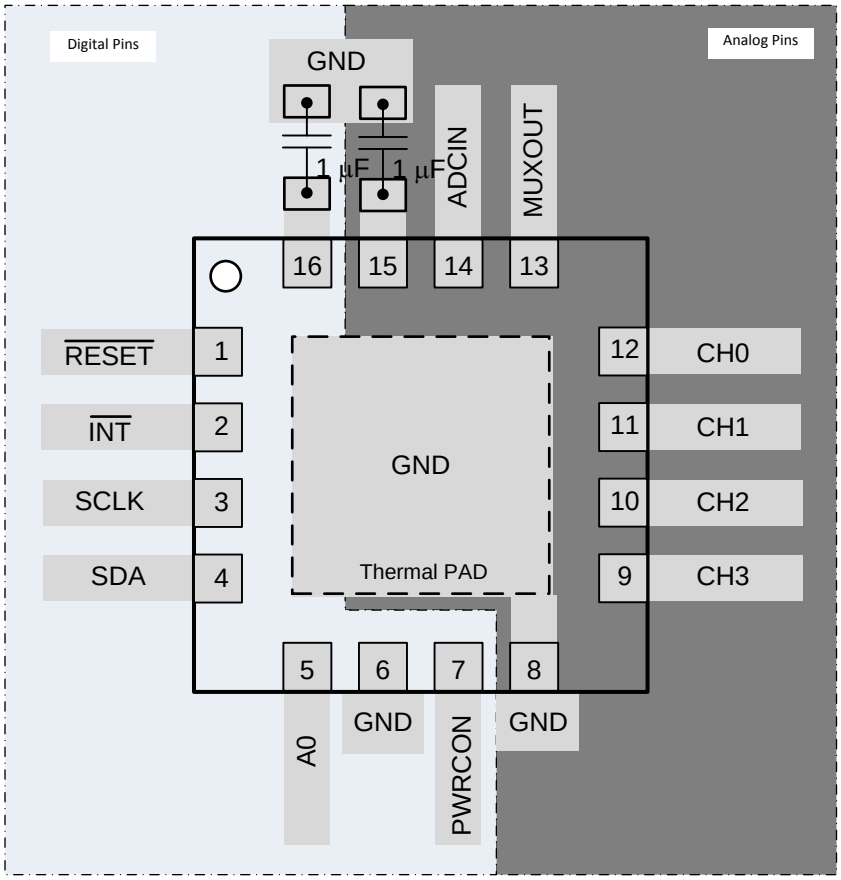


Figure 65. Example Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

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11.2 Trademarks

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11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, see the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7924IRTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7924	Samples
ADS7924IRTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	7924	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

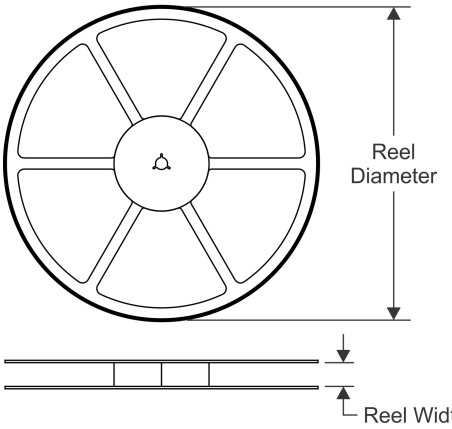
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

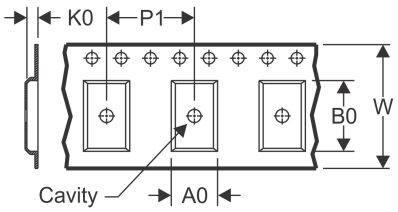
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

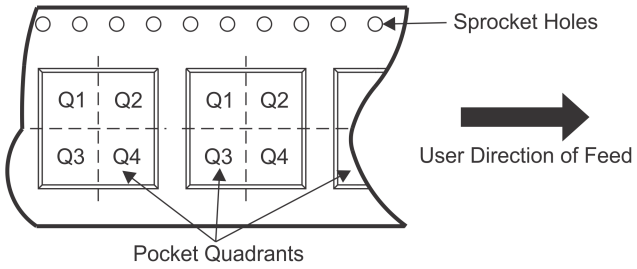


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

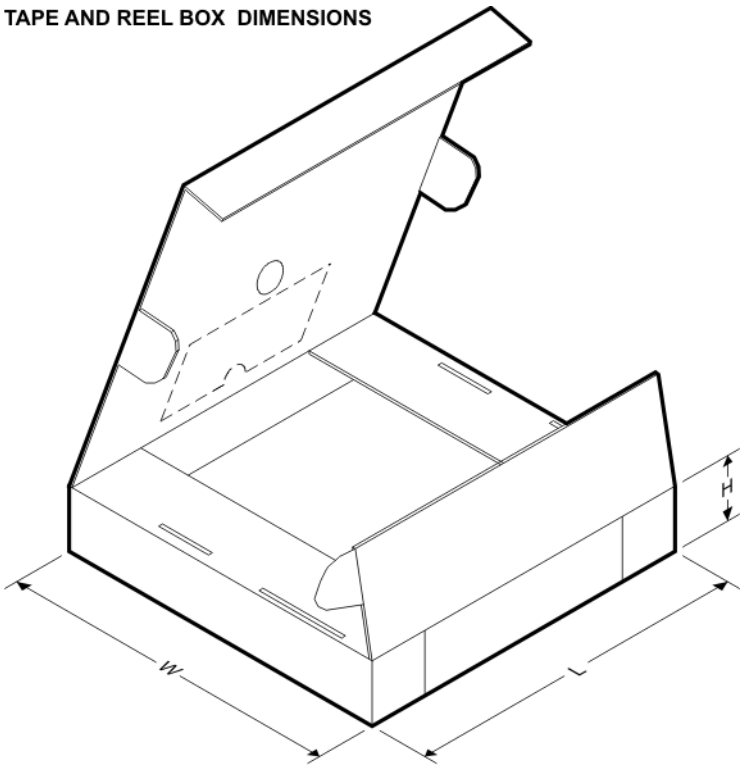
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7924IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7924IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

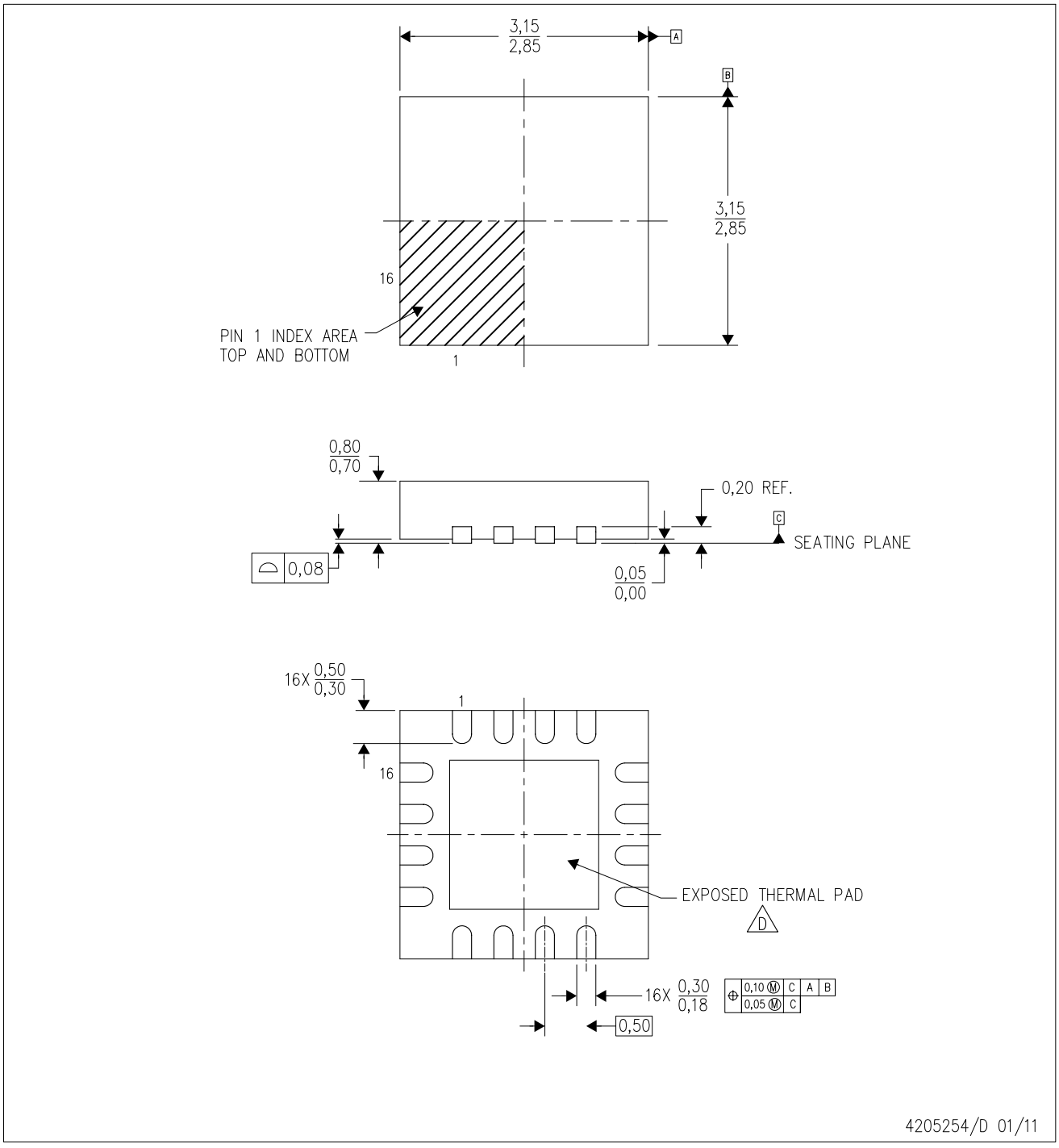
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7924IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7924IRTET	WQFN	RTE	16	250	210.0	185.0	35.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

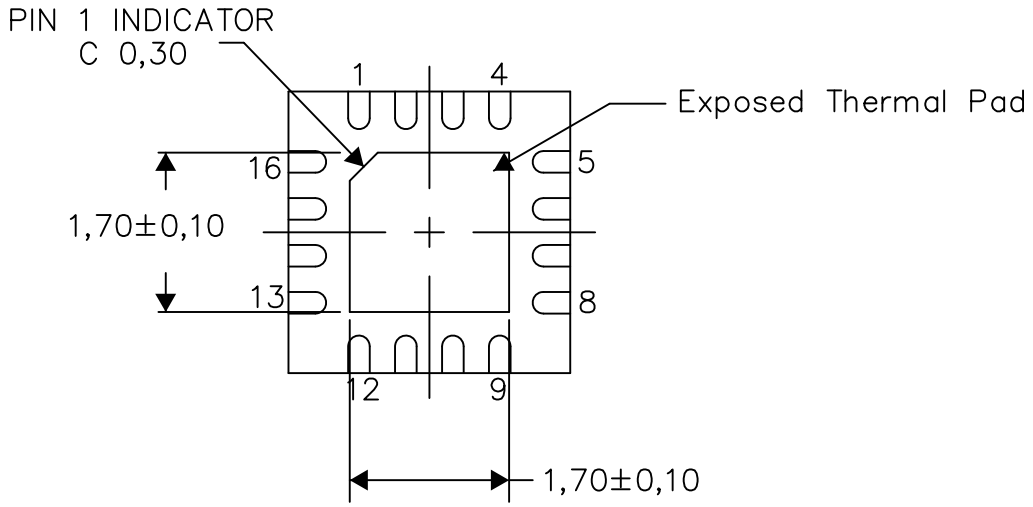
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



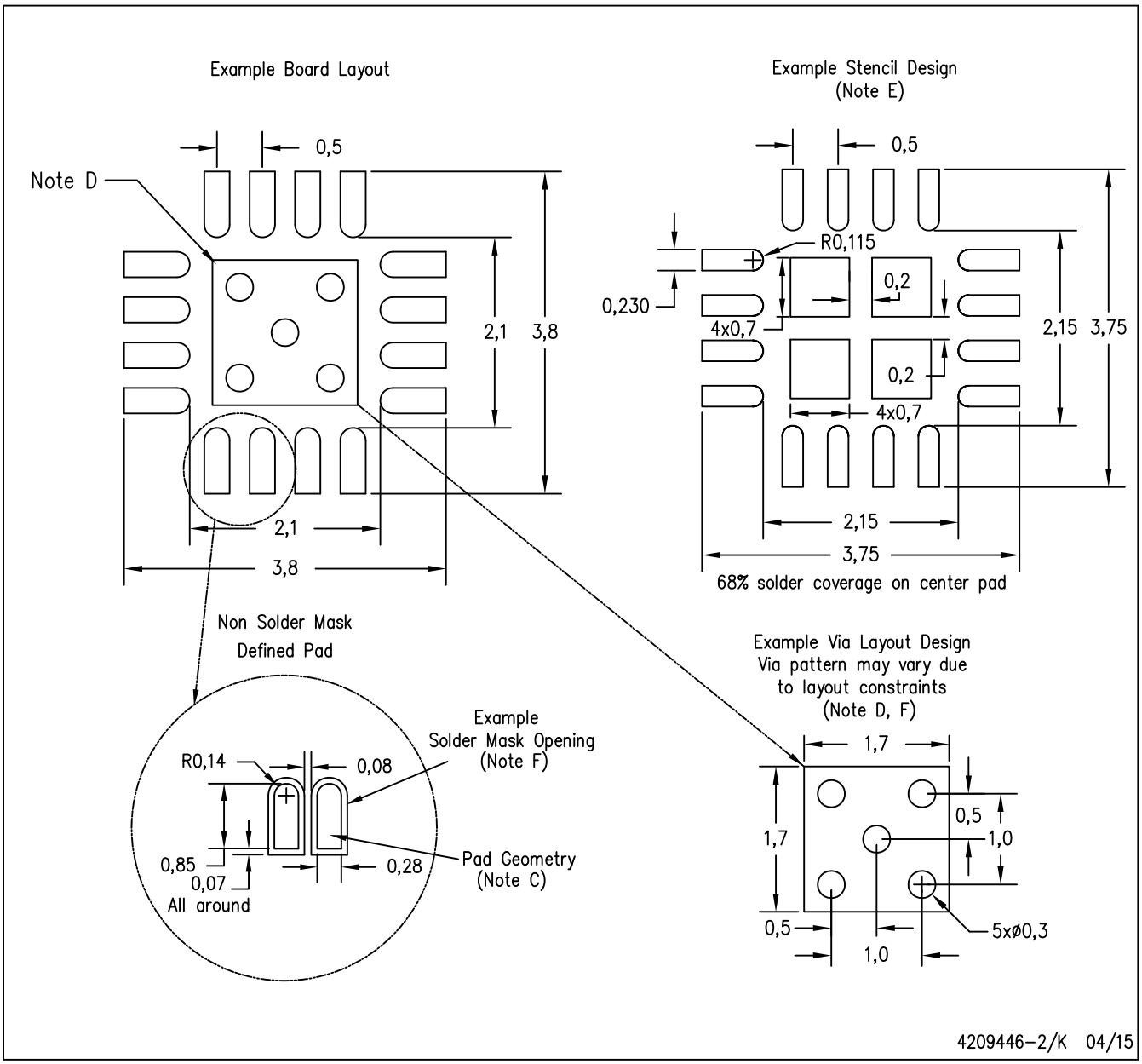
Bottom View

Exposed Thermal Pad Dimensions

4206446–3/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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