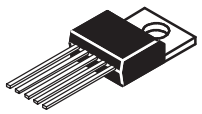
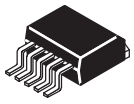




FAST-TRANSIENT RESPONSE, 3A, LOW-DROPOUT VOLTAGE REGULATORS

FEATURES

- **3A Low-Dropout Voltage Regulator**
- **Available in 1.5V, 1.8V, 2.5V, and 3.3V Fixed-Output and Adjustable Versions**
- **Dropout Voltage Typically 150mV at 3A (TPS75833)**
- **V_{REF} and Pinout Compatible with MIC29302 (TPS758A01)**
- **Low 125μA Typical Quiescent Current**
- **Fast Transient Response**
- **3% Tolerance Over Specified Conditions for Fixed-Output Versions**
- **Available in 5-Pin TO-220 and TO-263 Surface-Mount Packages**
- **Thermal Shutdown Protection**

DESCRIPTION

The TPS758xx family of 3A low dropout (LDO) regulators contains four fixed voltage option regulators and an adjustable voltage option regulator. These devices are capable of supplying 3A of output current with a dropout of 150mV (TPS75833). Therefore, the device is capable of performing a 3.3V to 2.5V conversion.

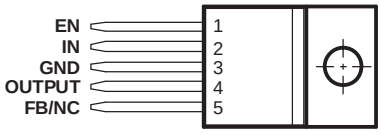
Quiescent current is 125μA at full load and drops to less than 1μA when the device is disabled. The TPS758xx is designed to have fast transient response for large load current changes.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 150mV at an output current of 3A for the TPS75833) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 125μA over the full range of output current). These two key specifications yield a significant improvement in operating life for battery-powered systems.

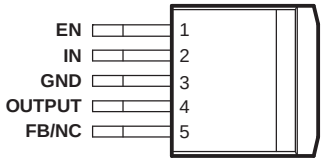
The device is enabled when EN (enable) is connected to a high voltage level (> 2V). Applying a low voltage level (< 0.7V) to EN shuts down the regulator, reducing the quiescent current to less than 1μA at T_J = +25°C.

The TPS758xx is offered in 1.5V, 1.8V, 2.5V, and 3.3V fixed-voltage versions and in an adjustable version (programmable over the range of 1.22V to 5V). Output voltage tolerance is specified as a maximum of 3% over line, load, and temperature ranges. The TPS758xx family is available in a 5-pin TO-220 (KC) and TO-263 (KTT) packages.

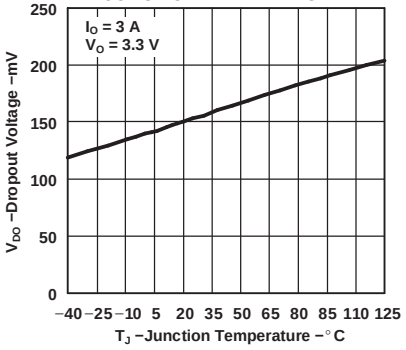
TO−220 (KC) PACKAGE
(TOP VIEW)



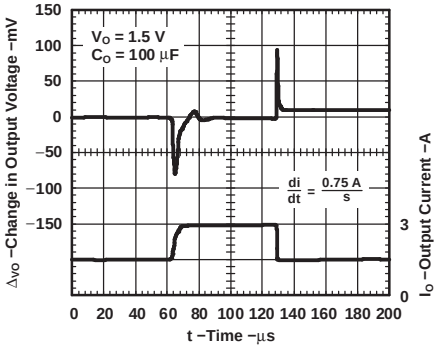
TO−263 (KTT) PACKAGE
(TOP VIEW)



TPS75833
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE



TPS75815
LOAD TRANSIENT RESPONSE



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}
TPS758**xxyyyz** or TPS758A01***yyyz***(2)	**XX** is nominal output voltage (for example, 25 = 2.5V, 01 = Adjustable). **YYY** is package designator. **Z** is package quantity.

(1) For the most current specification and package information, refer to the Package Option Addendum located at the end of this datasheet or see the TI website at www.ti.com.
(2) TPS758A01 available in adjustable version only. See *TPS758A01 Reference Voltage* in Electrical Characteristics for different V_{REF} range.

ABSOLUTE MAXIMUM RATINGS

Over operating junction temperature range (unless otherwise noted)(1)(2)

	TPS758xx	UNIT
Input voltage range, V_{IN}	–0.3 to 6	V
Voltage range at EN	–0.3 to 6	V
Peak output current	Internally limited	
Continuous total power dissipation	See Dissipation Ratings Table	
Output voltage, V_{OUT} (OUT, FB)	5.5	V
Operating junction temperature range, T_J	–40 to +150	°C
Storage temperature range, T_{STG}	–65 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network terminal ground.

DISSIPATION RATINGS TABLE

PACKAGE	$R_{\Theta JC}$(°C/W)	$R_{\Theta JA}$(°C/W)(1)
TO-220	2	58.7(2)
TO-263	2	38.7(3)

(1) For both packages, the $R_{\Theta JA}$ values were computed using a JEDEC High-K board (2S2P) with a 1-ounce internal copper plane and ground plane. There was no air flow across the packages.
(2) $R_{\Theta JA}$ was computed assuming a vertical, free-standing TO-220 package with pins soldered to the board. There is no heatsink attached to the package.
(3) $R_{\Theta JA}$ was computed assuming a horizontally-mounted TO-263 package with pins soldered to the board. There is no copper pad underneath the package.

ELECTRICAL CHARACTERISTICS

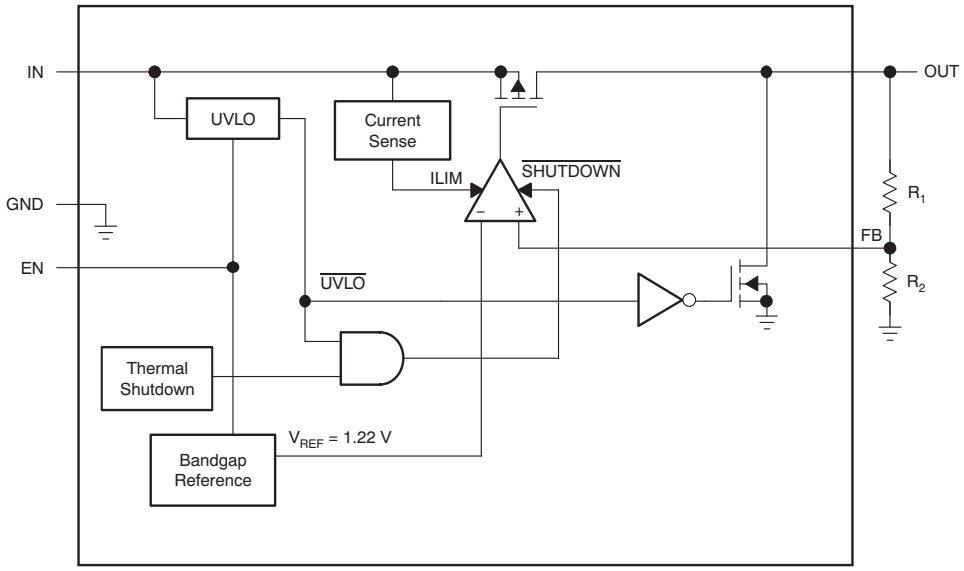
Over recommended operating junction temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 1mA, V_{EN} = V_{IN}, C_{OUT} = 100µF (unless otherwise noted). Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			2.8		5.5	V
V_{REF}	Reference voltage	TPS75801			1.225		V
		TPS758A01			1.24		V
V_{OUT}	Output voltage range			V_{REF}		5	V
	Accuracy(1)	TPS75801	V_{OUT} + 1V ≤ V_{IN} ≤ 5.5V, 1mA ≤ I_{OUT} ≤ 3A	–3		+3	%
		TPS758A01	V_{OUT} + 1V ≤ V_{IN} ≤ 5.5V, 1mA ≤ I_{OUT} ≤ 3A	–3		+3	%
$\Delta V_{OUT}\%/\Delta V_{IN}$	Line regulation(1)		V_{OUT} + 1V ≤ V_{IN} < 5.5V		0.04	0.1	%/V
$\Delta V_{OUT}\%/\Delta I_{OUT}$	Load regulation		1mA ≤ I_{OUT} ≤ 3A		0.15		%
V_{DO}	Dropout voltage (2)		V_{IN} = 3.2V, I_{OUT} = 3A		150	300	mV
I_{CL}	Output current limit		V_{OUT} = 0V	5.5	10	14	A
I_{GND}	Ground pin current		1mA ≤ I_{OUT} ≤ 3A		125	200	µA
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} = 0V		0.1	3	µA
I_{FB}	FB pin current		FB = 1.5V	–1		1	µA
PSRR	Power-supply rejection ratio (ripple rejection)		f = 100Hz, V_{IN} = 2.8V, V_{OUT} = 1.5V, I_{OUT} = 3A		62		dB
V_N	Output noise voltage		BW = 300Hz to 50kHz, V_{IN} = 2.8V, V_{OUT} = 1.5V		35		μV_{RMS}
V_{EN}(HI)	Enable high (enabled)			2			V
V_{EN}(LO)	Enable low (shutdown)					0.7	V
I_{EN}(HI)	Enable pin current (enabled)		V_{EN} = V_{IN}	–1		1	µA
			V_{EN} = 0V	–1	0	1	µA
	Output discharge transistor current		T_J = +25°C, V_{OUT} = 1.5V	10	25		mA
UVLO	Undervoltage lockout		T_J = +25°C, V_{IN} rising	2.2		2.75	V
	Hysteresis		V_{IN} falling		100		mV
T_{SD}	Thermal shutdown temperature				+150		°C
T_J	Operating junction temperature			–40		+125	°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.8V, whichever is greater.
(2) V_{IN} = $V_{OUT(nom)}$ – 0.1V. V_{DO} is not measured for devices with $V_{OUT(nom)}$ < 2.9V because minimum V_{IN} = 2.8V.

FUNCTIONAL BLOCK DIAGRAMS

ADJUSTABLE VOLTAGE VERSION



FIXED VOLTAGE VERSIONS

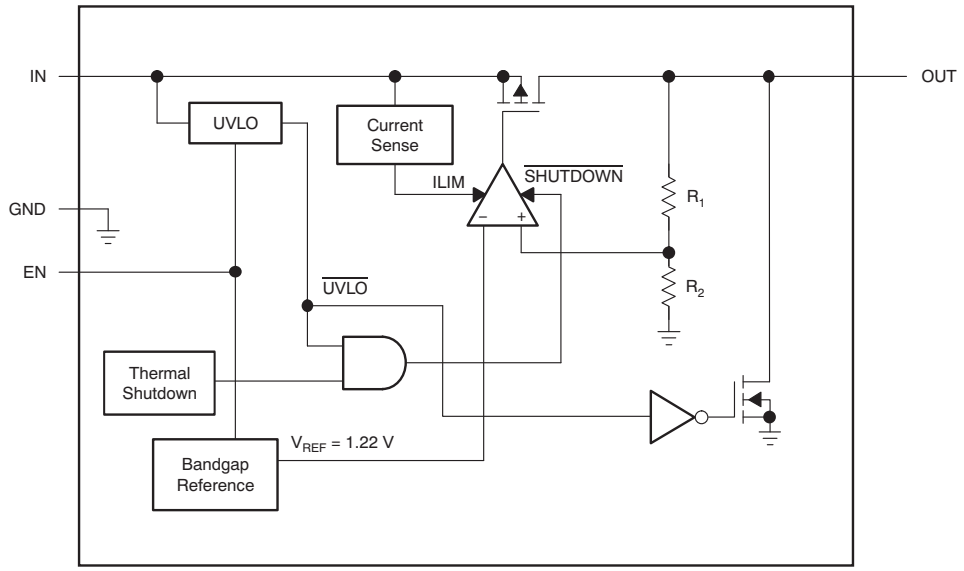


Table 1. TERMINAL FUNCTIONS

TPS758xx		
NAME	**PIN NO.**	**DESCRIPTION**
EN	1	Enable input
IN	2	Input supply
GND	3	Ground
OUT	4	Regulated output voltage; see Output Capacitor section for output capacitor requirements.
FB/NC	5	Feedback voltage for adjustable device. Connect to GND or leave open for fixed V_{OUT} devices.

TYPICAL CHARACTERISTICS

TPS75833
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

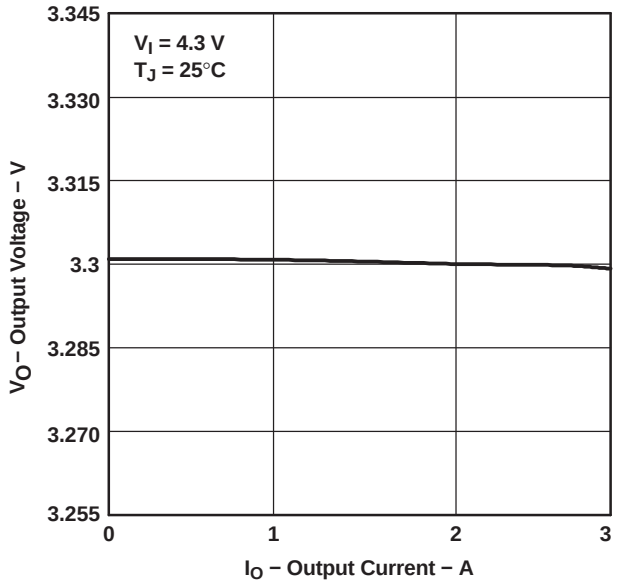


Figure 1.

TPS75815
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

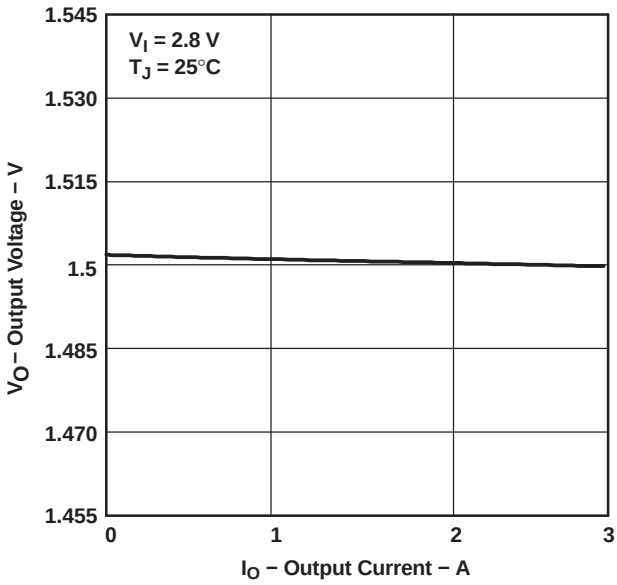


Figure 2.

TPS75833
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

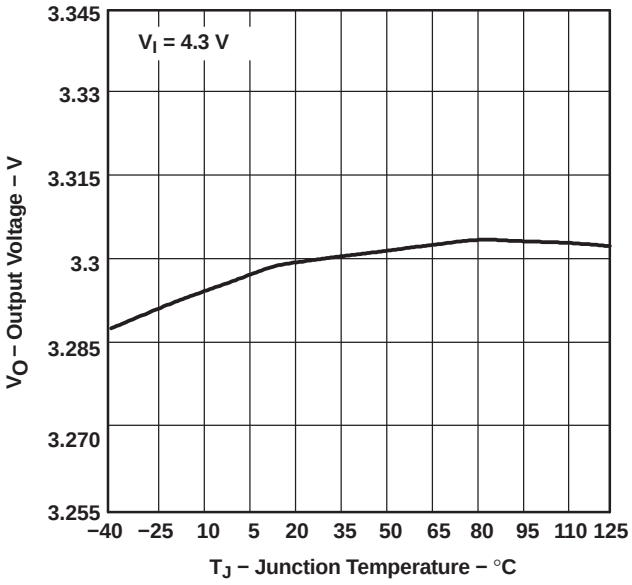


Figure 3.

TPS75815
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

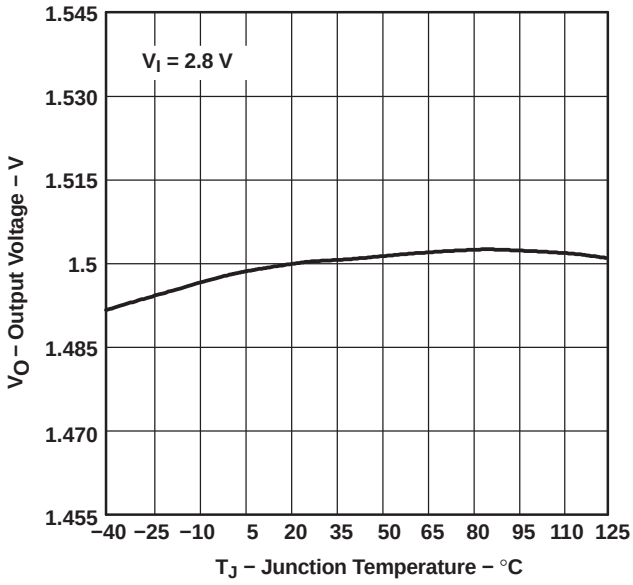


Figure 4.

TYPICAL CHARACTERISTICS (continued)

TPS758xx
GROUND CURRENT
vs
JUNCTION TEMPERATURE

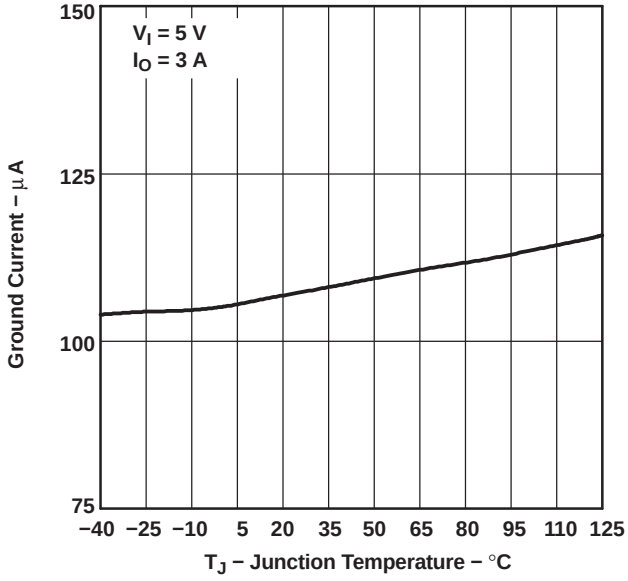


Figure 5.

TPS75833
POWER-SUPPLY RIPPLE REJECTION
vs
FREQUENCY

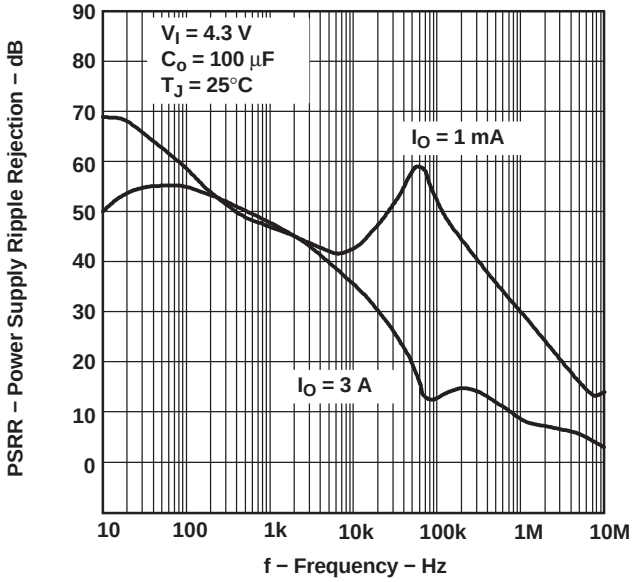


Figure 6.

TPS75833
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

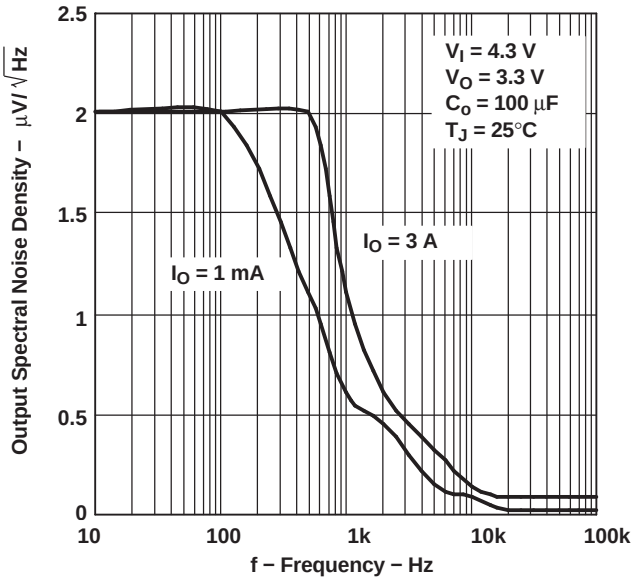


Figure 7.

TPS75833
OUTPUT IMPEDANCE
vs
FREQUENCY

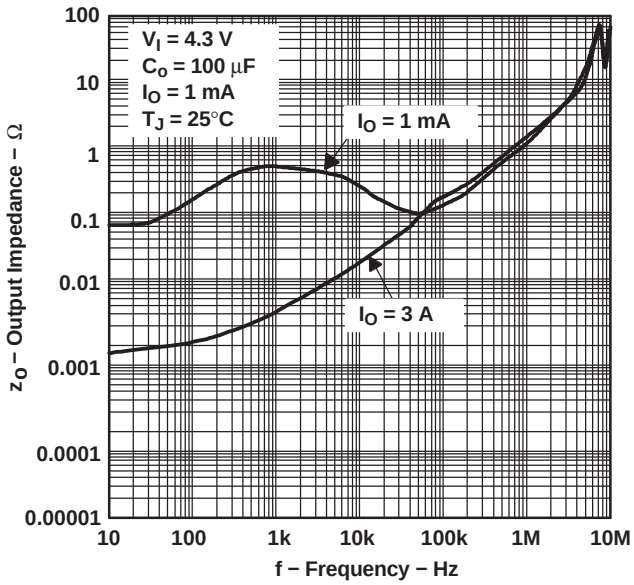


Figure 8.

TYPICAL CHARACTERISTICS (continued)

TPS75801
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

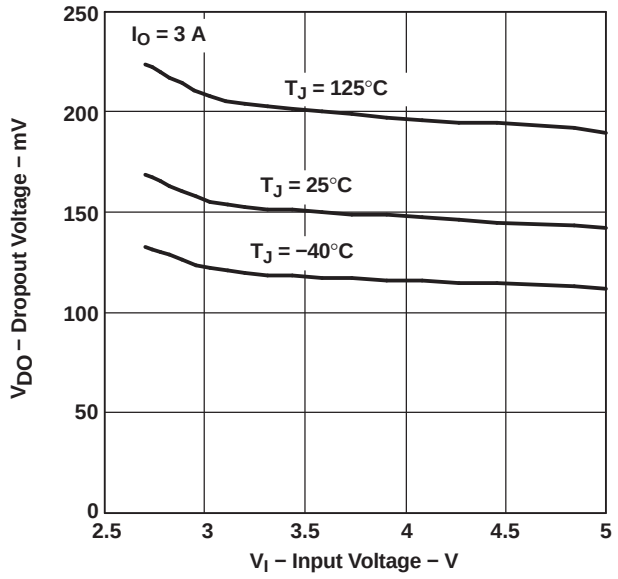


Figure 9.

TPS75833
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

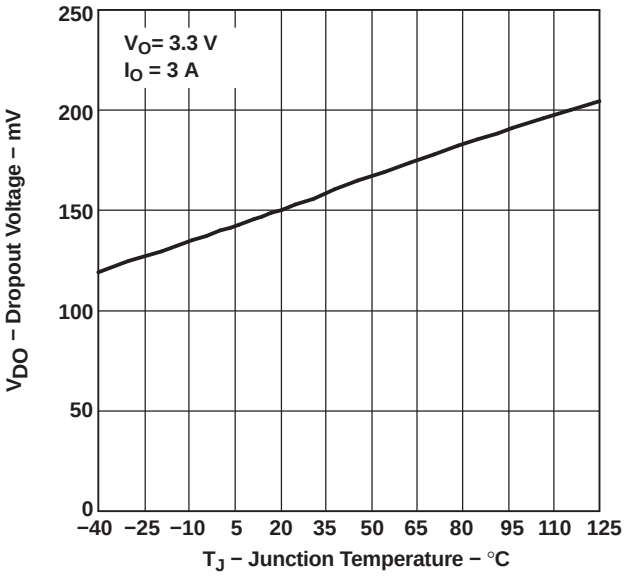


Figure 10.

MINIMUM REQUIRED INPUT VOLTAGE
vs
OUTPUT VOLTAGE

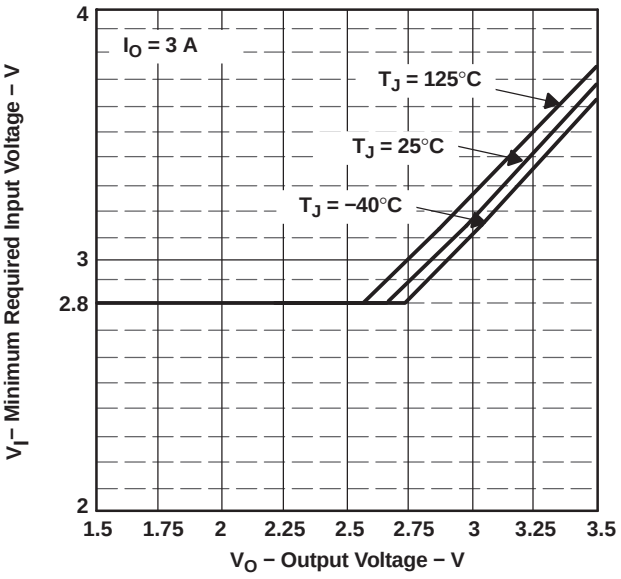


Figure 11.

TPS75815
LINE TRANSIENT RESPONSE

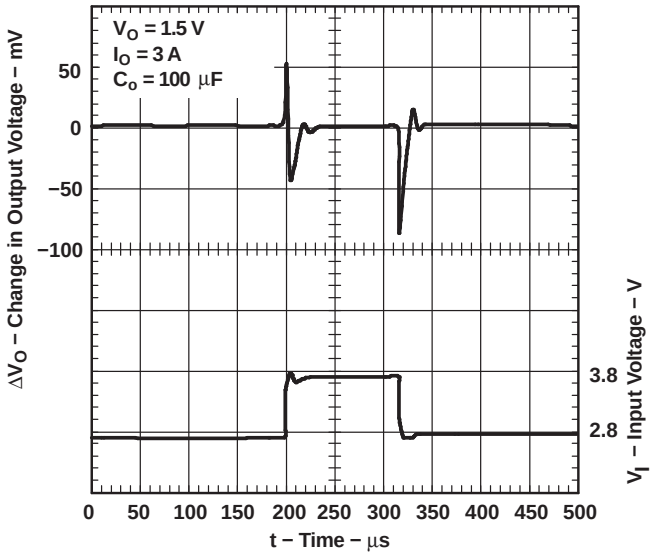


Figure 12.

TYPICAL CHARACTERISTICS (continued)

TPS75815
LOAD TRANSIENT RESPONSE

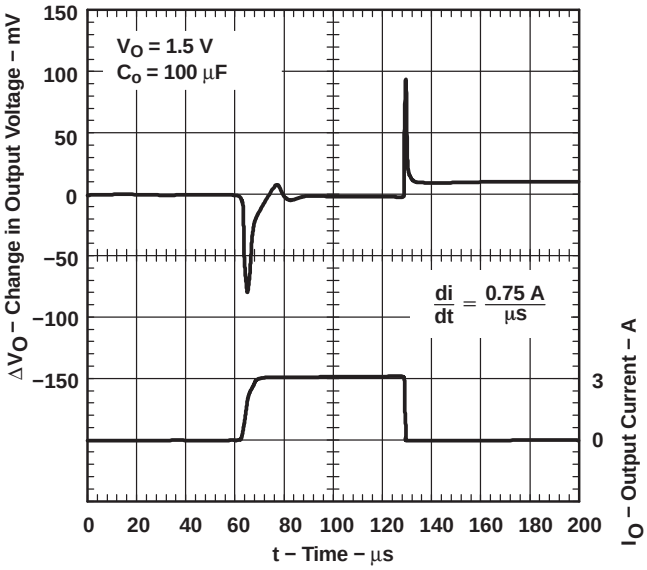


Figure 13.

TPS75833
LINE TRANSIENT RESPONSE

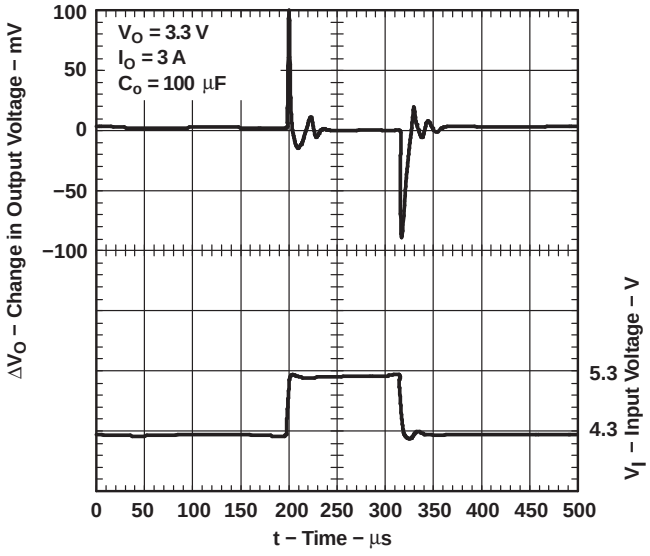


Figure 14.

TPS75833
LOAD TRANSIENT RESPONSE

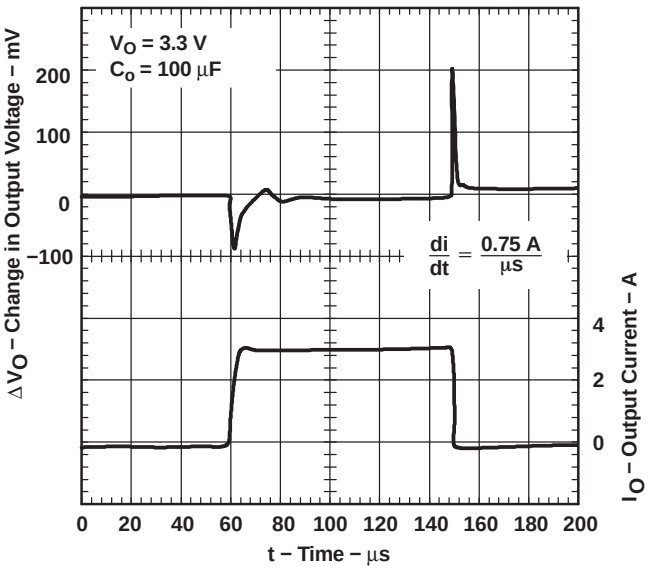


Figure 15.

TPS75833
OUTPUT VOLTAGE AND ENABLE VOLTAGE
TIME (START-UP)

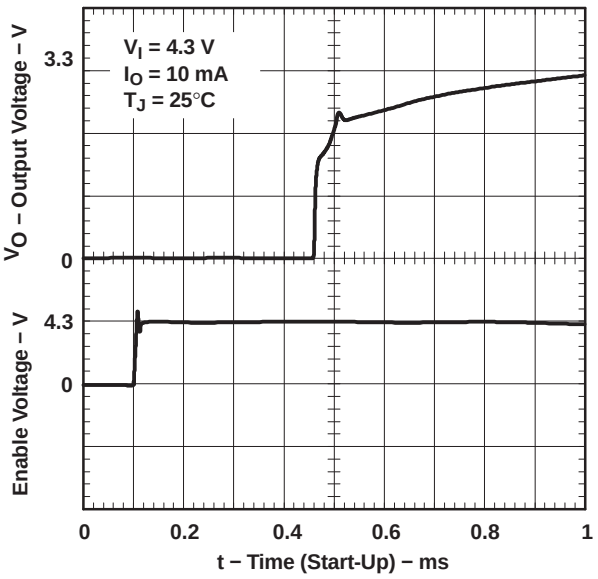


Figure 16.

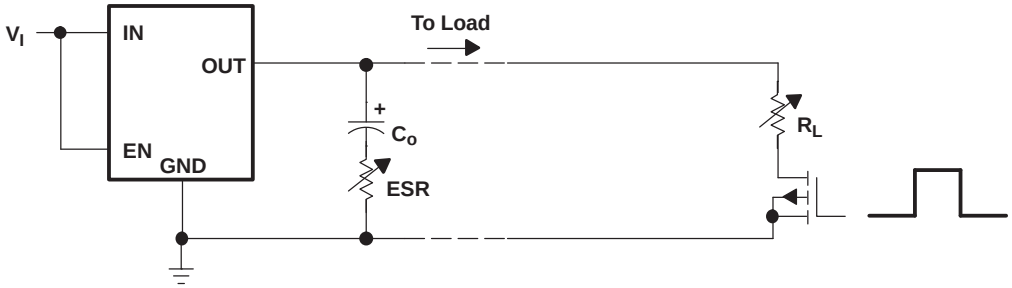


Figure 17. Test Circuit for Typical Regions of Stability (Figure 18 and Figure 19) (Fixed Output Options)

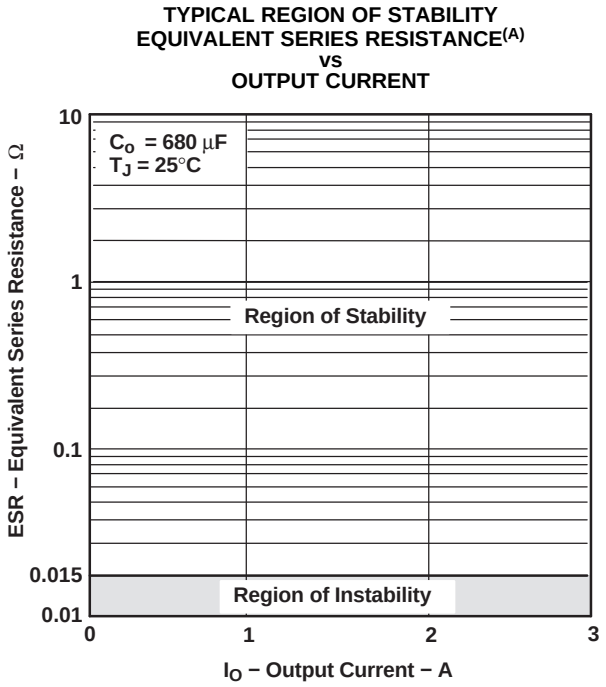


Figure 18.

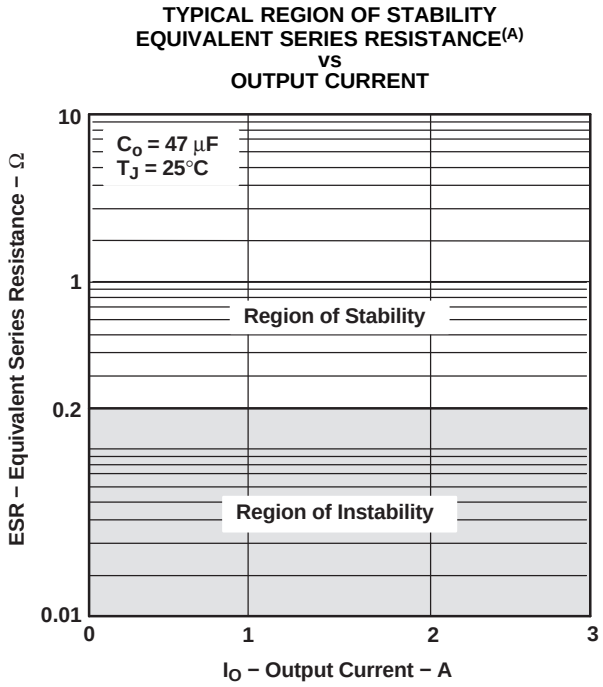


Figure 19.

A. Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and printed wiring board (PWB) trace resistance to C_{OUT}.

DETAILED DESCRIPTION

The TPS758xx family includes four fixed-output voltage regulators (1.5V, 1.8V, 2.5V, and 3.3V), and an adjustable regulator, the TPS75801 (adjustable from 1.22V to 5V). The bandgap voltage is typically 1.22V.

Pin Functions

Enable (EN)

The EN terminal is an input which enables or shuts down the device. If EN is a low voltage level (< 0.7V), the device will be in shutdown or sleep mode. When EN goes to a high voltage level (> 2V), the device will be enabled.

Feedback (FB)

FB is an input terminal used for the adjustable-output option and must be connected to the output terminal either directly, in order to generate the minimum output voltage of 1.22V, or through an external feedback resistor divider for other output voltages. The FB connection should be as short as possible. It is essential to route the terminal so that it minimizes/avoids noise pickup. Adding RC networks between the FB terminal and V_{OUT} to filter noise is not recommended because it may cause the regulator to oscillate.

Input Voltage (IN)

The V_{IN} terminal is an input to the regulator.

Output Voltage (OUTPUT)

The V_{OUTPUT} terminal is an output from the regulator.

APPLICATION INFORMATION

Programming the TPS75801 Adjustable LDO Regulator

The output voltage of the TPS75801 adjustable regulator is programmed using an external resistor divider as shown in Figure 20. The output voltage is calculated using:

$$V_O = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

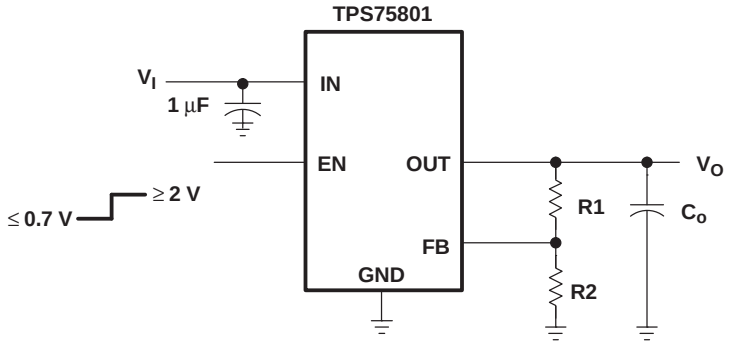
Where:

V_{REF} = 1.224V typ (the internal reference voltage).

Resistors R1 and R2 should be chosen for approximately 40µA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1kΩ to set the divider current at 40µA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{REF}} - 1\right) \times R2 \quad (2)$$

APPLICATION INFORMATION (continued)



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	31.6	30.1	kΩ
3.3 V	51	30.1	kΩ
3.6 V	58.3	30.1	kΩ

Figure 20. TPS75801 Adjustable LDO Regulator Programming

Regulator Protection

The TPS758xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS758xx also features internal current limiting and thermal protection. During normal operation, the TPS758xx limits output current to approximately 10A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds –150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below +130°C (typ), regulator operation resumes.

Input Capacitor

For a typical application, a ceramic input bypass capacitor (0.22μF to 1μF) is recommended to ensure device stability. This capacitor should be as close as possible to the input pin. Due to the impedance of the input supply, large transient currents will cause the input voltage to droop. If this droop causes the input voltage to drop below the UVLO threshold, the device will turn off. Therefore, it is recommended that a larger capacitor be placed in parallel with the ceramic bypass capacitor at the regulator input. The size of this capacitor depends on the output current, response time of the main power supply, and the distance of the main power supply to the regulator. At a minimum, the capacitor should be sized to ensure that the input voltage does not drop below the minimum UVLO threshold voltage during normal operating conditions.

Output Capacitor

As with most LDO regulators, the TPS758xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 47μF with an ESR (equivalent series resistance) of at least 200mΩ. As shown in Figure 21, most capacitor and ESR combinations with a product of 47^{-6} x 0.2 = 9.4^{-6} or larger will be stable, provided the capacitor value is at least 47μF. Solid tantalum electrolytic and aluminum electrolytic capacitors are all suitable, provided they meet the requirements described in this section. Larger capacitors provide a wider range of stability and better load transient response.

This information and the ESR graphs shown in Figure 18, Figure 19, and Figure 21, is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet these guidelines.

APPLICATION INFORMATION (continued)

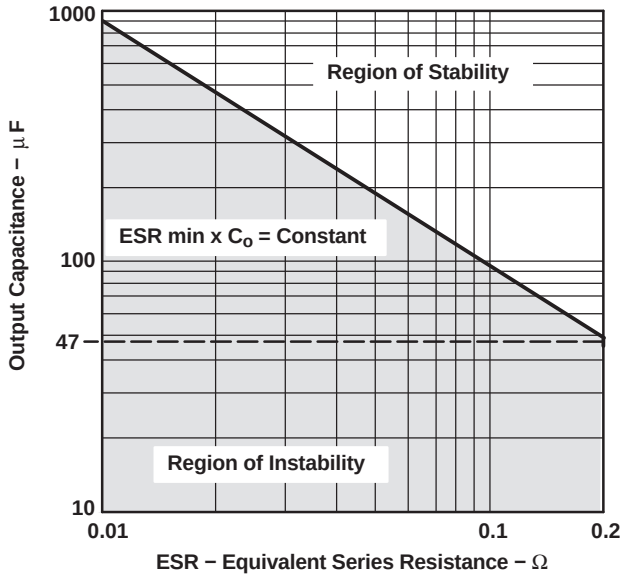


Figure 21. Output Capacitance vs Equivalent Series Resistance

THERMAL INFORMATION

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power it dissipates during operation. All integrated circuits have a maximum allowable junction temperature ($T_J$max) above which normal operation is not assured. A system designer must design the operating environment so that the operating junction temperature (T_J) does not exceed the maximum junction temperature ($T_J$max). The two main environmental variables that a designer can use to improve thermal performance are air flow and external heatsinks. The purpose of this information is to aid the designer in determining the proper operating environment for a linear regulator that is operating at a specific power level.

In general, the maximum expected power ($P_{D(max)}$) consumed by a linear regulator is computed as:

$$P_D\,\text{max} = \left(V_{I(avg)} - V_{O(avg)}\right) \times I_{O(avg)} + V_{I(avg)} \times I_{(Q)} \quad (3)$$

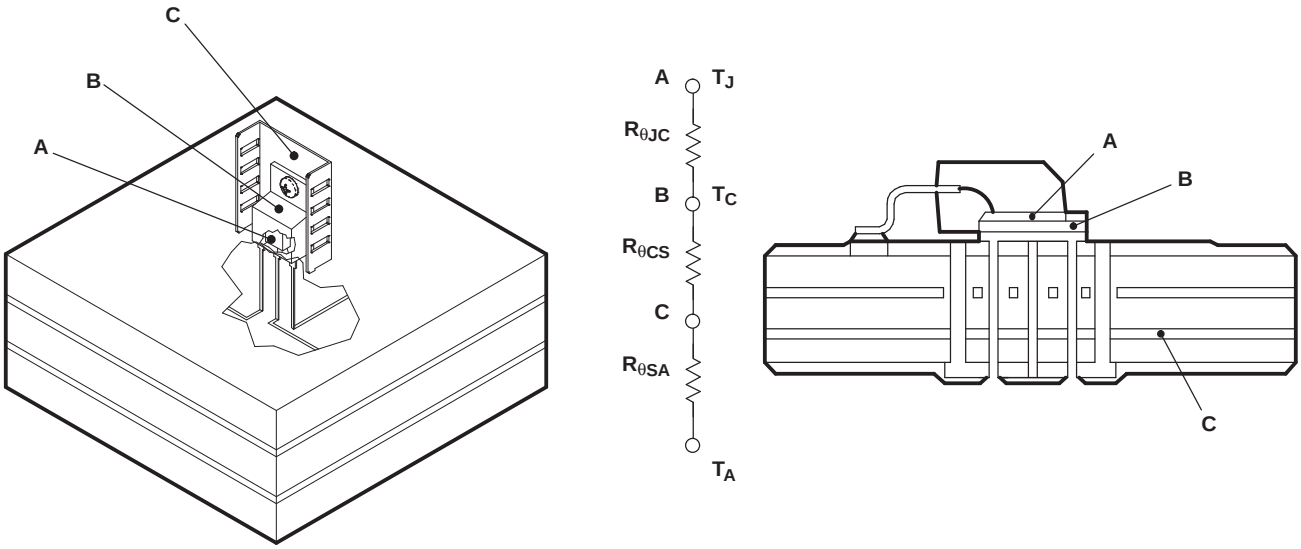
Where:

- $V_{I(avg)}$ is the average input voltage.
- $V_{O(avg)}$ is the average output voltage.
- $I_{O(avg)}$ is the average output current.
- $I_{(Q)}$ is the quiescent current.

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term $V_{I(avg)} \times I_{(Q)}$ can be neglected. The operating junction temperature is computed by adding the ambient temperature (T_A) and the increase in temperature due to the regulator power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ($R_{\Theta JC}$), the case to heatsink ($R_{\Theta CS}$), and the heatsink to ambient ($R_{\Theta SA}$). Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the object's thermal resistance.

Figure 22 illustrates these thermal resistances for (a) a TO-220 package attached to a heatsink, and (b) a TO-263 package mounted on a JEDEC High-K board.

THERMAL INFORMATION (continued)



TO−220 Package
(a)

TO−263 Package
(b)

Figure 22. Thermal Resistances

Equation 4 summarizes the computation:

$$T_J = T_A + P_D \max \cdot \left(R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA}\right) \quad (4)$$

The $R_{\Theta JC}$ is specific to each regulator as determined by its package, lead frame, and die size provided in the regulator's data sheet. The $R_{\Theta SA}$ is a function of the type and size of heatsink. For example, black body radiator type heatsinks, like the one attached to the TO-220 package in Figure 22(a), can have $R_{\Theta CS}$ values ranging from 5°C/W for very large heatsinks to 50°C/W for very small heatsinks. The $R_{\Theta CS}$ is a function of how the package is attached to the heatsink. For example, if a thermal compound is used to attach a heatsink to a TO-220 package, $R_{\Theta CS}$of 1°C/W is reasonable.

Even if no external black body radiator type heatsink is attached to the package, the board on which the regulator is mounted will provide some heatsinking through the pin solder connections. Some packages, like the TO-263 and TI's TSSOP PowerPAD™ packages, use a copper plane underneath the package or the circuit board ground plane for additional heatsinking to improve their thermal performance. Computer-aided thermal modeling can be used to compute very accurate approximations of integrated circuit thermal performance in different operating environments (for example, different types of circuit boards, different types and sizes of heatsinks, different air flows, etc.). Using these models, the three thermal resistances can be combined into one thermal resistance between junction and ambient ($R_{\Theta JA}$). This $R_{\Theta JA}$is valid only for the specific operating environment used in the computer model.

Equation 4 simplifies into Equation 5:

$$T_J = T_A + P_D \max \cdot R_{\Theta JA} \quad (5)$$

Rearranging Equation 5 results in Equation 6:

$$R_{\Theta JA} = \frac{T_J - T_A}{P_D \max} \quad (6)$$

Using Equation 5 and the computer model generated curves shown in Figure 23 and Figure 26, a designer can quickly compute the required heatsink thermal resistance/board area for a given ambient temperature, power dissipation, and operating environment.

THERMAL INFORMATION (continued)

TO-220 Power Dissipation

The TO-220 package provides an effective means of managing power dissipation in through-hole applications. The TO-220 package dimensions are provided in the mechanical drawings at the end of this data sheet. A heatsink can be used with the TO-220 package to effectively lower the junction-to-ambient thermal resistance.

To illustrate, the TPS75825 in a TO-220 package was chosen. For this example, the average input voltage is 3.3V, the average output voltage is 2.5V, the average output current is 3A, the ambient temperature +55°C, the air flow is 150 LFM, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is:

$$P_D\,\text{max} = (3.3 - 2.5)\ \text{V} \times 3\text{A} = 2.4\text{W} \quad (7)$$

Substituting $T_J$max for T_J in Equation 6 results in Equation 8:

$$R_{\Theta JA}\,\text{max} = \frac{(125 - 55)^{\circ}\text{C}}{2.4\text{W}} = 29^{\circ}\text{C/W} \quad (8)$$

From Figure 23, *$R_{\Theta JA}$ vs Heatsink Thermal Resistance*, a heatsink with $R_{\Theta SA}$ = 22°C/W is required to dissipate 2.4W. The model operating environment used in the computer model to construct Figure 23 consisted of a standard JEDEC High-K board (2S2P) with a 1-ounce internal copper plane and ground plane. Since the package pins were soldered to the board, 450mm^2 of the board was modeled as a heatsink. Figure 24 shows the side view of the operating environment used in the computer model.

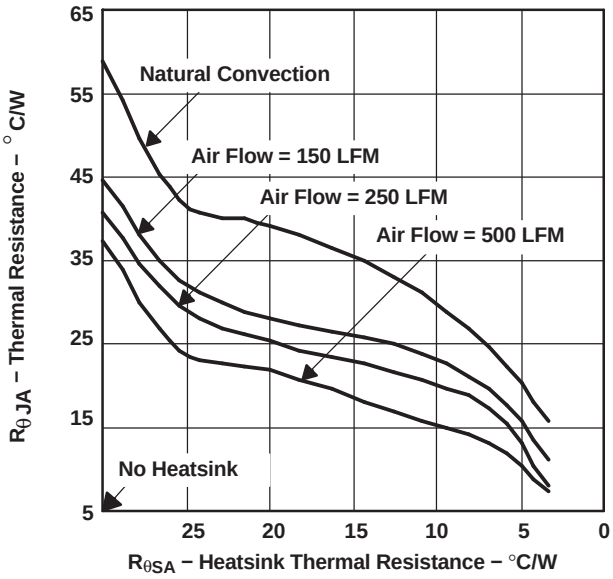


Figure 23. Thermal Resistance vs Heatsink Thermal Resistance

THERMAL INFORMATION (continued)

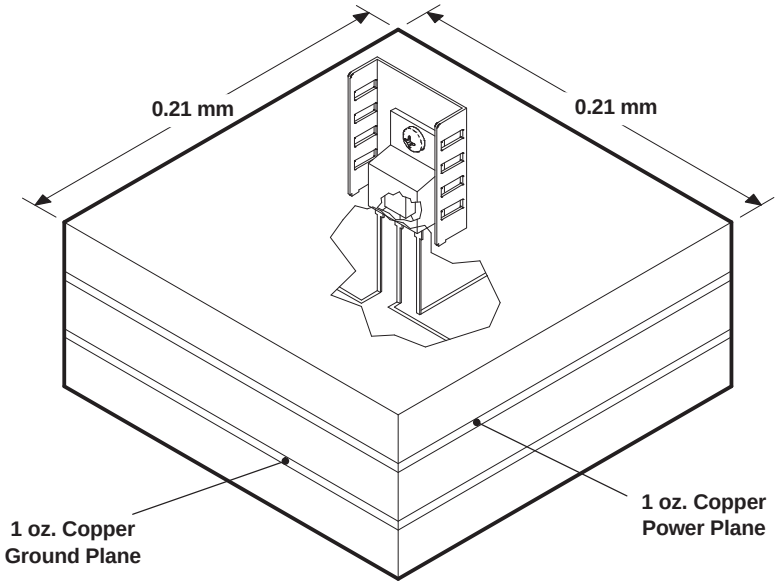


Figure 24. TO-220 Thermal Resistance

From the data in Figure 23 and rearranging Equation 6, the maximum power dissipation for a different heatsink $R_{\Theta SA}$ and a specific ambient temperature can be computed (see Figure 25).

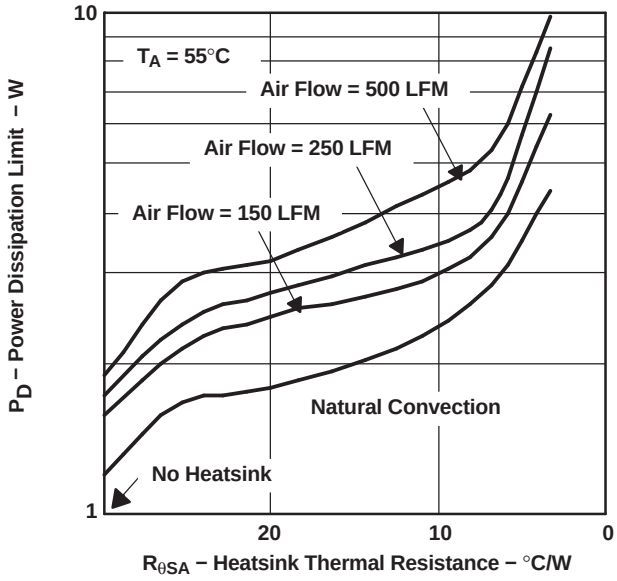


Figure 25. Power Dissipation vs Heatsink Thermal Resistance

THERMAL INFORMATION (continued)

TO-263 Power Dissipation

The TO-263 package provides an effective means of managing power dissipation in surface-mount applications. The TO-263 package dimensions are provided in the mechanical drawings at the end of the data sheet. The addition of a copper plane directly underneath the TO-263 package enhances the thermal performance of the package.

To illustrate, the TPS75825 in a TO-263 package was chosen. For this example, the average input voltage is 3.3V, the average output voltage is 2.5V, the average output current is 3A, the ambient temperature +55°C, the air flow is 150 LFM, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is:

$$P_D\,\text{max} = (3.3 - 2.5)\ \text{V} \times 3\text{A} = 2.4\text{W} \quad (9)$$

Substituting $T_J$max for T_J in Equation 6 results in Equation 10:

$$R_{\Theta JA}\,\text{max} = \frac{(125 - 55)^\circ\text{C}}{2.4\text{W}} = 29^\circ\text{C/W} \quad (10)$$

From Figure 26, *$R_{\Theta JA}$ vs Copper Heatsink Area*, the ground plane needs to be 2cm^2 for the part to dissipate 2.4W. The model operating environment used in the computer model to construct Figure 26 consisted of a standard JEDEC High-K board (2S2P) with a 1-ounce internal copper plane and ground plane. The package is soldered to a 2-ounce copper pad. The pad is tied through thermal vias to the 1-ounce ground plane. Figure 27 shows the side view of the operating environment used in the computer model.

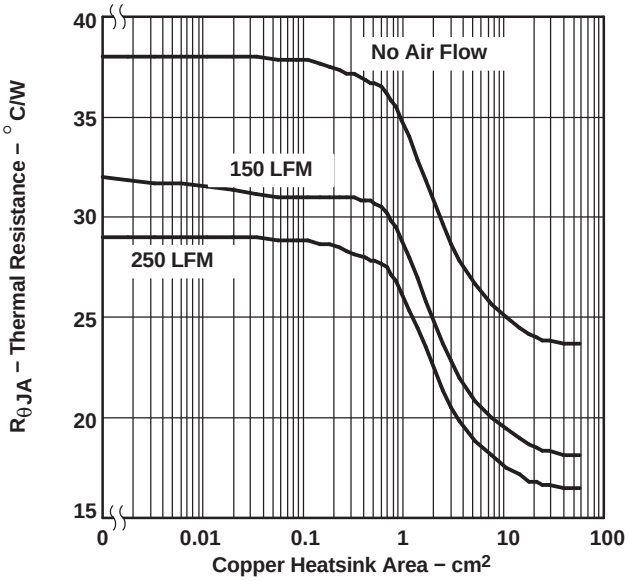


Figure 26. Thermal Resistance vs Copper Heatsink Area

THERMAL INFORMATION (continued)

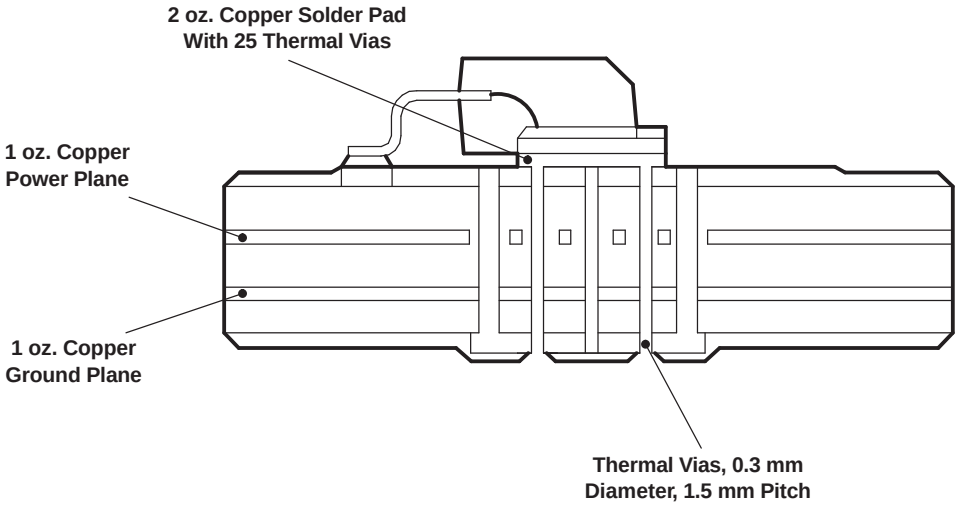


Figure 27. TO-263 Thermal Resistance

The maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed from the data in Figure 26 and from rearranging Equation 6 (see Figure 28).

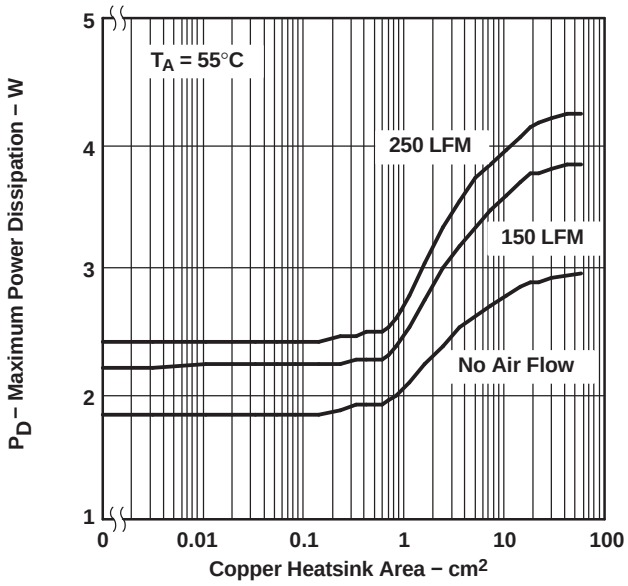


Figure 28. Maximum Power Dissipation vs Copper Heatsink Area

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS75801KC	ACTIVE	TO-220	KC	5	50	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 85	75801	Samples
TPS75801KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	75801	Samples
TPS75801KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	75801	Samples
TPS75801KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	75801	Samples
TPS75801KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	75801	Samples
TPS75815KC	ACTIVE	TO-220	KC	5	50	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 85	75815	Samples
TPS75815KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	75815	Samples
TPS75815KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		75815	Samples
TPS75815KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		75815	Samples
TPS75818KC	ACTIVE	TO-220	KC	5	50	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 85	75818	Samples
TPS75818KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	75818	Samples
TPS75818KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	75818	Samples
TPS75818KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		75818	Samples
TPS75818KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		75818	Samples
TPS75825KC	ACTIVE	TO-220	KC	5	50	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 85	75825	Samples
TPS75825KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	75825	Samples
TPS75825KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	75825	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS75825KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		75825	Samples
TPS75825KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		75825	Samples
TPS75833KC	ACTIVE	TO-220	KC	5	50	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 85	75833	Samples
TPS75833KCG3	ACTIVE	TO-220	KC	5	50	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 85	75833	Samples
TPS75833KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	75833	Samples
TPS75833KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		75833	Samples
TPS75833KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		75833	Samples
TPS758A01KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	758A01	Samples
TPS758A01KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	758A01	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

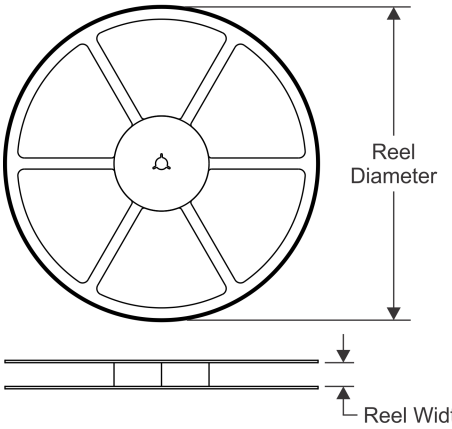
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

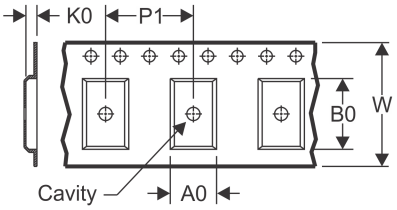
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

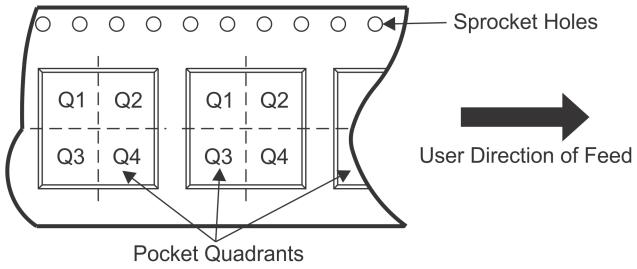


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

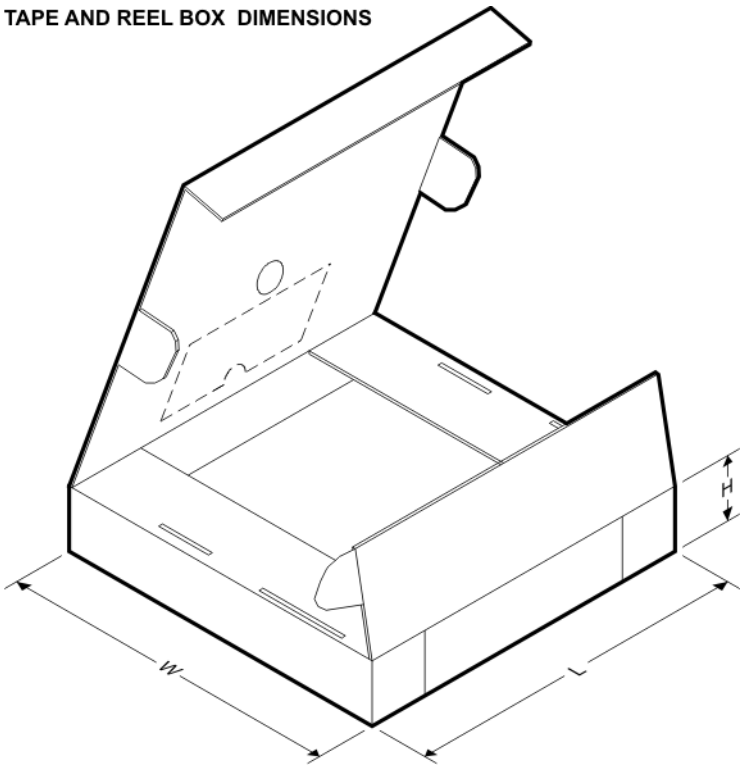


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS75801KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS75801KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS75815KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS75815KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS75818KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS75818KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS75825KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS75825KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS75833KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS75833KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS758A01KTTR	DDPAK/	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	TO-263											
TPS758A01KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

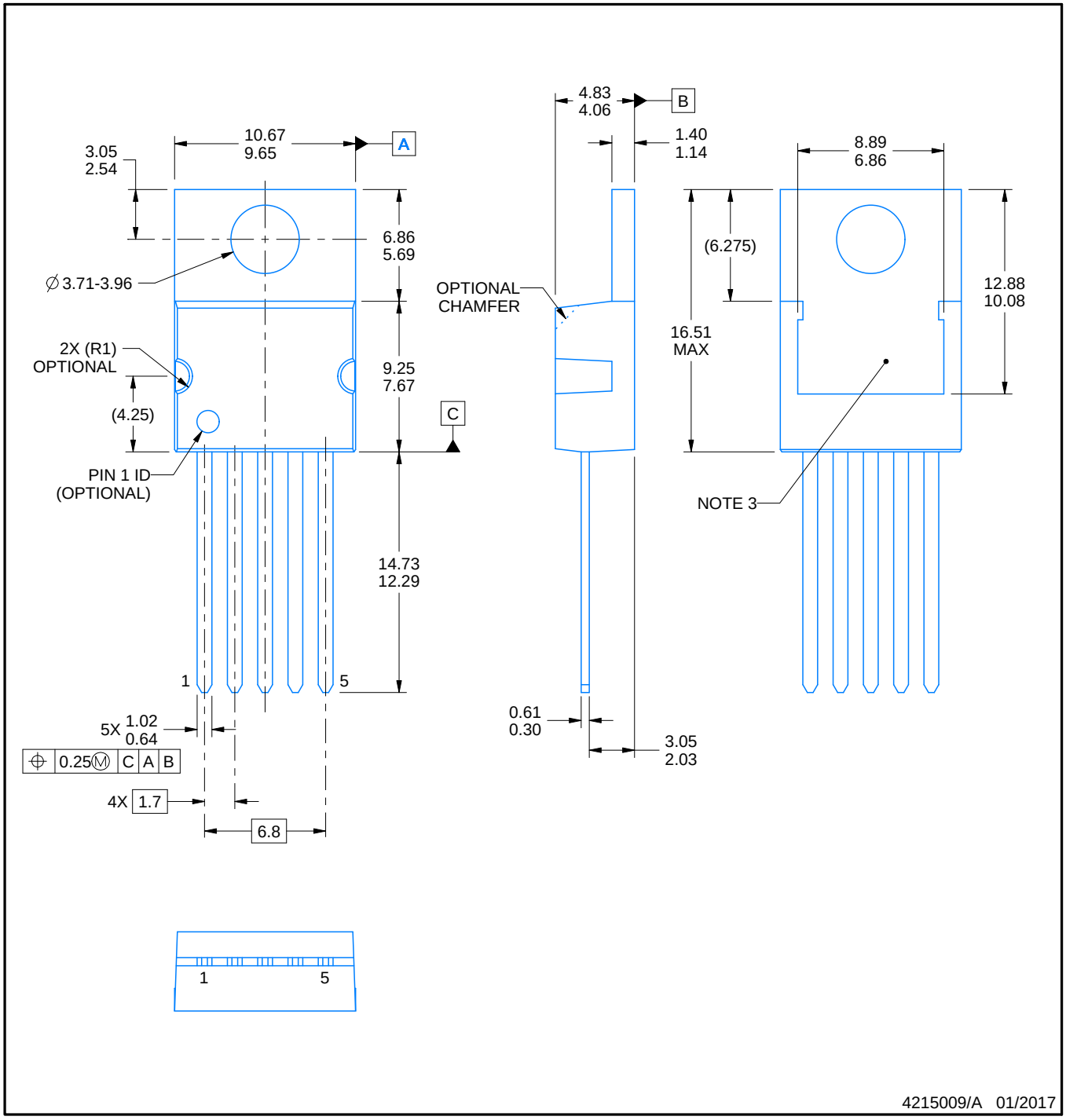
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS75801KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS75801KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
TPS75815KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS75815KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
TPS75818KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS75818KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
TPS75825KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS75825KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
TPS75833KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS75833KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
TPS758A01KTTR	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
TPS758A01KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0

KC0005A

PACKAGE OUTLINE

TO-220 - 16.51 mm max height

TO-220



NOTES:

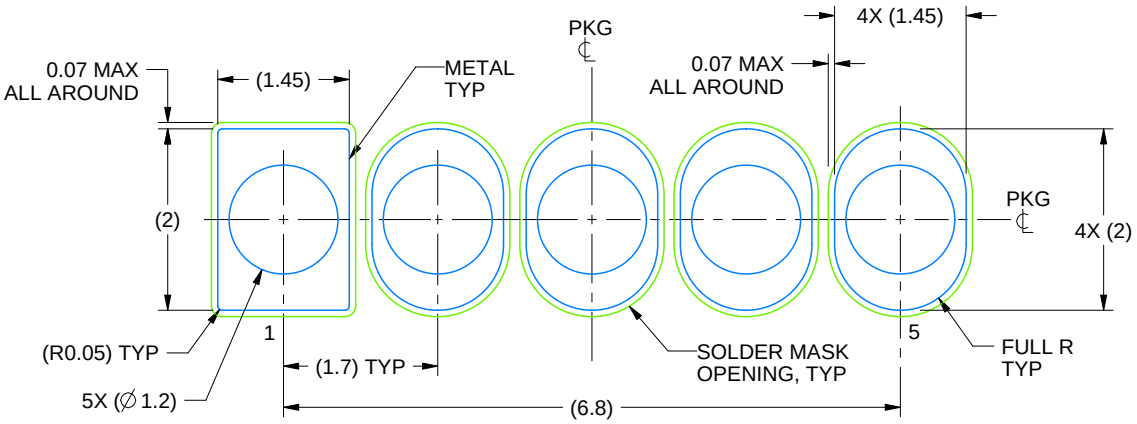
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.

EXAMPLE BOARD LAYOUT

KC0005A

TO-220 - 16.51 mm max height

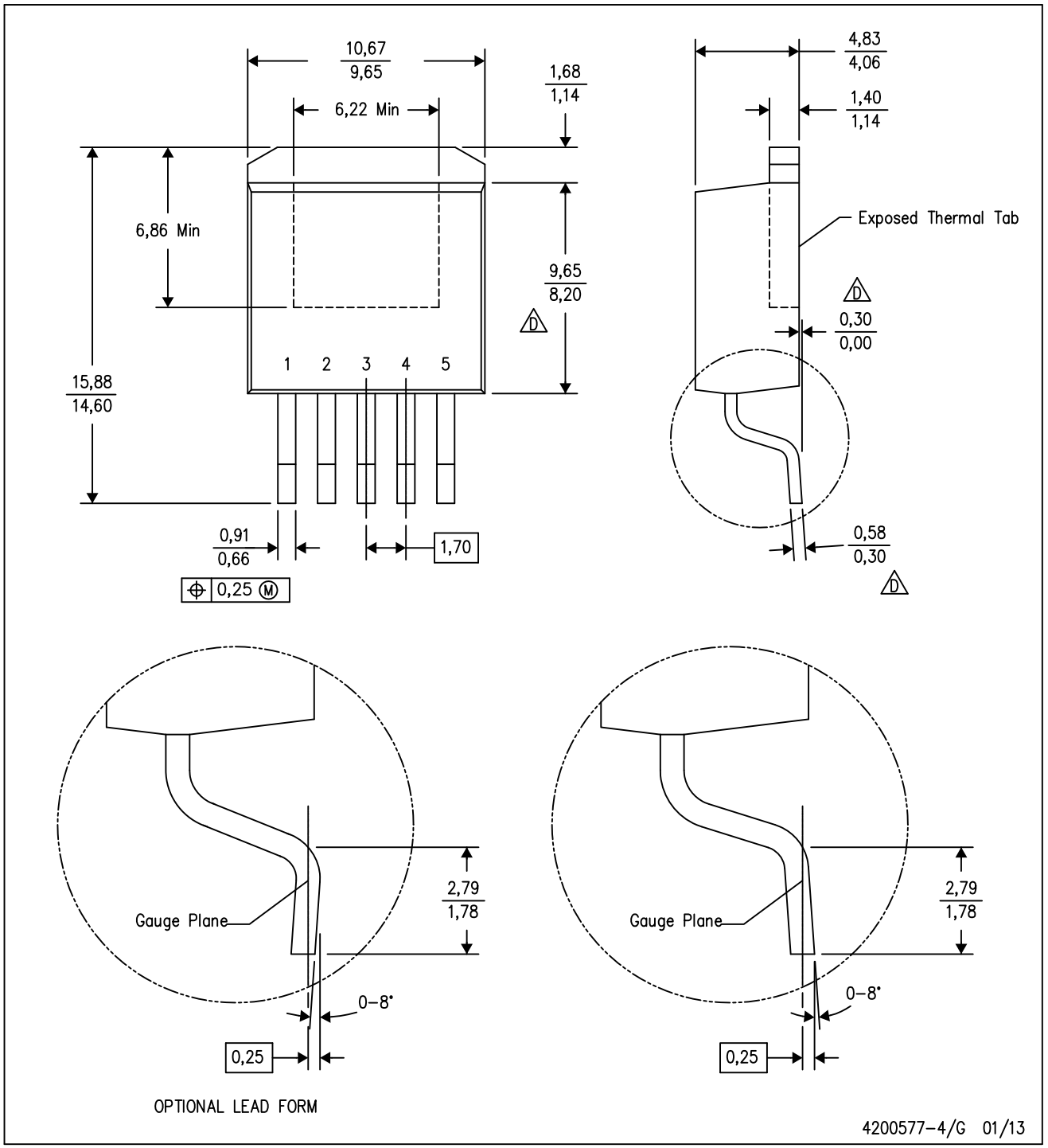
TO-220



LAND PATTERN
NON-SOLDER MASK DEFINED
SCALE:12X

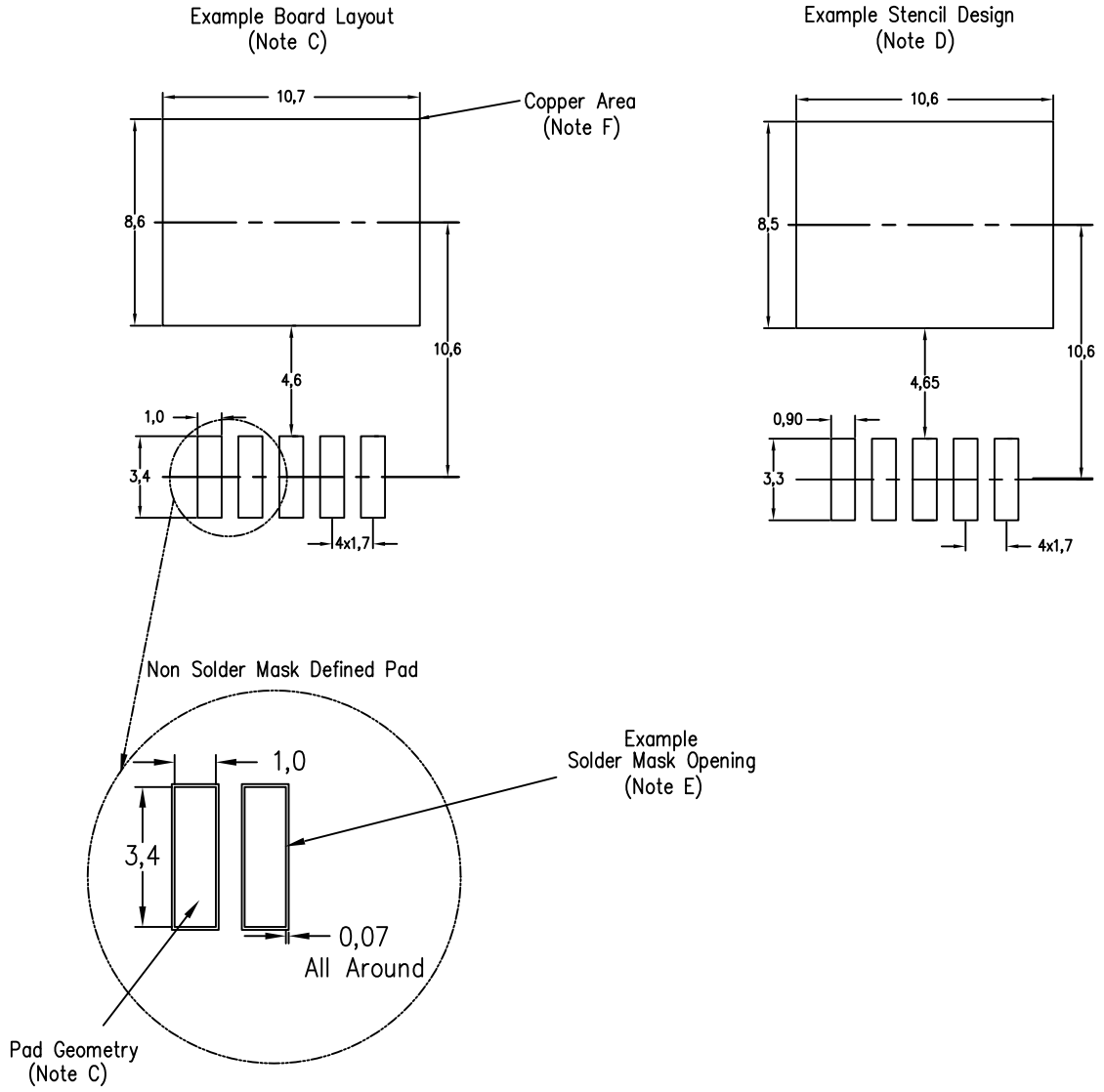
4215009/A 01/2017

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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