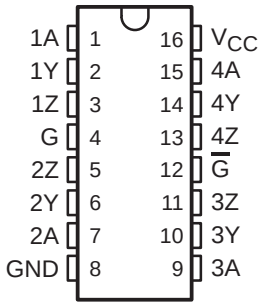
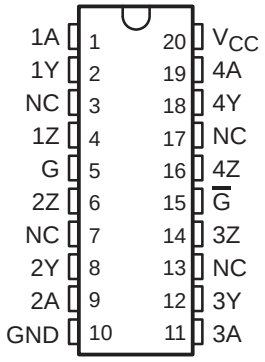
- **Meets or Exceeds ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for 20-MBaud Operation in Both Serial and Parallel Applications**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply-Current Requirements: 55 mA Max**
- **Wide Positive and Negative Input/Output Bus-Voltage Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Logically Interchangeable With SN75172**

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN75ALS172A comprises four line drivers with 3-state differential outputs. They are designed to meet the requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11. This device is optimized for balanced multipoint bus transmission at rates of up to 20 Mbaud. Each driver features wide positive and negative common-mode output voltage ranges, making it suitable for party-line applications in noisy environments.

The SN75ALS172A provides positive- and negative-current limiting and thermal shutdown for protection from line-fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C.

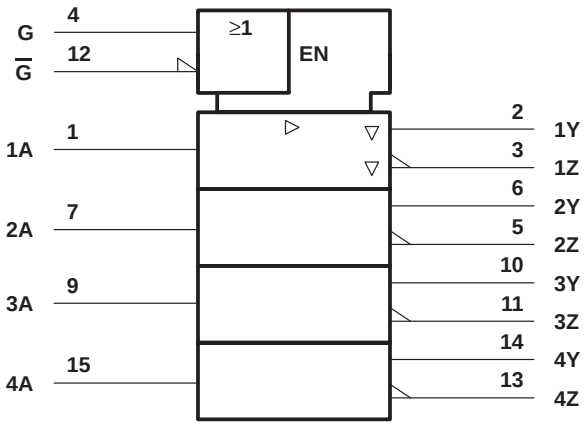
The SN75ALS172A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

INPUT A	ENABLES G	ENABLES $\overline{G}$	OUTPUTS Y	OUTPUTS Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

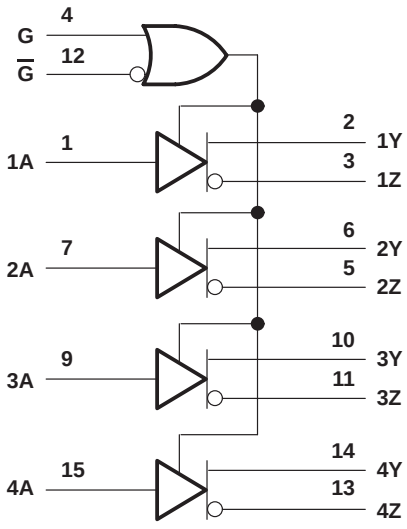
H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

logic symbol†



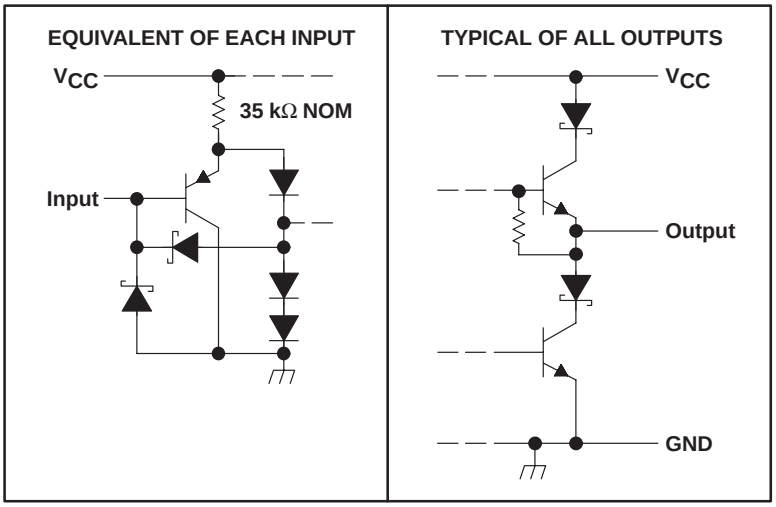
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)



Pin numbers shown are for the N package.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Output voltage range, V_O . . . . . –9 V to 14 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}			12 –7	V
High-level output current, I_{OH}			–60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA					–1.5	V
V_O	Output voltage	I_O = 0			0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0			1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	V_{CC} = 5 V,	R_L = 100 Ω,	See Figure 1	1/2 V_{OD1} or 2‡			V
		R_L = 54 Ω,	See Figure 1		1.5	2.5	5	
$\|V_{OD3}\|$	Differential output voltage	See Note 2			1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage¶	R_L = 54 Ω or 100 Ω,	See Figure 1				3 –1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1				±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = –7 V to 12 V				±100	µA
I_{OZ}	High-impedance-state output current	V_O = –7 V to 12 V					±100	µA
I_{IH}	High-level input current	V_I = 2.7 V					20	µA
I_{IL}	Low-level input current	V_I = 0.4 V					–100	µA
I_{OS}	Short-circuit output current	V_O = –7 V to 12 V					±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled			36	55	mA
			Outputs disabled			15	30	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
NOTE 2: See EIA Standard RS-485, Figure 3-5, Test Termination Measurement 2.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54 Ω,	See Figure 2	9	15	22	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 3	30	45	70	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 4	25	40	65	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 3	10	20	35	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 4	10	30	45	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

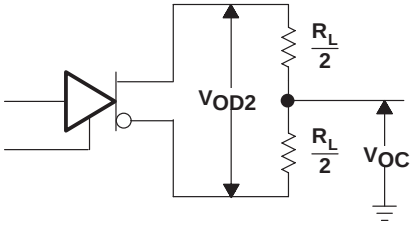
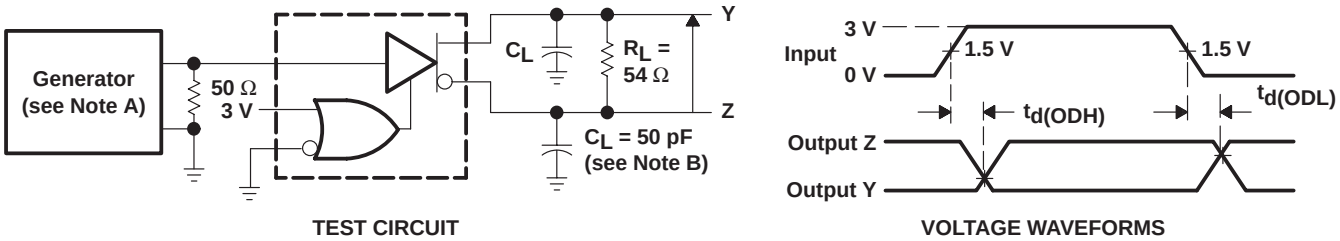
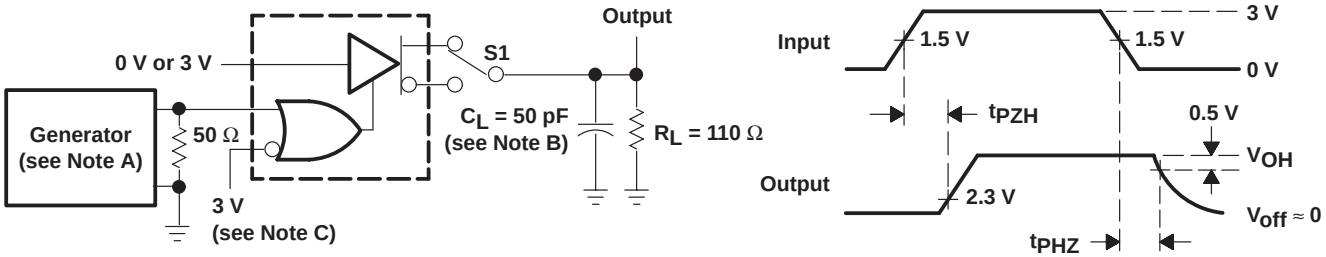


Figure 1. Differential and Common-Mode Output Voltages



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \le 5$ ns, $t_r \le 5$ ns.
B. C_L includes probe and stray capacitance.

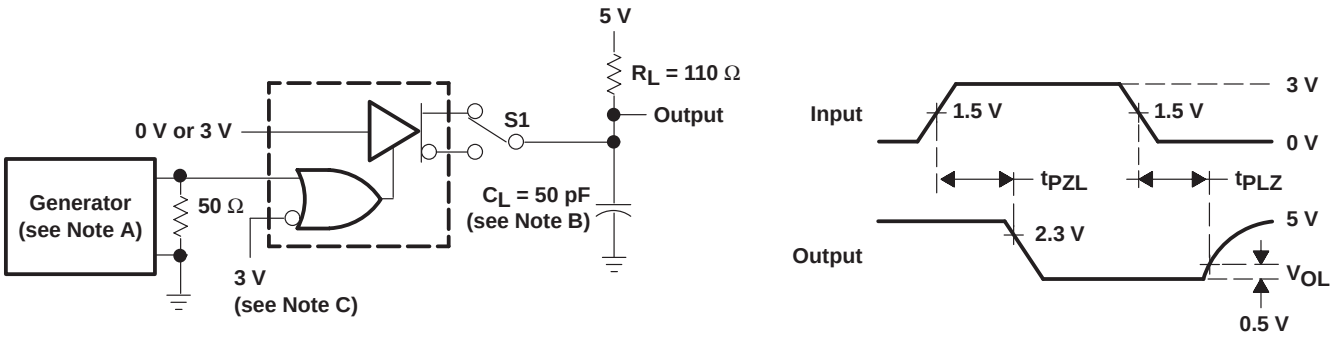
Figure 2. Differential Output Test Circuit and Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \le 5$ ns, $t_r \le 5$ ns.
B. C_L includes probe and stray capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

Figure 3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \le 5$ ns, $t_r \le 5$ ns.
B. C_L includes probe and stray capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

Figure 4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS172ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS172A	Samples
SN75ALS172ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS172A	Samples
SN75ALS172ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS172A	Samples
SN75ALS172AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS172AN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

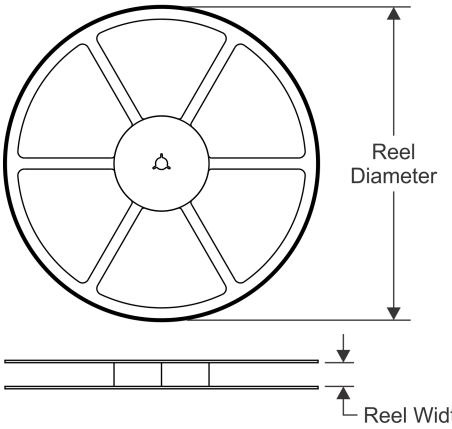
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

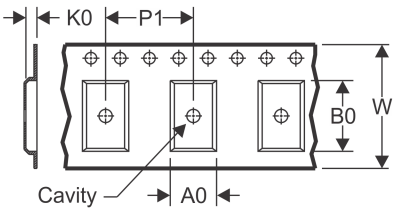
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

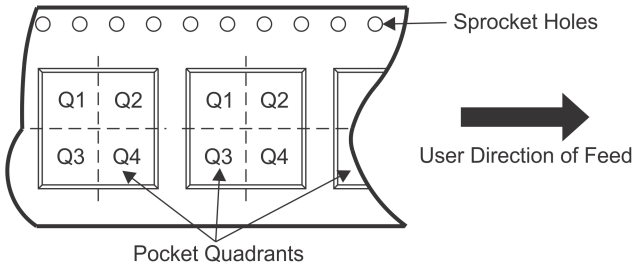


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

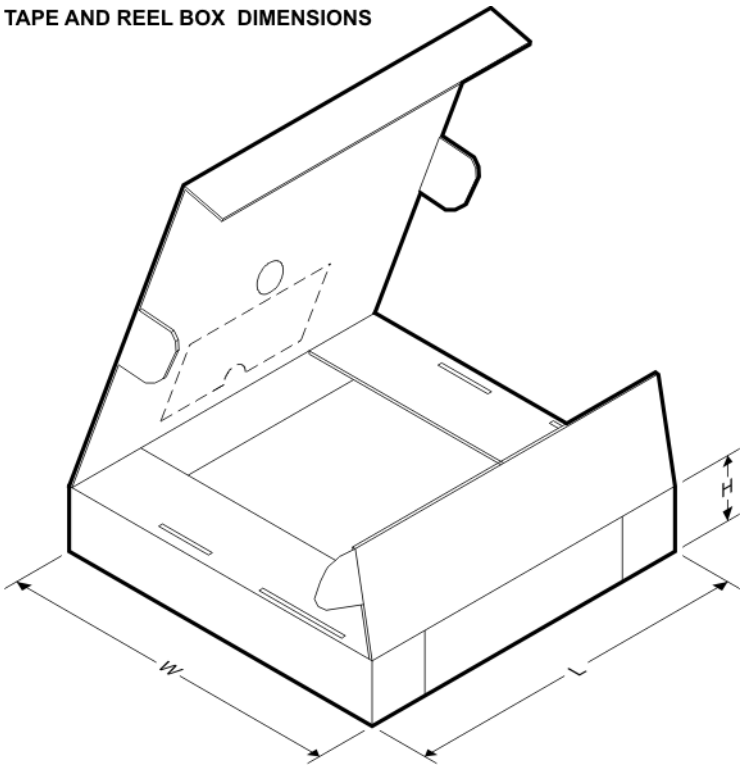
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS172ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75ALS172ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



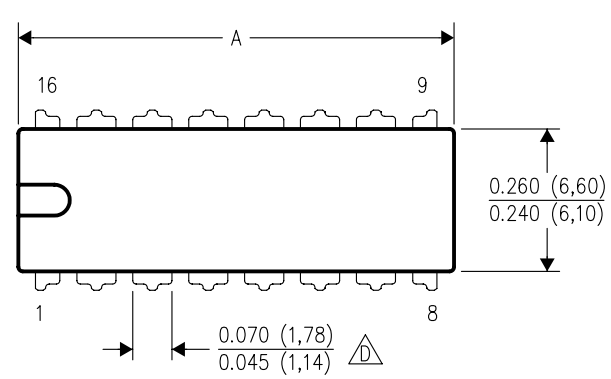
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS172ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN75ALS172ADWR	SOIC	DW	20	2000	367.0	367.0	45.0

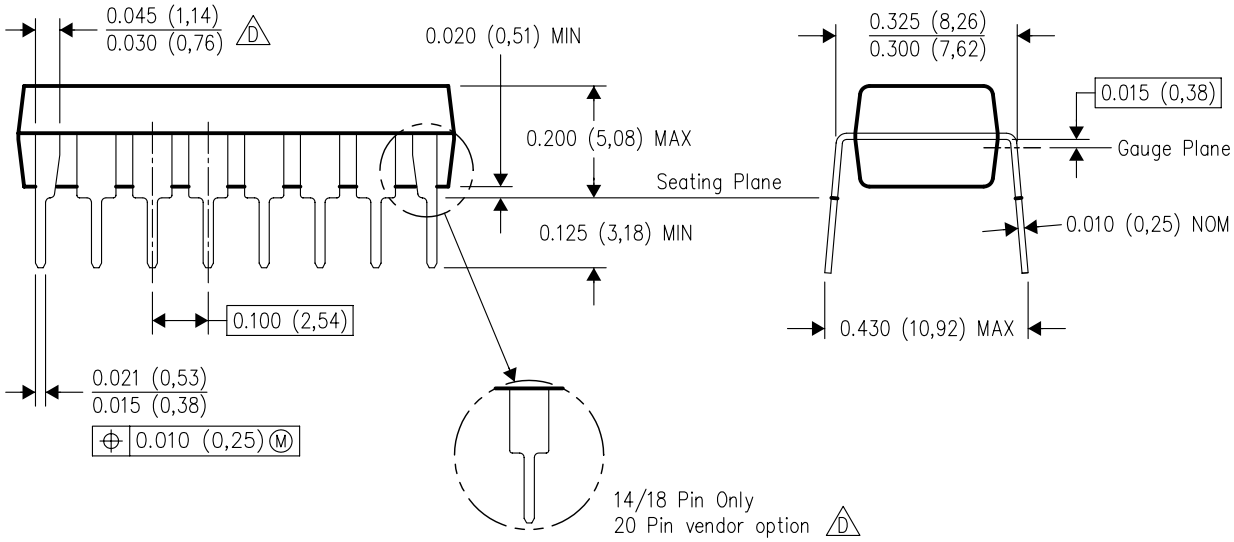
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

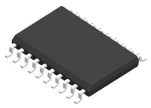


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

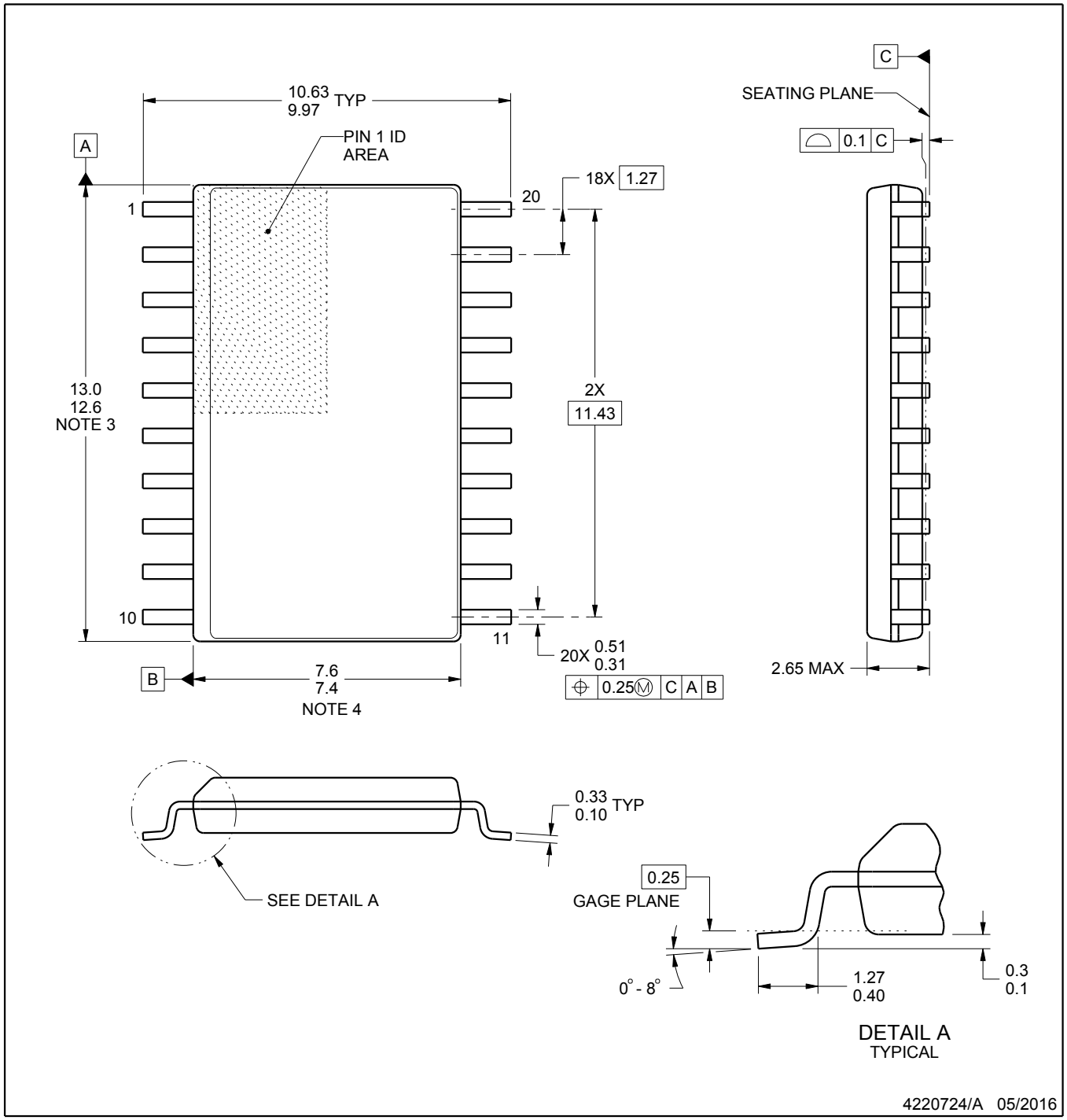


PACKAGE OUTLINE

DW0020A

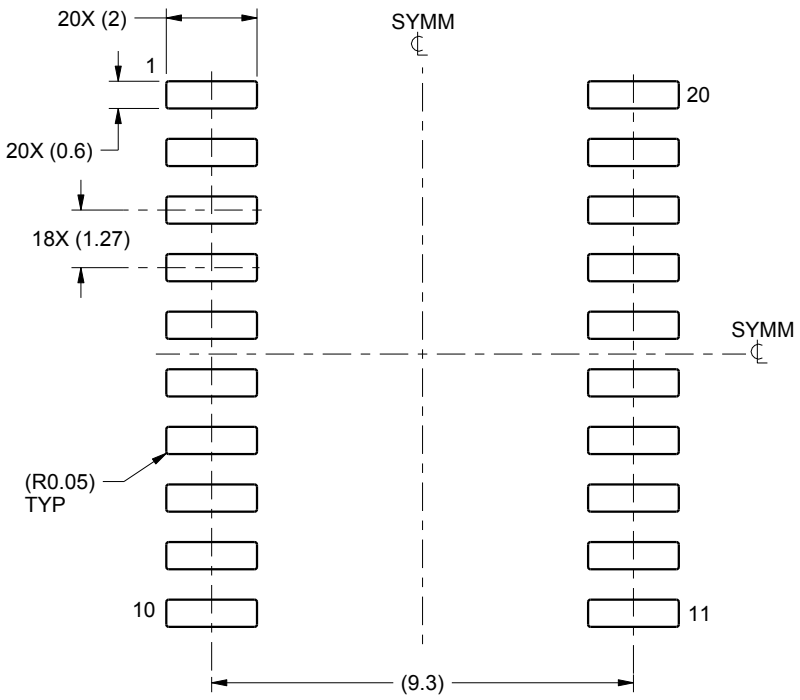
SOIC - 2.65 mm max height

SOIC

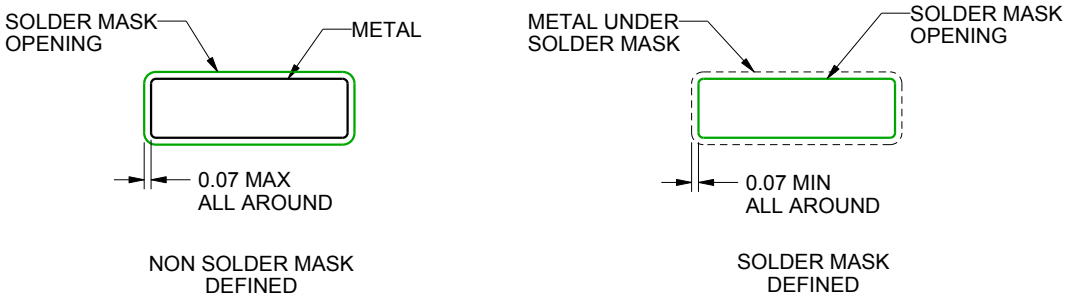


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

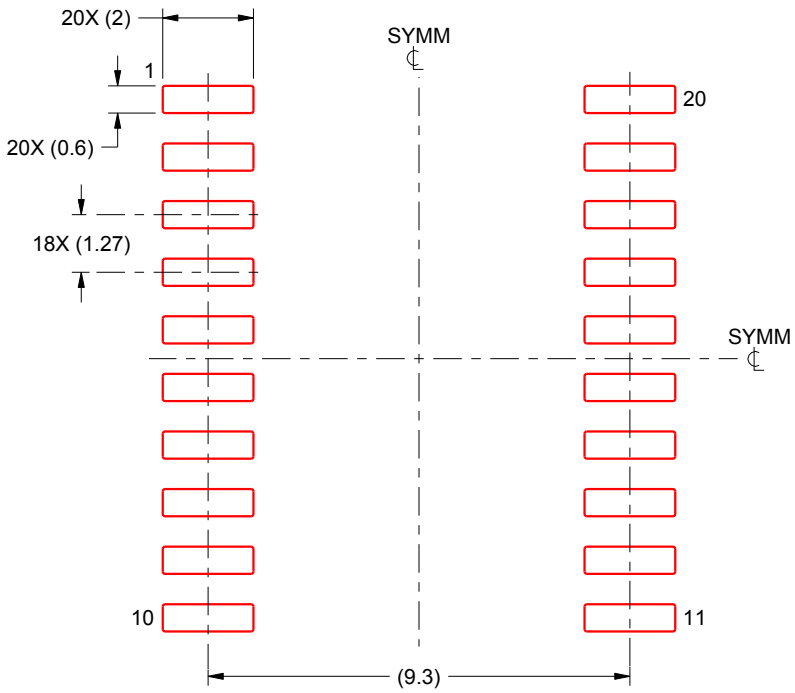


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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