

## 3-A OUTPUT SINGLE SYNCHRONOUS STEP DOWN SWITCHER WITH INTEGRATED FET

Check for Samples: [TPS54327](#)

### FEATURES

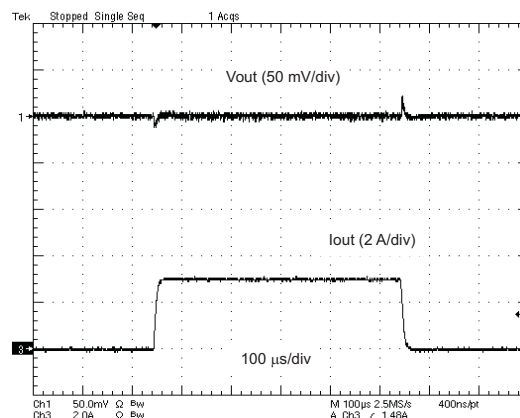
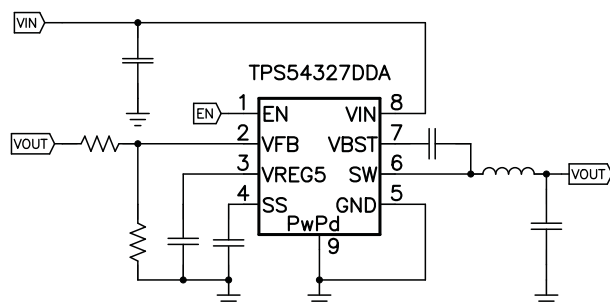
- **D-CAP2™ Mode Enables Fast Transient Response**
- **Low Output Ripple and Allows Ceramic Output Capacitor**
- **Wide  $V_{IN}$  Input Voltage Range: 4.5 V to 18 V**
- **Output Voltage Range: 0.76 V to 7.0 V**
- **Highly Efficient Integrated FET's Optimized for Lower Duty Cycle Applications**
  - 100 m $\Omega$  (High Side) and 70 m $\Omega$  (Low Side)
- **High Efficiency, less than 10  $\mu$ A at shutdown**
- **High Initial Bandgap Reference Accuracy**
- **Adjustable Soft Start**
- **Pre-Biased Soft Start**
- **700-kHz Switching Frequency ( $f_{sw}$ )**
- **Cycle By Cycle Over Current Limit**

### DESCRIPTION

The TPS54327 is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS54327 enables system designers to complete the suite of various end equipment's power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54327 uses the D-CAP2™ mode control which provides a fast transient response with no external compensation components. The TPS54327 also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V  $V_{IN}$  input. The output voltage can be programmed between 0.76 V and 7 V. The device also features an adjustable soft start time. The TPS54327 is available in the 8-pin DDA package and 10-pin DRC, and is designed to operate from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### APPLICATIONS

- **Wide Range of Applications for Low Voltage System**
  - Digital TV Power Supply
  - High Definition Blu-ray Disc™ Players
  - Networking Home Terminal
  - Digital Set Top Box (STB)



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup> <sup>(3)</sup>	ORDERABLE PART NUMBER	PIN	TRANSPORT MEDIA
–45°C to 85°C	DDA	TPS54327DDA	8	Tube
		TPS54327DDAR		Tape and Reel
	DRC	TPS54327DRCT	10	Tape and Reel
		TPS54327DRCR		

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).
- (3) All package options have Cu NIPDAU lead/ball finish.

### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		VALUE		UNIT
		MIN	MAX	
Input voltage range	VIN, EN	–0.3	20	V
	VBST	–0.3	26	V
	VBST (10 ns transient)	–0.3	28	V
	VBST (vs SW)	–0.3	6.5	V
	VFB, SS	–0.3	6.5	V
	SW	–2	20	V
	SW (10 ns transient)	–3	22	V
Output voltage range	VREG5	–0.3	6.5	V
	GND	–0.3	0.3	V
Voltage from GND to thermal pad, V <sub>diff</sub>		–0.2	0.2	V
Electrostatic discharge	Human Body Model (HBM)		2	kV
	Charged Device Model (CDM)		500	V
Operating junction temperature, T <sub>J</sub>		–40	150	°C
Storage temperature, T <sub>stg</sub>		–55	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TPS54327		UNITS
		DDA (8 PINS)	DRC (10-PINS)	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	42.1	43.9	°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance	50.9	55.4	
θ <sub>JB</sub>	Junction-to-board thermal resistance	31.8	18.9	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	5	0.7	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	13.5	19.1	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	7.1	5.3	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com/lit/zip/spra953).

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V <sub>IN</sub>	Supply input voltage range	4.5	18	V	
V <sub>I</sub>	Input voltage range	VBST	-0.1	24	V
		VBST (10 ns transient)	-0.1	27	
		VBST(vs SW)	-0.1	6	
		SS	-0.1	5.7	
		EN	-0.1	18	
		VFB	-0.1	5.5	
		SW	-1.8	18	
		SW (10 ns transient)	-3	21	
	GND	-0.1	0.1		
V <sub>O</sub>	Output voltage range	VREG5	-0.1	5.7	V
I <sub>O</sub>	Output Current range	I <sub>VREG5</sub>	0	10	mA
T <sub>A</sub>	Operating free-air temperature		-40	85	°C
T <sub>J</sub>	Operating junction temperature		-40	150	°C

## ELECTRICAL CHARACTERISTICS

 over operating free-air temperature range V<sub>IN</sub> = 12 V (unless otherwise noted)

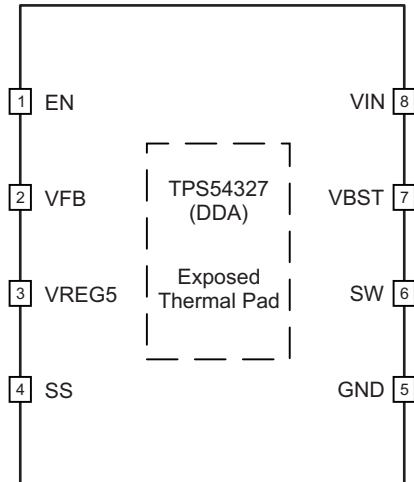
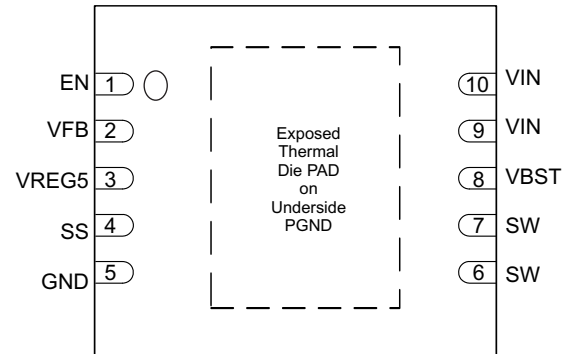
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
I <sub>VIN</sub>	Operating - non-switching supply current	V <sub>IN</sub> current, T <sub>A</sub> = 25°C, EN = 5 V, V <sub>FB</sub> = 0.8 V		800	1200	μA
I <sub>VINSDN</sub>	Shutdown supply current	V <sub>IN</sub> current, T <sub>A</sub> = 25°C, EN = 0 V		1.8	10	μA
<b>LOGIC THRESHOLD</b>						
V <sub>ENH</sub>	EN high-level input voltage	EN	1.6			V
V <sub>ENL</sub>	EN low-level input voltage	EN			0.45	V
<b>V<sub>FB</sub> VOLTAGE AND DISCHARGE RESISTANCE</b>						
V <sub>FBTH</sub>	V <sub>FB</sub> threshold voltage	T <sub>A</sub> = 25°C, V <sub>O</sub> = 1.05 V, continuous mode	749	765	781	mV
I <sub>VFB</sub>	V <sub>FB</sub> input current	V <sub>FB</sub> = 0.8 V, T <sub>A</sub> = 25°C		0	±0.1	μA
<b>V<sub>REG5</sub> OUTPUT</b>						
V <sub>VREG5</sub>	V <sub>REG5</sub> output voltage	T <sub>A</sub> = 25°C, 6.0 V < V <sub>IN</sub> < 18 V, 0 < I <sub>VREG5</sub> < 5 mA	5.2	5.5	5.7	V
V <sub>LN5</sub>	Line regulation	6 V < V <sub>IN</sub> < 18 V, I <sub>VREG5</sub> = 5 mA			25	mV
V <sub>LD5</sub>	Load regulation	0 mA < I <sub>VREG5</sub> < 5 mA			100	mV
I <sub>VREG5</sub>	Output current	V <sub>IN</sub> = 6 V, V <sub>REG5</sub> = 4.0 V, T <sub>A</sub> = 25°C		60		mA
<b>MOSFET</b>						
R <sub>DS(on)h</sub>	High side switch resistance	25°C, V <sub>BST</sub> - SW = 5.5 V		100		mΩ
R <sub>DS(on)l</sub>	Low side switch resistance	25°C		70		mΩ
<b>CURRENT LIMIT</b>						
I <sub>ocd</sub>	Current limit	L out = 1.5 μH <sup>(1)</sup> , T <sub>A</sub> = -20°C to 85°C	3.5	4.2	5.7	A

(1) Not production tested.

**ELECTRICAL CHARACTERISTICS (continued)**over operating free-air temperature range  $V_{IN} = 12\text{ V}$  (unless otherwise noted)

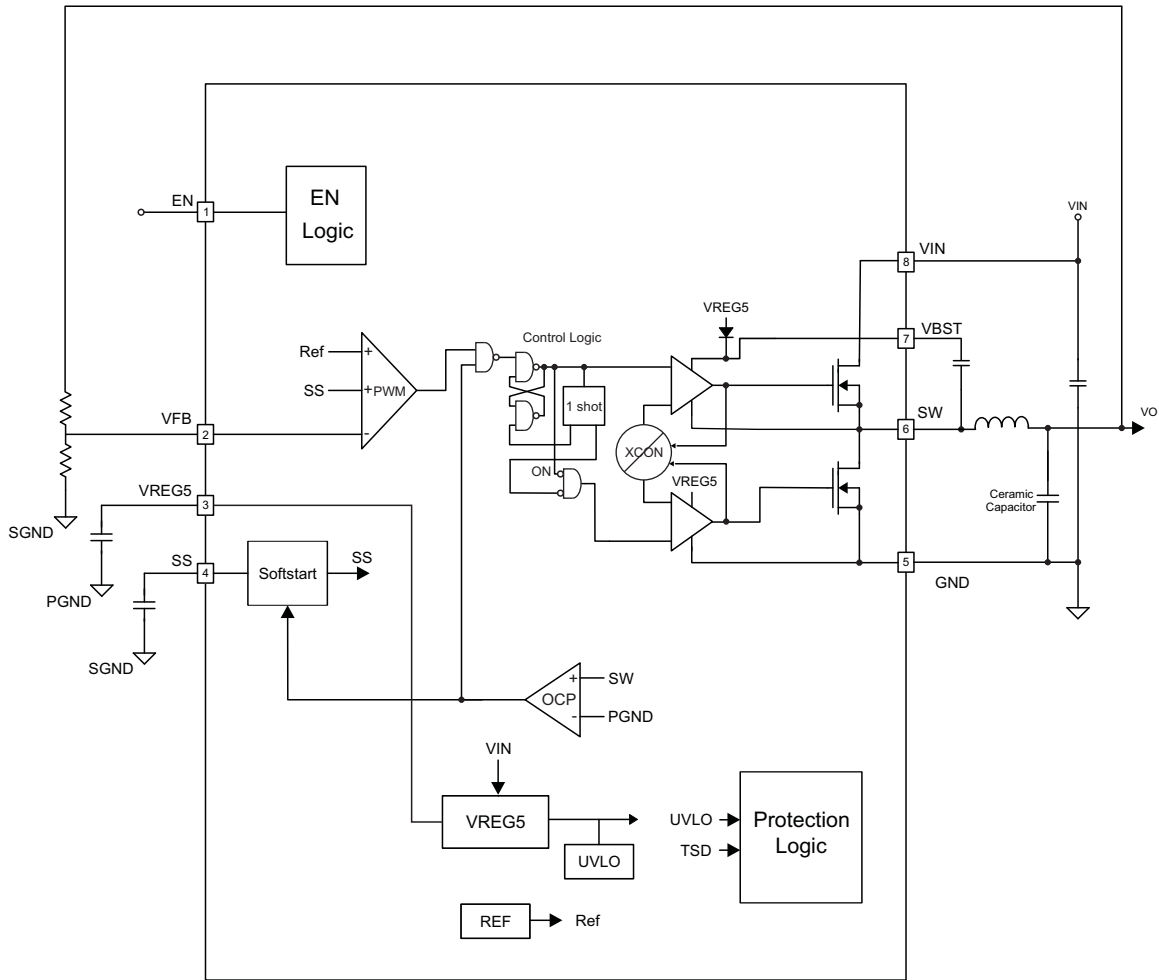
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>THERMAL SHUTDOWN</b>						
$T_{SDN}$	Thermal shutdown threshold	Shutdown temperature <sup>(2)</sup>	165			°C
		Hysteresis <sup>(2)</sup>	30			
<b>ON-TIME TIMER CONTROL</b>						
$t_{ON}$	On time	$V_{IN} = 12\text{ V}$ , $V_O = 1.05\text{ V}$	150			ns
$t_{OFF(MIN)}$	Minimum off time	$T_A = 25^\circ\text{C}$ , $V_{FB} = 0.7\text{ V}$	260	310	ns	
<b>SOFT START</b>						
$I_{SSC}$	SS charge current	$V_{SS} = 0\text{ V}$	1.4	2.0	2.6	μA
$I_{SSD}$	SS discharge current	$V_{SS} = 0.5\text{ V}$	0.05	0.1	mA	
<b>UVLO</b>						
UVLO	UVLO threshold	Wake up $V_{REG5}$ voltage	3.45	3.75	4.05	V
		Hysteresis $V_{REG5}$ voltage	0.17	0.32	0.45	

(2) Not production tested.

**DEVICE INFORMATION**
**DDA PACKAGE  
(TOP VIEW)**

**DRC PACKAGE  
(TOP VIEW)**

**PIN FUNCTIONS**

NAME	PIN		DESCRIPTION
	DDA	DRC	
EN	1	1	Enable input control. Active high.
VFB	2	2	Converter feedback input. Connect to output voltage with feedback resistor divider.
VREG5	3	3	5.5 V power supply output. A capacitor (typical 1 $\mu$ F) should be connected to GND. VREG5 is not active when EN is low.
SS	4	4	Soft-start control. An external capacitor should be connected to GND.
GND	5	5	Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point.
SW	6	6, 7	Switch node connection between high-side NFET and low-side NFET.
VBST	7	8	Supply input for the high-side FET gate drive circuit. Connect 0.1 $\mu$ F capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST.
VIN	8	9, 10	Input voltage supply pin.
Exposed Thermal Pad	Back side		Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND.
		Back side	Thermal pad of the package. PGND power ground return of internal low-side FET. Must be soldered to achieve appropriate dissipation.

FUNCTIONAL BLOCK DIAGRAM



## OVERVIEW

The TPS54327 is a 3-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

## DETAILED DESCRIPTION

### PWM Operation

The main control loop of the TPS54327 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot is set by the converter input voltage, VIN, and the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

### PWM Frequency and Adaptive On-Time Control

TPS54327 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54327 runs with a pseudo-constant frequency of 700 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

### Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 2-μA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in Equation 1. VFB voltage is 0.765 V and SS pin source current is 2 μA.

$$t_{SS}(\text{ms}) = \frac{C6(\text{nF}) \times V_{REF} \times 1.1}{I_{SS}(\mu\text{A})} = \frac{C6(\text{nF}) \times 0.765 \times 1.1}{2} \quad (1)$$

The TPS54327 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage VFB), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (VO) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

### Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by Vin, Vout, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current IOUT. The TPS54327 constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each SW cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching

cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists for 7 consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL limit is returned to the higher value.

There are some important considerations for this type of over-current protection. The load current one half of the peak-to-peak inductor current higher than the over-current threshold. Also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the over current condition is removed, the output voltage will return to the regulated value. This protection is non-latching.

### UVLO Protection

Undervoltage lock out protection (UVLO) monitors the voltage of the  $V_{REG5}$  pin. When the  $V_{REG5}$  voltage is lower than UVLO threshold voltage, the TPS54327 is shut off. This protection is non-latching.

### Thermal Shutdown

TPS54327 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 165°C), the device is shut off. This is non-latch protection.



**TYPICAL CHARACTERISTICS**

V<sub>IN</sub> = 12 V, T<sub>A</sub> = 25°C (unless otherwise noted)

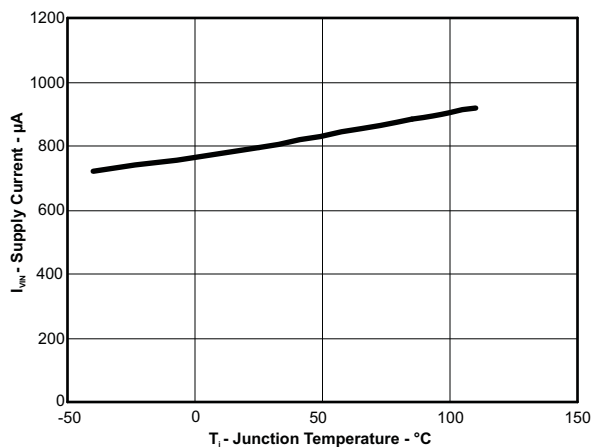


Figure 1. VIN CURRENT vs JUNCTION TEMPERATURE

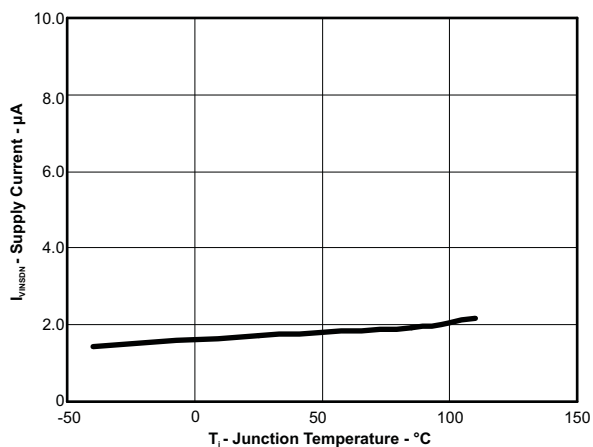


Figure 2. VIN SHUTDOWN CURRENT vs JUNCTION TEMPERATURE

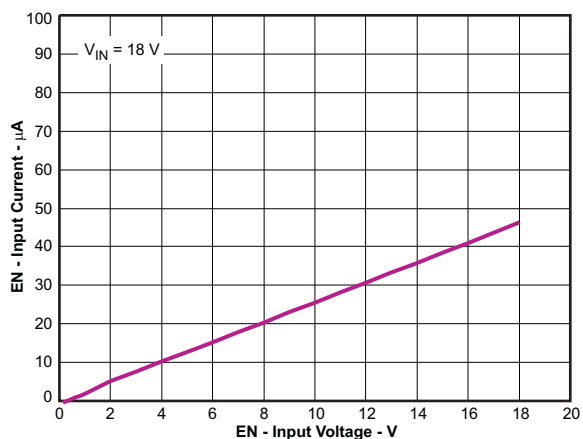


Figure 3. EN CURRENT vs EN VOLTAGE

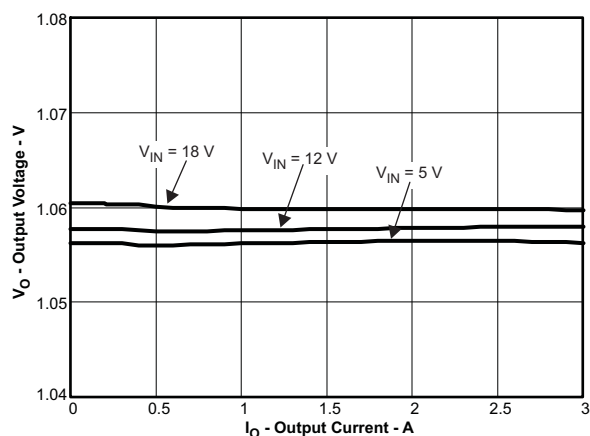


Figure 4. 1.05-V OUTPUT VOLTAGE vs OUTPUT CURRENT

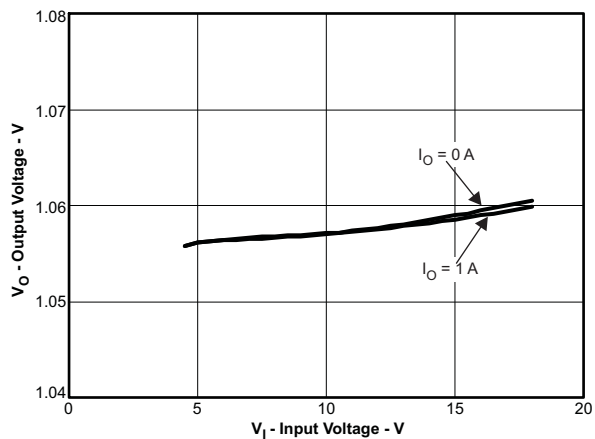


Figure 5. 1.05-V OUTPUT VOLTAGE vs INPUT VOLTAGE

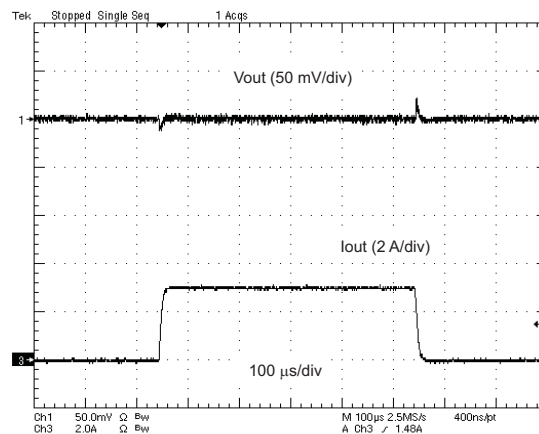


Figure 6. 1.05-V, 0-A to 3-A LOAD TRANSIENT RESPONSE

**TYPICAL CHARACTERISTICS (continued)**

V<sub>IN</sub> = 12 V, T<sub>A</sub> = 25°C (unless otherwise noted)

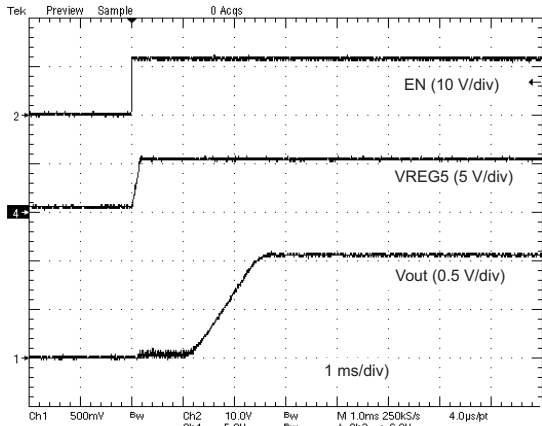


Figure 7. START-UP WAVE FORM

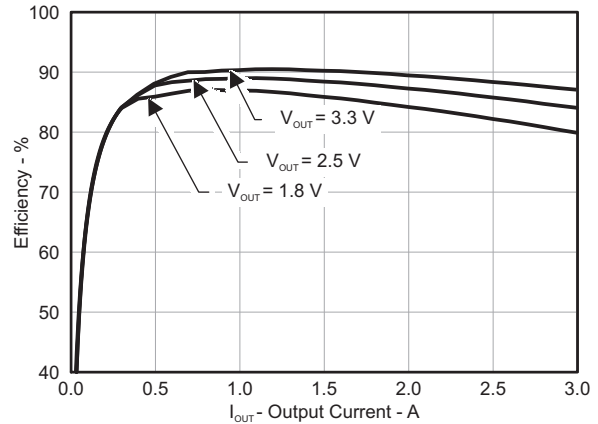


Figure 8. EFFICIENCY vs OUTPUT CURRENT

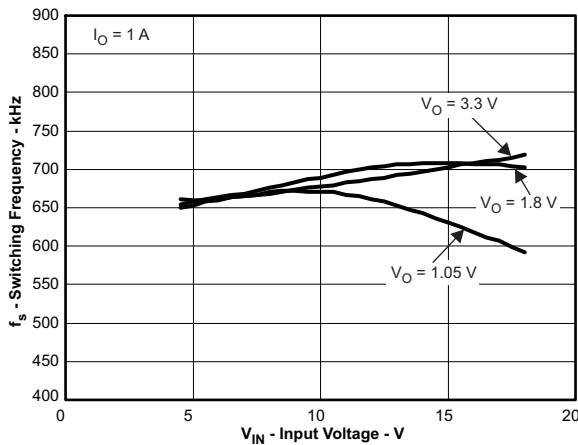


Figure 9. SWITCHING FREQUENCY vs INPUT VOLTAGE

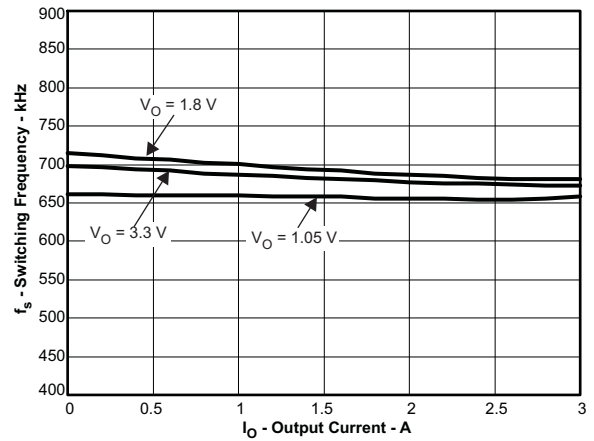


Figure 10. SWITCHING FREQUENCY vs OUTPUT CURRENT

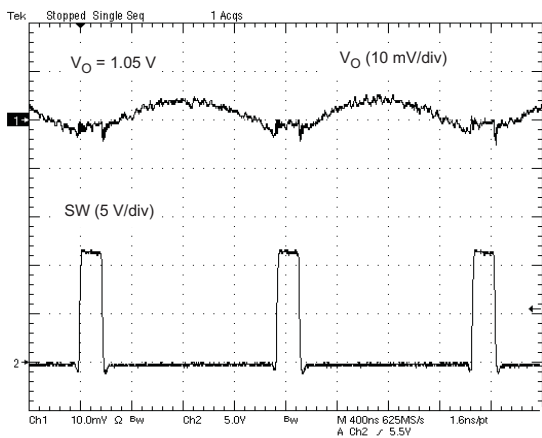


Figure 11. VOLTAGE RIPPLE AT OUTPUT (I<sub>O</sub> = 3 A)

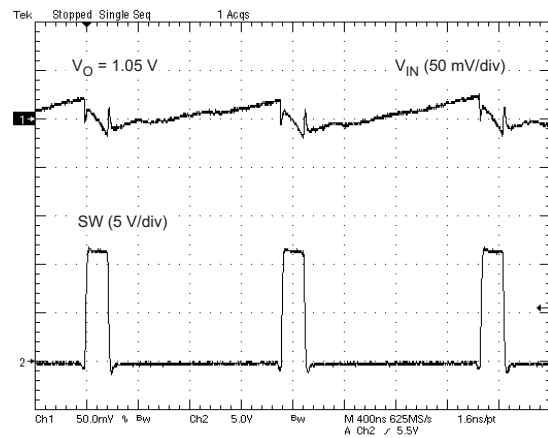


Figure 12. VOLTAGE RIPPLE AT INPUT (I<sub>O</sub> = 3 A)

## DESIGN GUIDE

### Step By Step Design Procedure

To begin the design process, you must know a few application parameters:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

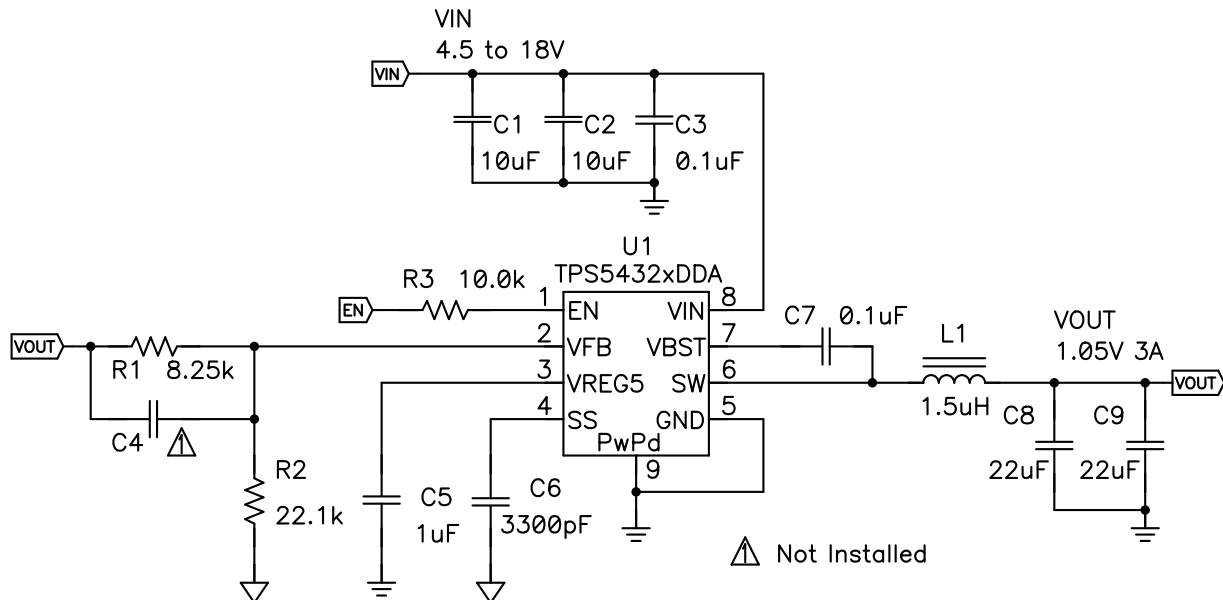


Figure 13. Shows the schematic diagram for this design example.

### Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 2 to calculate  $V_{OUT}$ .

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.765 \times \left( 1 + \frac{R1}{R2} \right) \quad (2)$$

### Output Filter Selection

The output filter used with the TPS54327 is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54327. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a -40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to -20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 1

**Table 1. Recommended Component Values**

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)	L1 (μH)	C8 + C9 (μF)
1	6.81	22.1		1.5	22 - 68
1.05	8.25	22.1		1.5	22 - 68
1.2	12.7	22.1		1.5	22 - 68
1.8	30.1	22.1	5 - 22	2.2	22 - 68
2.5	49.9	22.1	5 - 22	2.2	22 - 68
3.3	73.2	22.1	5 - 22	2.2	22 - 68
5	124	22.1	5 - 22	3.3	22 - 68
6.5	165	22.1	5 - 22	3.3	22 - 68

Since the DC gain is dependent on the output voltage, the required inductor value will increase as the output voltage increases. For higher output voltages above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 4, Equation 5 and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 700 kHz for  $f_{SW}$ .

Use 700 kHz for  $f_{SW}$ . Make sure the chosen inductor is rated for the peak current of Equation 5 and the RMS current of Equation 6.

$$I_{IPP} = \frac{V_{OUT}}{V_{IN(max)}} \times \frac{V_{IN(max)} - V_{OUT}}{L_O \times f_{SW}} \quad (4)$$

$$I_{Ipeak} = I_O + \frac{I_{IPP}}{2} \quad (5)$$

$$I_{Lo(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{IPP}^2} \quad (6)$$

For this design example, the calculated peak current is 3.47 A and the calculated RMS current is 3.01 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54327 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22μF to 68μF. Use Equation 7 to determine the required RMS current rating for the output capacitor.

$$I_{Co(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (7)$$

For this design two TDK C3216X5R0J226M 22μF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is .271A and each output capacitor is rated for 4A.

### Input Capacitor Selection

The TPS54327 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 μF is recommended for the decoupling capacitor. An additional 0.1 μF capacitor from pin 14 to ground is recommended to improve the stability of the over-current limit function. The capacitor voltage rating needs to be greater than the maximum input voltage.

### Bootstrap Capacitor Selection

A 0.1 μF. ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

### VREG5 Capacitor Selection

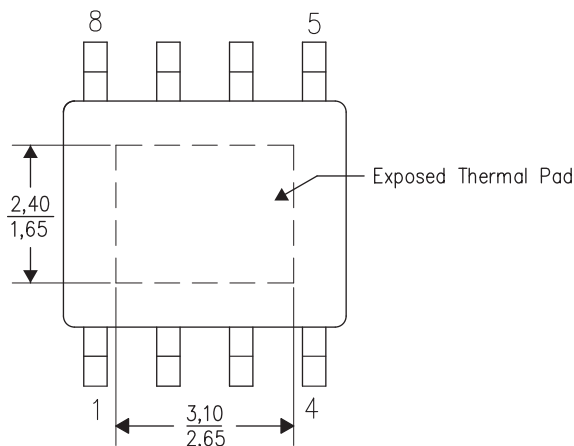
A 1-μF. ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

**THERMAL INFORMATION**

This 8-pin DDA package incorporates an exposed thermal pad that is designed to be directly to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD™ Thermally Enhanced Package, Texas Instruments Literature No. [SLMA002](#) and Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. [SLMA004](#).

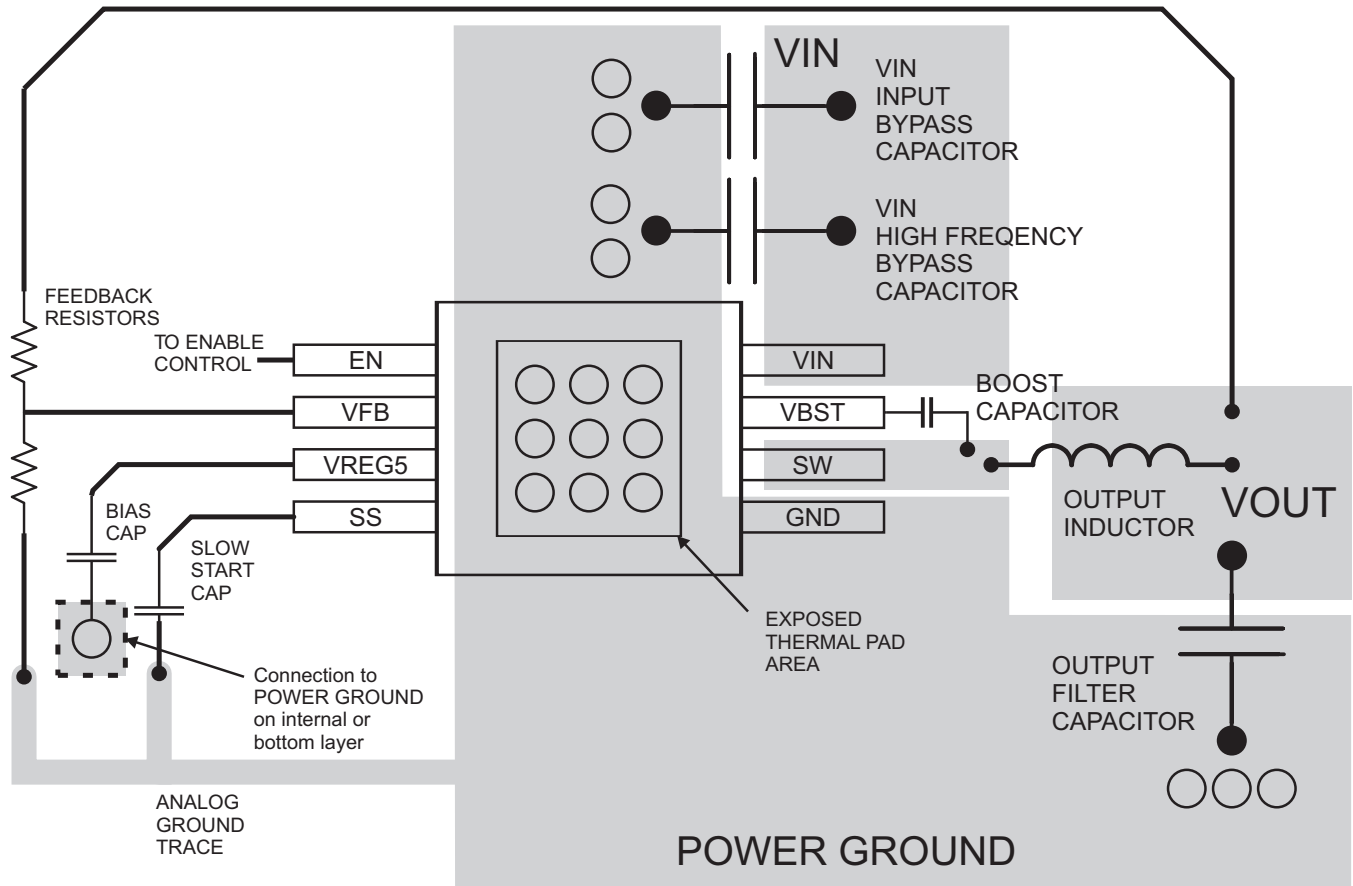
The exposed thermal pad dimensions for this package are shown in the following illustration.



**Figure 14. Thermal Pad Dimensions (Top View)**

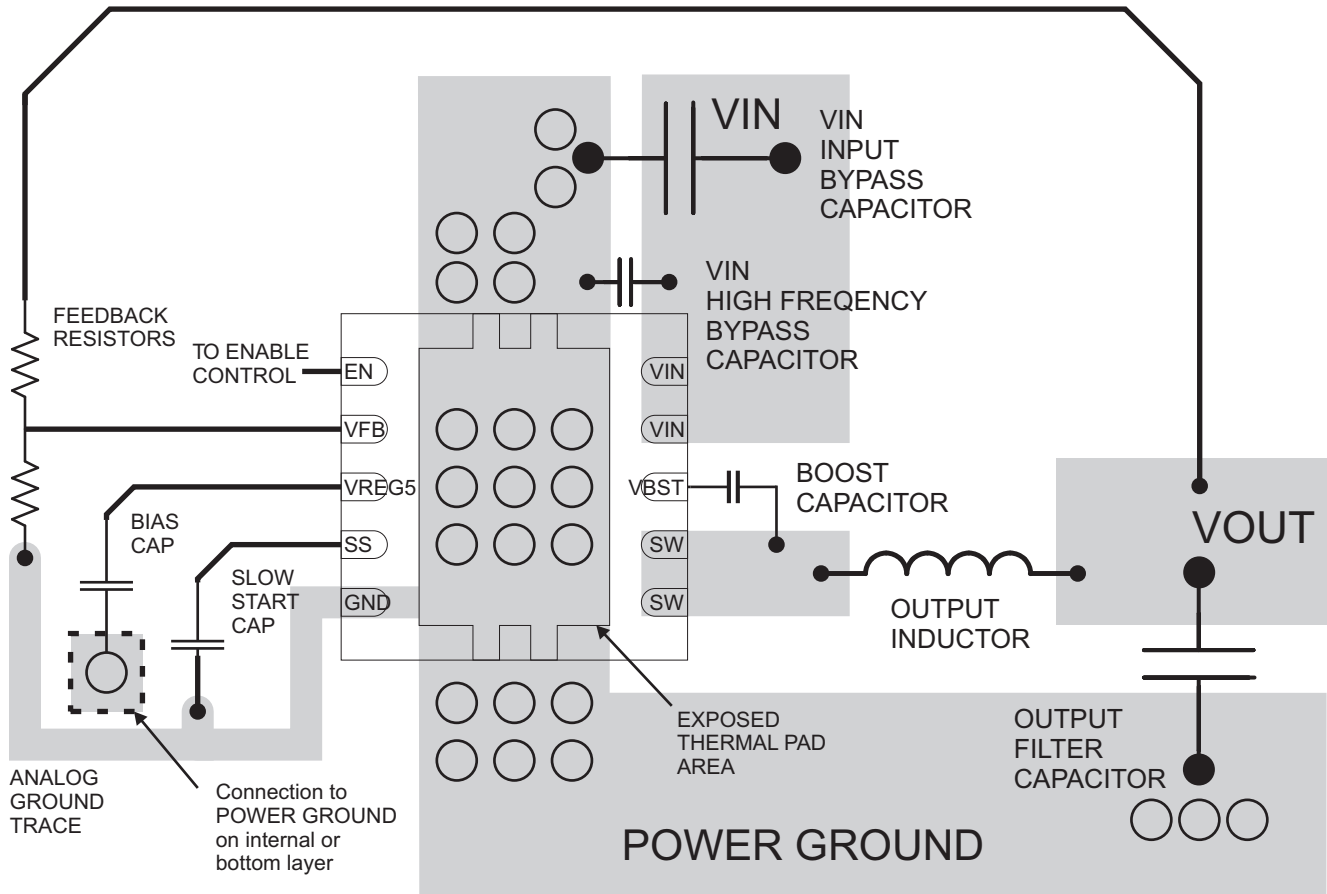
**LAYOUT CONSIDERATIONS**

1. Keep the input switching current loop as small as possible.
2. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
3. Keep analog and non-switching components away from switching components.
4. Make a single point connection from the signal ground to power ground.
5. Do not allow switching current to flow under the device.
6. Keep the pattern lines for VIN and PGND broad.
7. Exposed pad of device must be connected to PGND with solder.
8. VREG5 capacitor should be placed near the device, and connected PGND.
9. Output capacitor should be connected to a broad pattern of the PGND.
10. Voltage feedback loop should be as short as possible, and preferably with ground shield.
11. Lower resistor of the voltage divider which is connected to the VFB pin should be tied to SGND.
12. Providing sufficient via is preferable for VIN, SW and PGND connection.
13. PCB pattern for VIN, SW, and PGND should be as broad as possible.
14. VIN Capacitor should be placed as near as possible to the device.



○ VIA to Ground Plane

**Figure 15. PCB Layout**



○ VIA to Ground Plane

Figure 16. PCB Layout for the DRC Package

## REVISION HISTORY

<b>Changes from Original (November 2010) to Revision A</b>	<b>Page</b>
• Changed the $V_{ENH}$ Min value From: 2 V To: 1.6 V in the Logic Threshold section .....	3
• Changed Pin 6 (SW) Description In the Pin Functions table .....	5
• Changed <a href="#">Equation 1</a> .....	7
• Changed <a href="#">Figure 8</a> .....	9

<b>Changes from Revision A (October 2011) to Revision B</b>	<b>Page</b>
• Removed (SWIFT™) from the data sheet title .....	1
• Added "and 10-pin DRC" to the DESCRIPTION .....	1
• Changed the front page scope image .....	1
• Added the DRC-10 pin Package to the ORDERING INFORMATION table .....	2
• Changed the VBST(vs SW) MAX value From: 6V to 6.5V in the Abs Max Ratings table .....	2
• Changed the VBST(vs SW) MAX value From: 5.7V to 6V in the ROC table .....	3
• Changed UVLO Min Value From: 0.19 V To: 0.17 V .....	4
• Added the DRC-10 Pin package pin out .....	5
• Added Added a conditions statement "VIN = 12 V, TA = 25°C" to the TYPICAL CHARACTERISTICS .....	9
• Changed <a href="#">Figure 6</a> title From: 1.05-V, 50-mA to 2-A LOAD TRANSIENT RESPONSE To: 1.05-V, 0-A to 3-A LOAD TRANSIENT RESPONSE .....	9
• Changed <a href="#">Figure 11</a> Figure Title From: ( $I_O = 2$ A) To: ( $I_O = 3$ A) .....	10
• Changed <a href="#">Figure 12</a> Figure Title From: ( $I_O = 2$ A) To: ( $I_O = 3$ A) .....	10
• Added <a href="#">Figure 16</a> .....	15



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54327DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	54327	<a href="#">Samples</a>
TPS54327DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	54327	<a href="#">Samples</a>
TPS54327DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	54327	<a href="#">Samples</a>
TPS54327DRCT	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	54327	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54327DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS54327DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54327DRCT	SON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54327DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
TPS54327DRCR	SON	DRC	10	3000	367.0	367.0	35.0
TPS54327DRCT	SON	DRC	10	250	210.0	185.0	35.0

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



4202561/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

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- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

DRC (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



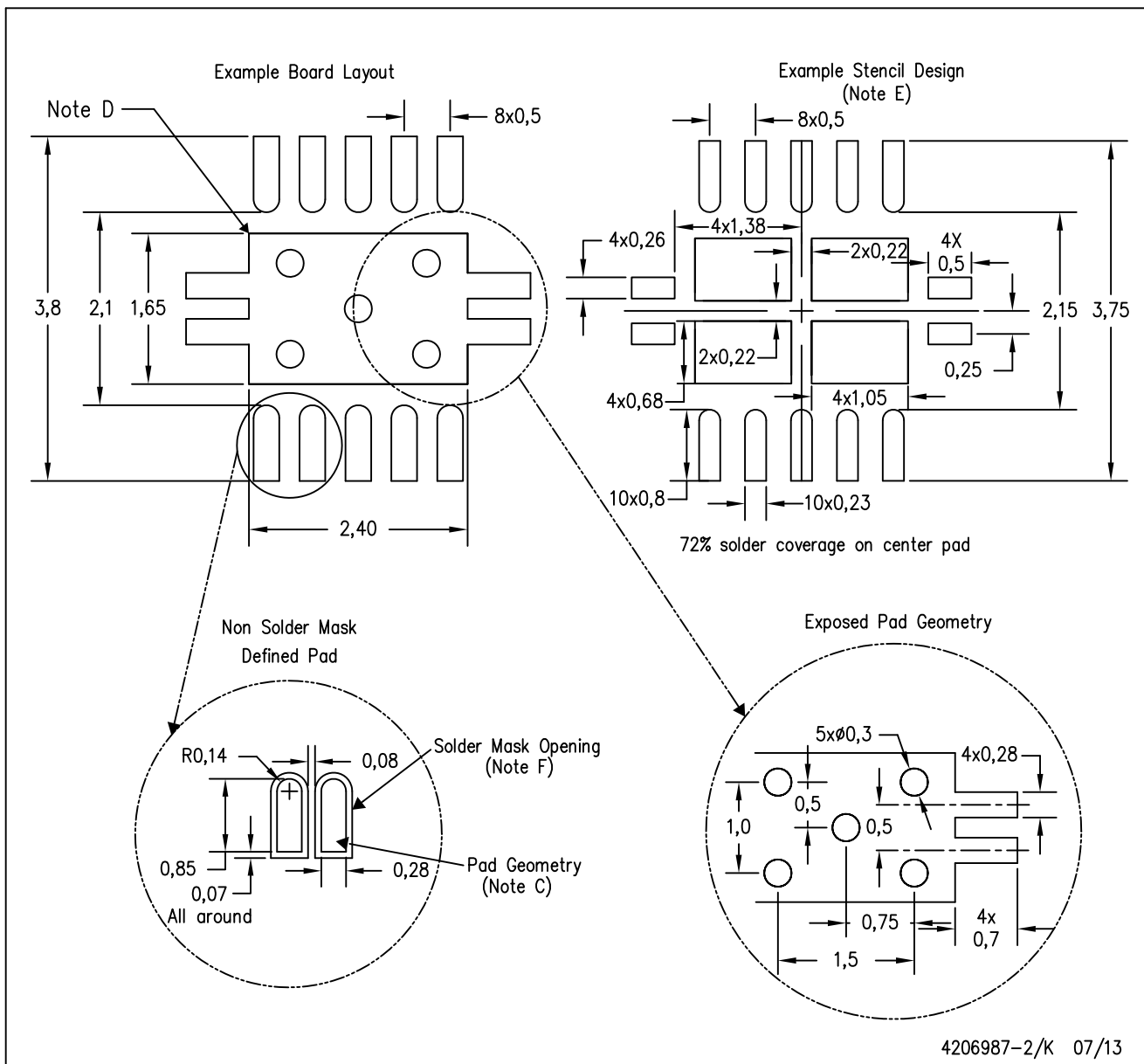
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Small Outline No-Lead (SON) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present





DRC (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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