# 3-Pin Voltage Supervisors with Active-High, Push-Pull Reset

**Check for Samples: TLV810M, TLV810R, TLV810S, TLV810Z**

## FEATURES

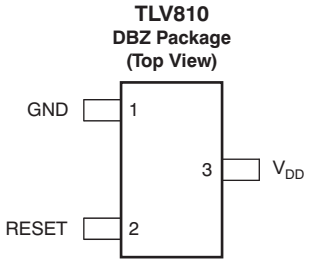
- **3-Pin SOT23 Package**
- **Supply Current: 9 µA (Typical)**
- **Precision Supply Voltage Monitor: 2.5 V, 3 V, 3.3 V, 5 V**
- **Power-On Reset Generator with Fixed Delay Time of 200 ms**
- **Pin-for-Pin Compatible with MAX810**
- **Temperature Range: –40°C to +125°C**
- **Push-Pull, RESET Output**

## APPLICATIONS

- **DSPs, Microcontrollers, and Microprocessors**
- **Wireless Communication Systems**
- **Portable/Battery-Powered Equipment**
- **Programmable Controls**
- **Intelligent Instruments**
- **Industrial Equipment**
- **Notebook and Desktop Computers**
- **Automotive Systems**

### DEVICE FAMILY COMPARISON

| DEVICE | FUNCTION |
|---|---|
| TLV803 | Open-Drain, $\overline{\text{RESET}}$ Output |
| TLV809 | Push-Pull, $\overline{\text{RESET}}$ Output |
| TLV810 | Push-Pull, RESET Output |



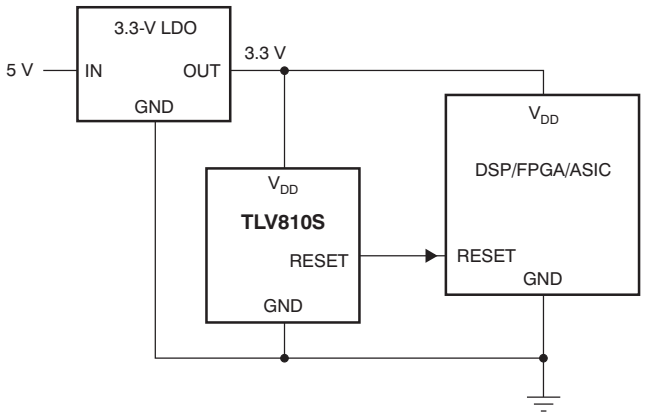

## DESCRIPTION

The TLV810 family of supervisory circuits provides circuit initialization and timing supervision, primarily for DSPs and processor-based systems.

During power-on, RESET is asserted when the supply voltage ($V_{DD}$) becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors $V_{DD}$ and keeps RESET active as long as $V_{DD}$ remains below the threshold voltage $V_{IT}$. An internal timer delays the return of the output to the inactive state (low) to ensure proper system reset. The delay time ($t_{d(typ)}$ = 200 ms) starts after $V_{DD}$ has risen above the threshold voltage, $V_{IT}$. When the supply voltage drops below the $V_{IT}$ threshold voltage, the output becomes active (high) again. No external components are required. All the devices in this family have a fixed sense-threshold voltage ($V_{IT}$) set by an internal voltage divider.

The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 3-pin SOT-23 package. The TLV810 devices are characterized for operation over a temperature range of –40°C to +125°C.

### TYPICAL APPLICATION



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION(1)

| PRODUCT | THRESHOLD VOLTAGE | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED OPERATING TEMPERATURE | PACKAGE MARKING | ORDERING INFORMATION | TRANSPORT MEDIA, QUANTITY |
|---|---|---|---|---|---|---|---|
| TLV810Z | 2.25 V | SOT23-3 | DBZ | –40°C to +125°C | VOVQ | TLV810ZDBZR | Tape and Reel, 3000 |
| | | | | | | TLV810ZDBZT | Tape and Reel, 250 |
| TLV810R | 2.64 V | SOT23-3 | DBZ | –40°C to +125°C | VOWQ | TLV810RDBZR | Tape and Reel, 3000 |
| | | | | | | TLV810RDBZT | Tape and Reel, 250 |
| TLV810S | 2.93 V | SOT23-3 | DBZ | –40°C to +125°C | VOXQ | TLV810SDBZR | Tape and Reel, 3000 |
| | | | | | | TLV810SDBZT | Tape and Reel, 250 |
| TLV810M | 4.38 V | SOT23-3 | DBZ | –40°C to +125°C | VOYQ | TLV810MDBZR | Tape and Reel, 3000 |
| | | | | | | TLV810MDBZT | Tape and Reel, 250 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or visit the device product folders at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

| | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Voltage | $V_{DD}$ (2) | 0 | 7 | V |
| | All other pins (2) | –0.3 | 7 | V |
| Current | Maximum low output current, $I_{OL}$ | | 5 | mA |
| | Maximum high output current, $I_{OH}$ | | –5 | mA |
| | Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{DD}$) | | ±20 | mA |
| | Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{DD}$) | | ±20 | mA |
| Temperature | Operating free-air temperature range, $T_A$ | –40 | +125 | °C |
| | Storage temperature range, $T_{stg}$ | –65 | +150 | °C |
| | Soldering temperature | | +260 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation the device should not be operated at 7 V for more than t = 1000h continuously.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | TLV810 DBZ 3 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 286.9 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 105.6 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 124.4 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 25.8 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 107.9 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | — | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## RECOMMENDED OPERATING CONDITIONS

At specified temperature range (unless otherwise noted).

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.1 | 6 | V |
| $T_A$ | Operating free-air temperature range | –40 | +125 | °C |

## ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted).

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | | $V_{DD}$ = 2.0 V to 6 V, $I_{OH}$ = –500 µA | $V_{DD}$ – 0.2 | | | V |
| | | | $V_{DD}$ = 3.3 V, $I_{OH}$ = –2 mA | $V_{DD}$ – 0.4 | | | |
| | | | $V_{DD}$ = 6 V, $I_{OH}$ = –4 mA, $T_A$ = –40°C to +85°C | $V_{DD}$ – 0.4 | | | |
| | | | $V_{DD}$ = 6 V, $I_{OH}$ = –4 mA, $T_A$ = +85°C to +125°C | $V_{DD}$ – 0.5 | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{DD}$ = 2.5 V to 6 V, $I_{OL}$ = 500 µA | | | 0.2 | V |
| | | | $V_{DD}$ = 3.3 V, $I_{OL}$ = 2 mA | | | 0.4 | |
| | | | $V_{DD}$ = 6 V, $I_{OL}$ = 4 mA | | | 0.4 | |
| | Power-up reset voltage[1] | | $V_{OH} \geq V_{DD}$ – 0.2 V, $I_{OH}$ = –50 µA | 1.1 | | | V |
| $V_{IT–}$ | Negative-going input threshold voltage[2] | TLV810Z | | 2.20 | 2.25 | 2.30 | V |
| | | TLV810R | | 2.58 | 2.64 | 2.70 | |
| | | TLV810S | | 2.87 | 2.93 | 2.99 | |
| | | TLV810M | | 4.28 | 4.38 | 4.48 | |
| $V_{hys}$ | Hysteresis | TLV810Z | $I_{OH}$ = –50 µA, $T_A$ = +25°C | | 30 | | mV |
| | | TLV810R | | | 35 | | |
| | | TLV810S | | | 40 | | |
| | | TLV810M | | | 60 | | |
| $I_{DD}$ | Supply current | | $V_{DD}$ = 2 V, output unconnected | | 9 | 15 | µA |
| | | | $V_{DD}$ = 6 V, output unconnected | | 20 | 30 | |

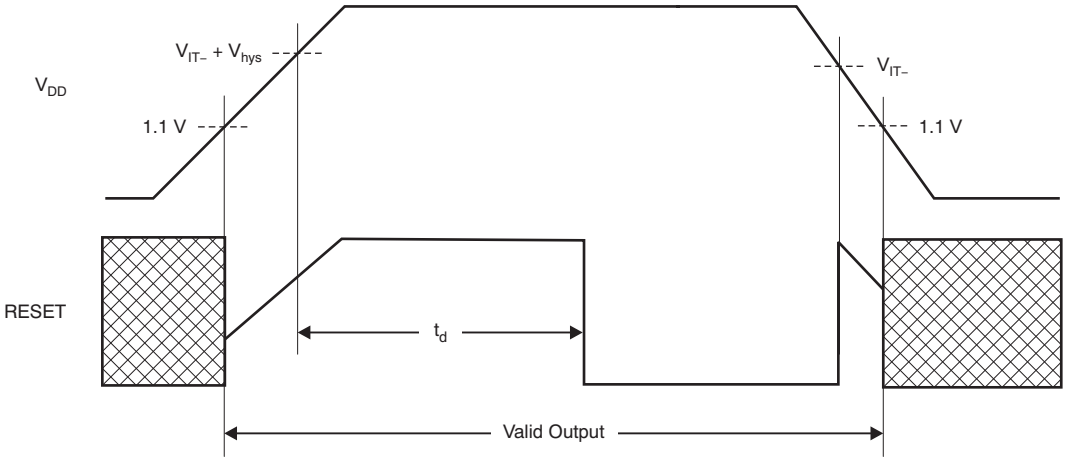
(1) The lowest supply voltage at which RESET becomes valid. $t_{r,\ VDD} \leq 66.7$ ms/V.
(2) To ensure best stability of the threshold voltage, a bypass capacitor ( 0.1-µF ceramic) should be placed near the supply terminals.

## SWITCHING CHARACTERISTICS

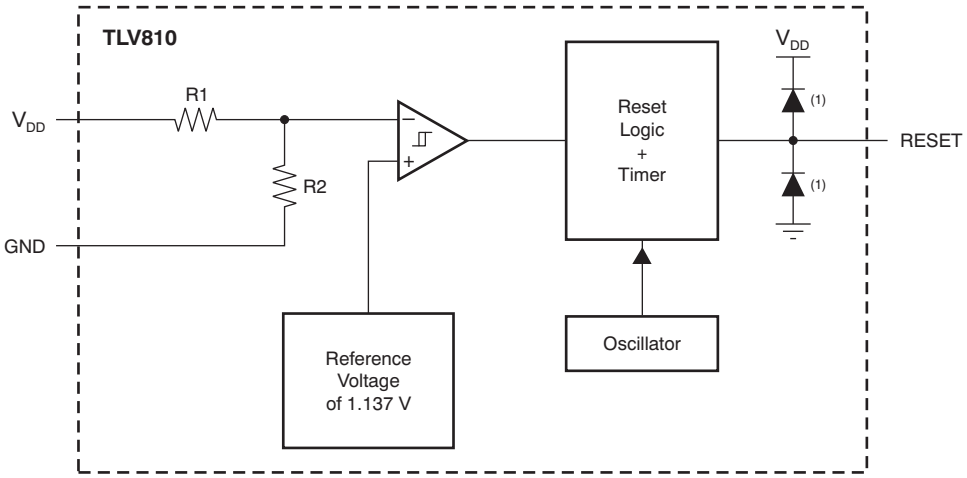
At $T_A$ = +25°C, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_w$ | Pulse width at $V_{DD}$ | $V_{DD}$ = 1.08 $V_{IT-}$ to 0.92 $V_{IT-}$ | | 1 | | µs |
| $t_d$ | Delay time | $V_{DD} \geq V_{IT-}$ + 0.2 V; see Timing Diagram | 120 | 200 | 280 | ms |

## TIMING DIAGRAM




## FUNCTIONAL BLOCK DIAGRAM




(1) Parasitic diode.

## TYPICAL CHARACTERISTICS

At $T_A$ = +25°C, $V_{IT-}$ = 4.38 V, and $V_{DD}$ = 5.0 V, unless otherwise noted.

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

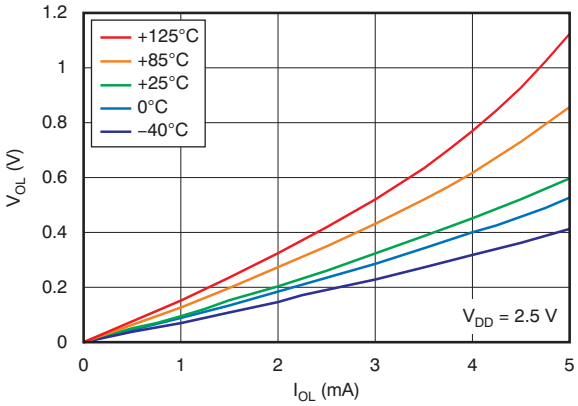



**Figure 1.**

**SUPPLY CURRENT vs SUPPLY VOLTAGE**

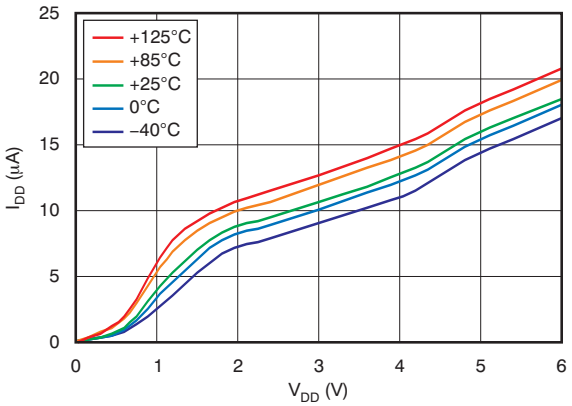



**Figure 2.**

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

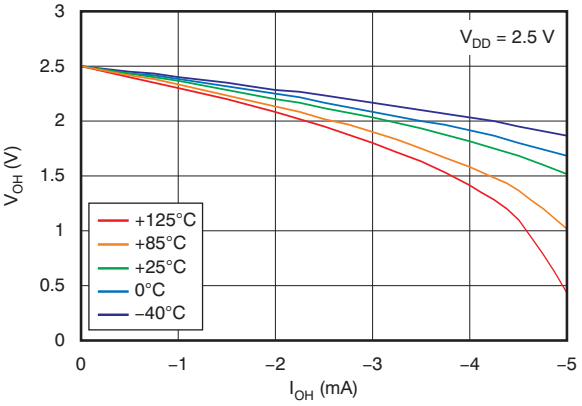



**Figure 3.**

**NORMALIZED INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE AT $V_{DD}$**

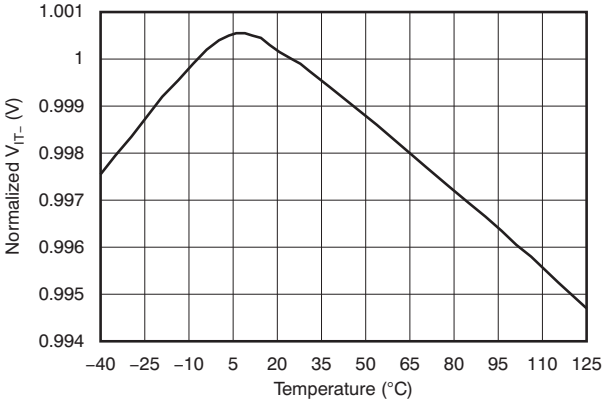



**Figure 4.**

**MINIMUM PULSE DURATION AT $V_{DD}$ vs $V_{DD}$ THRESHOLD OVERDRIVE VOLTAGE (TLV810M)**

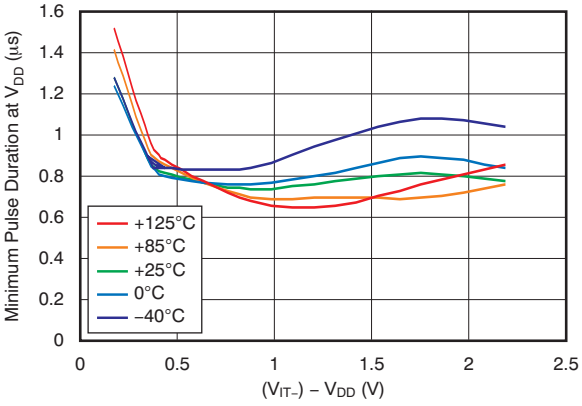



**Figure 5.**

**DELAY TIME vs TEMPERATURE**

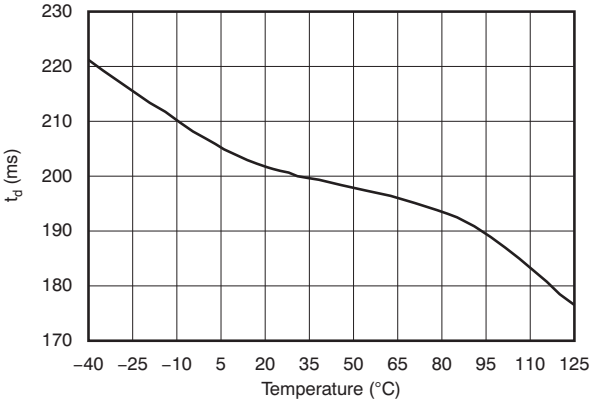



**Figure 6.**

## APPLICATION INFORMATION

### $V_{DD}$ TRANSIENT REJECTION

The TLV810 has built-in rejection of fast transients on the $V_{DD}$ pin. The rejection of transients depends on both the duration and the amplitude of the transient. The amplitude of the transient is measured from the bottom of the transient to the negative threshold voltage of the TLV810, as shown in Figure 7.

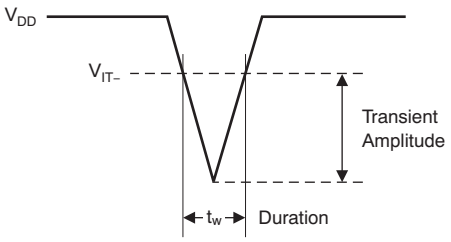



**Figure 7. Voltage Transient Measurement**

The TLV810 does not respond to transients that are fast duration/low amplitude or long duration/small amplitude. Figure 5 shows the relationship between the transient amplitude and the duration needed to trigger a reset. Any combination of duration and amplitude above the curve generates a reset signal.

### RESET DURING POWER UP/DOWN

The TLV810 output is valid when $V_{DD}$ is greater than 1.1 V. When $V_{DD}$ is less than 1.1 V, the output is undefined. Figure 8 shows a typical waveform for the power-up sequence.

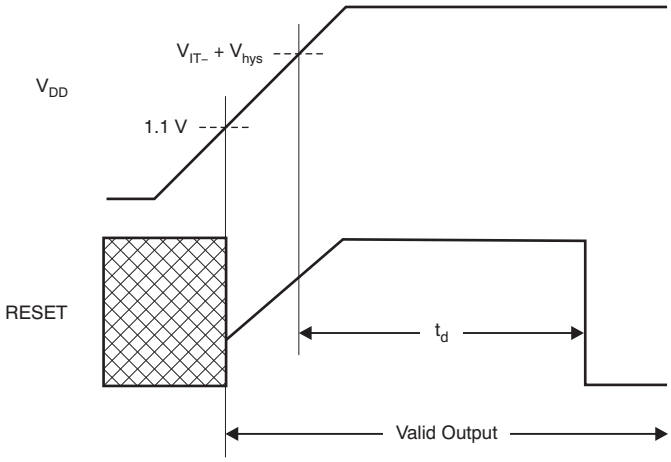



**Figure 8. Power-Up Response**

## BIDIRECTIONAL RESET PINS

Some microcontrollers have bidirectional reset pins that act as both inputs and outputs. In a situation where both the TLV810 and the microcontroller are attempting to drive the RESET line, a series resistor should be placed between the output of the TLV810 and the RESET pin of the microcontroller to protect against excessive current flow. Figure 9 shows the connection of the TLV810 to a microcontroller using a series resistor to drive a bidirectional RESET line.

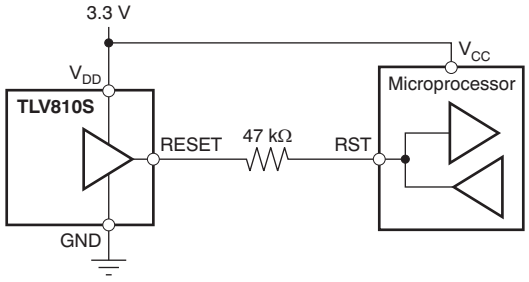



**Figure 9. Connection to Bidirectional Reset Pin**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV810MDBZR | ACTIVE | SOT-23 | DBZ | 3 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VOYQ | Samples |
| TLV810MDBZT | ACTIVE | SOT-23 | DBZ | 3 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VOYQ | Samples |
| TLV810RDBZR | ACTIVE | SOT-23 | DBZ | 3 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VOWQ | Samples |
| TLV810RDBZT | ACTIVE | SOT-23 | DBZ | 3 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VOWQ | Samples |
| TLV810SDBZR | ACTIVE | SOT-23 | DBZ | 3 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VOXQ | Samples |
| TLV810SDBZT | ACTIVE | SOT-23 | DBZ | 3 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VOXQ | Samples |
| TLV810ZDBZR | ACTIVE | SOT-23 | DBZ | 3 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VOVQ | Samples |
| TLV810ZDBZT | ACTIVE | SOT-23 | DBZ | 3 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VOVQ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

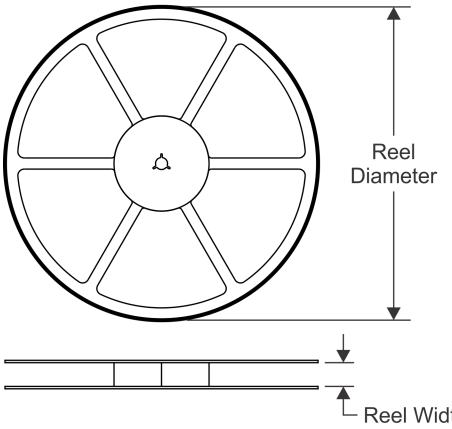
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

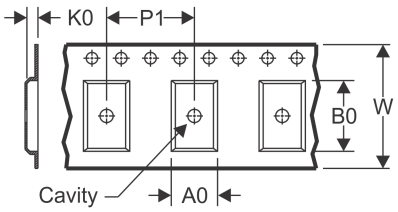
**(4)** Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

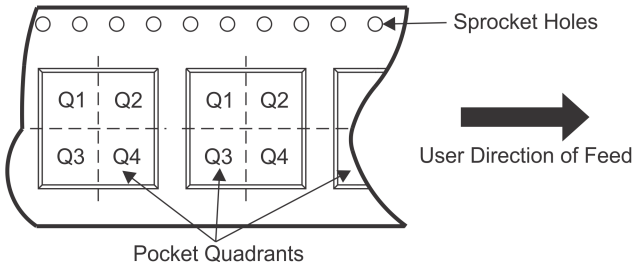



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

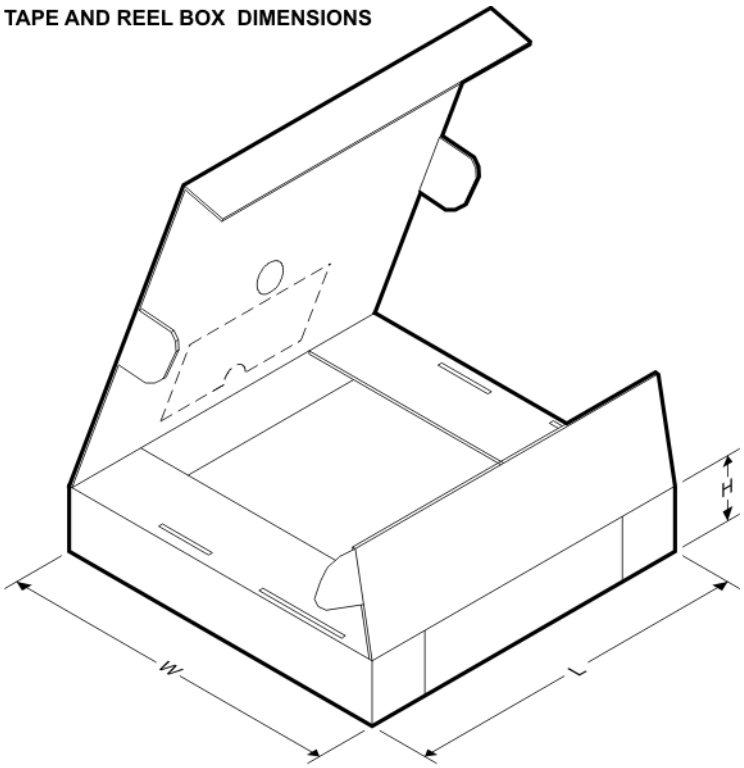
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV810MDBZR | SOT-23 | DBZ | 3 | 3000 | 179.0 | 8.4 | 3.15 | 2.95 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV810MDBZT | SOT-23 | DBZ | 3 | 250 | 179.0 | 8.4 | 3.15 | 2.95 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV810RDBZR | SOT-23 | DBZ | 3 | 3000 | 179.0 | 8.4 | 3.15 | 2.95 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV810RDBZT | SOT-23 | DBZ | 3 | 250 | 179.0 | 8.4 | 3.15 | 2.95 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV810SDBZR | SOT-23 | DBZ | 3 | 3000 | 179.0 | 8.4 | 3.15 | 2.95 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV810SDBZT | SOT-23 | DBZ | 3 | 250 | 179.0 | 8.4 | 3.15 | 2.95 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV810ZDBZR | SOT-23 | DBZ | 3 | 3000 | 179.0 | 8.4 | 3.15 | 2.95 | 1.22 | 4.0 | 8.0 | Q3 |
| TLV810ZDBZT | SOT-23 | DBZ | 3 | 250 | 179.0 | 8.4 | 3.15 | 2.95 | 1.22 | 4.0 | 8.0 | Q3 |

**TAPE AND REEL BOX DIMENSIONS**



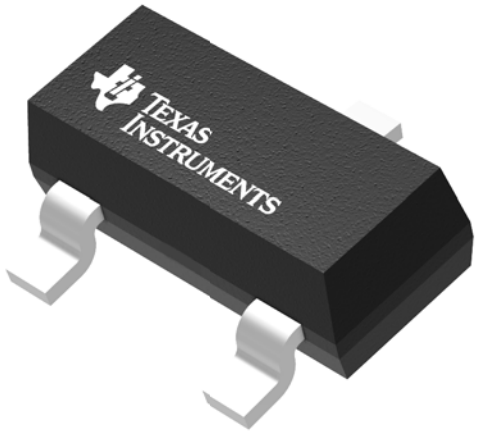

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV810MDBZR | SOT-23 | DBZ | 3 | 3000 | 203.0 | 203.0 | 35.0 |
| TLV810MDBZT | SOT-23 | DBZ | 3 | 250 | 203.0 | 203.0 | 35.0 |
| TLV810RDBZR | SOT-23 | DBZ | 3 | 3000 | 203.0 | 203.0 | 35.0 |
| TLV810RDBZT | SOT-23 | DBZ | 3 | 250 | 203.0 | 203.0 | 35.0 |
| TLV810SDBZR | SOT-23 | DBZ | 3 | 3000 | 203.0 | 203.0 | 35.0 |
| TLV810SDBZT | SOT-23 | DBZ | 3 | 250 | 203.0 | 203.0 | 35.0 |
| TLV810ZDBZR | SOT-23 | DBZ | 3 | 3000 | 203.0 | 203.0 | 35.0 |
| TLV810ZDBZT | SOT-23 | DBZ | 3 | 250 | 203.0 | 203.0 | 35.0 |

# GENERIC PACKAGE VIEW

## DBZ 3 SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



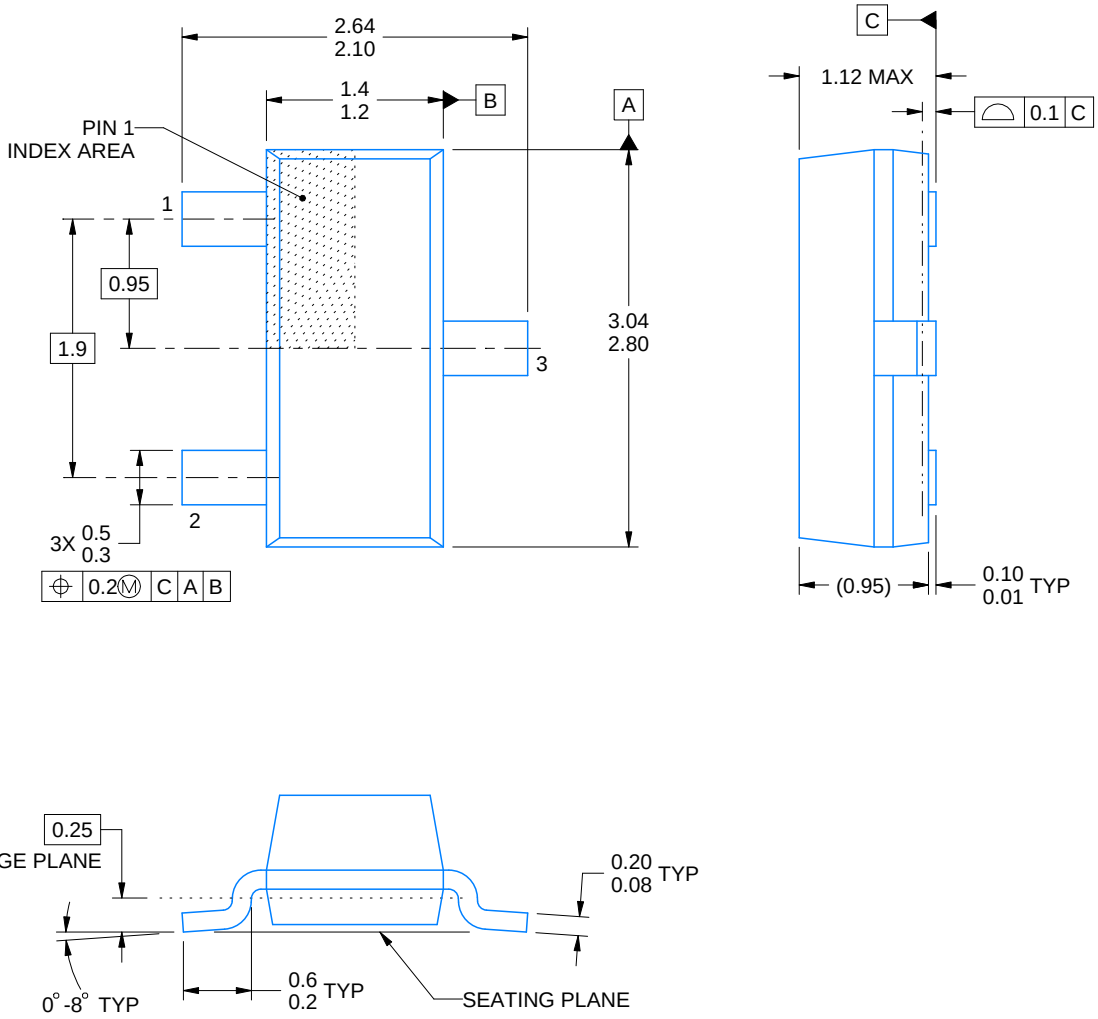

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

# PACKAGE OUTLINE

## DBZ0003A

## SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR

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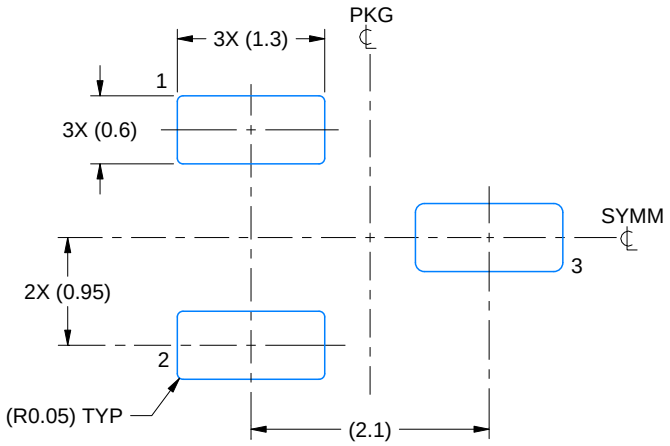
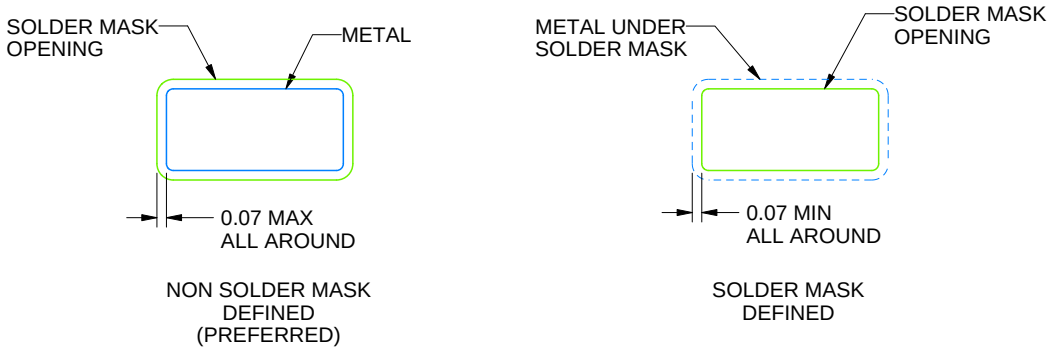
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.




LAND PATTERN EXAMPLE
SCALE:15X




SOLDER MASK DETAILS

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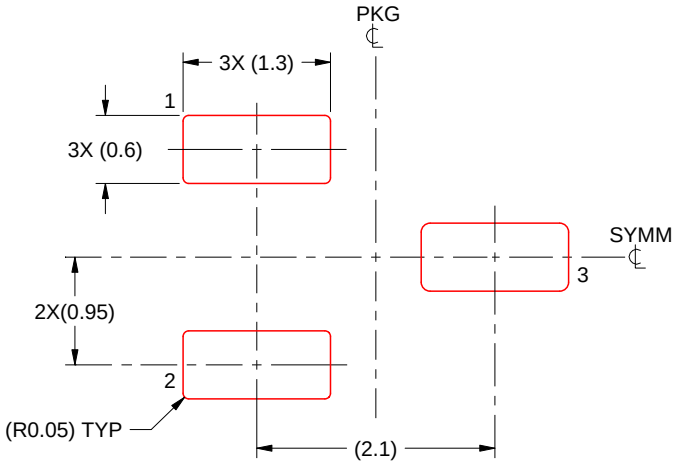
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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