BUF634 250-mA High-Speed Buffer

1 Features

- High Output Current: 250 mA
- Slew Rate: 2000 V/µs
- Pin-Selected Bandwidth: 30 MHz to 180 MHz
- Low Quiescent Current: 1.5 mA (30 MHz BW)
- Wide Supply Range: ±2.25 to ±18 V
- Internal Current Limit
- Thermal Shutdown Protection
- 8-Pin PDIP, SOIC-8, 5-Lead TO-220, 5-Lead DDPAK-TO-263 Surface-Mount

2 Applications

- Valve Driver
- Solenoid Driver
- Op Amp Current Booster
- Line Driver
- Headphone Driver
- Video Driver
- Motor Driver
- Test Equipment
- ATE Pin Driver

3 Description

The BUF634 device is a high speed, unity-gain open-loop buffer recommended for a wide range of applications. The BUF634 device can be used inside the feedback loop of op amps to increase output current, eliminate thermal feedback, and improve capacitive load drive.

For low power applications, the BUF634 device operates on 1.5-mA quiescent current with 250-mA output, 2000-V/µs slew rate, and 30-MHz bandwidth. Bandwidth can be adjusted from 30 MHz to 180 MHz by connecting a resistor between V– and the BW Pin.

Output circuitry is fully protected by internal current limit and thermal shut-down, making it rugged and easy to use.

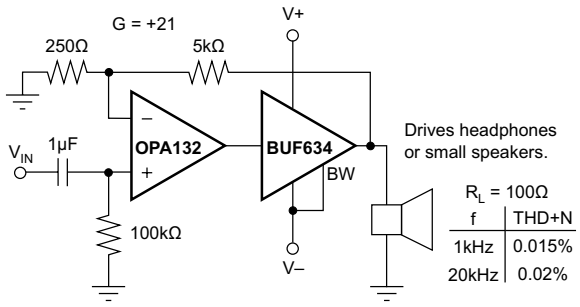
The BUF634 device is available in a variety of packages to suit mechanical and power dissipation requirements. Types include 8-pin PDIP, SOIC-8 surface-mount, 5-lead TO-220, and a 5-lead DDPAK-TO-263 surface-mount plastic power package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
BUF634	SOIC (8)	3.91 mm × 4.90 mm
	PDIP (8)	6.35 mm × 9.81 mm
	TO-220 (5)	8.51 mm × 10.16 mm
	DDPAK/TO-263 (5)	8.42 mm × 10.16 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Boost the Output Current of any Operational Amplifier



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2000) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

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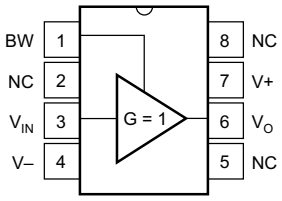
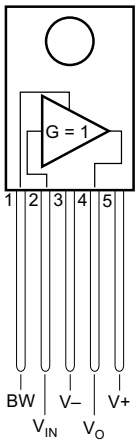
5 Pin Configuration and Functions

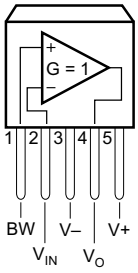
P and D Package
8-Pin PDIP and SOIC
Top View



KC Package
5-Pin TO-220
Top View



KTT Package
5-Pin DDPAK/TO-263
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	8 PINS	5 PINS		
BW	1	1	I	Bandwidth adjust pin
NC	2, 5, 8	–	–	No internal connection
V+	7	5	I	Positive power supply
V_{IN}	3	2	I	Input
V_O	6	4	O	Output
V–	4	3	I	Negative power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage		±18	V
Input voltage		$\pm V_S$	
Output short-circuit (to ground)		Continuous	
Operating temperature	–40	125	°C
Junction temperature		150	°C
Lead temperature (soldering, 10 s)		300	°C
Storage temperature, T_{stg}	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
BUF634F in PDIP and SOIC Packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
BUF634F in SOIC-8 Package Only				
$V_{(ESD)}$	Electrostatic discharge,	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	V
BUF634F in TO-220 and DDPAK Packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Vs = (V+) - (V-)	Supply voltage	±2.25 (4.5)	±15 (30)	±18 (36)	V
T_A	Operating temperature	-40	+25	+85	°C

6.4 Thermal Information

THERMAL METRIC (1)		BUF634				UNIT
		PDIP	SOIC	TO-220	DDPAK-TO-263	
		8 PINS	8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.5	103.4	32.1	41.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.8	44.2	25.6	45	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.8	44.5	18.3	24.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12	5.4	8.5	13.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.6	43.8	17.7	23.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	0.7	2.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953

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6.5 Electrical Characteristics

At T_A = +25°C[1], V_S = ±15 V, specifications are for both low quiescent-current mode and wide-bandwidth mode unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
Offset Voltage					±30	±100	mV
Offset Voltage vs Temperature		Specified Temperature Range			±100		µV/°C
Offset Voltage vs Power Supply		V_S = ±2.25 V[2] to ±18 V			0.1	1	mV/V
Input Bias Current		V_{IN} = 0V	Low Quiescent Current Mode		±0.5	±2	µA
			Wide Bandwidth Mode		±5	±20	
Input Impedance		R_L = 100 Ω	Low Quiescent Current Mode		80 || 8		MΩ || pF
			Wide Bandwidth Mode		8 || 8		
Noise Voltage		f = 10 kHz			4		nV/√Hz
GAIN							
Gain		R_L = 1 kΩ, V_O = ±10 V		0.95	0.99		V/V
		R_L = 100 Ω, V_O = ±10 V		0.85	0.93		
		R_L = 67 Ω, V_O = ±10 V		0.8	0.9		
OUTPUT							
Current Output, Continuous					±250		mA
Voltage Output	Positive	I_O = 10 mA		(V+) –2.1	(V+) –1.7		V
	Negative	I_O = –10 mA		(V–) +2.1	(V–) +1.8		
	Positive	I_O = 100 mA		(V+) –3	(V+) –2.4		
	Negative	I_O = –100 mA		(V–) +4	(V–) +3.5		
	Positive	I_O = 150 mA		(V+) –4	(V+) –2.8		
	Negative	I_O = –150 mA		(V–) +5	(V–) +4		
Short-Circuit Current		Low Quiescent Current Mode			±350	±550	mA
		Wide Bandwidth Mode			±400	±550	
DYNAMIC RESPONSE							
Bandwidth, –3dB		R_L = 1 kΩ	Low Quiescent Current Mode		30		MHz
			Wide Bandwidth Mode		180		
		R_L = 100 Ω	Low Quiescent Current Mode		20		
			Low Quiescent Current Mode		160		
Slew Rate		20 Vp-p, R_L = 100 Ω			2000		V/µs
Settling Time	0.1%	20-V Step, R_L = 100 Ω			200		ns
	1%				50		
Differential Gain		3.58 MHz, V_O = 0.7 V, R_L = 150 Ω	Low Quiescent Current Mode		4%		
			Wide Bandwidth Mode		0.4%		
Differential Phase		3.58 MHz, V_O = 0.7 V, R_L = 150 Ω	Low Quiescent Current Mode		2.5		°
			Wide Bandwidth Mode		0.1		
POWER SUPPLY							
Specified Operating Voltage					±15		V
Operating Voltage Range				±2.25[2]		±18	V

(1) Tests are performed on high speed automatic test equipment, at approximately 25°C junction temperature. The power dissipation of this product will cause some parameters to shift when warmed up. See *Typical Characteristics* for over-temperature performance.
(2) Limited output swing available at low supply voltage. See Output voltage specifications.

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Electrical Characteristics (continued)

At T_A = +25°C[(1)], V_S = ±15 V, specifications are for both low quiescent-current mode and wide-bandwidth mode unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_Q	Quiescent Current	I_O = 0	Low Quiescent Current Mode		±1.5	±2	mA
			Wide Bandwidth Mode		±15	±20	
TEMPERATURE RANGE							
	Specification			–40		85	°C
	Operating			–40		125	°C
T_J	Thermal Shutdown Temperature				175		°C

6.6 Typical Characteristics

At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

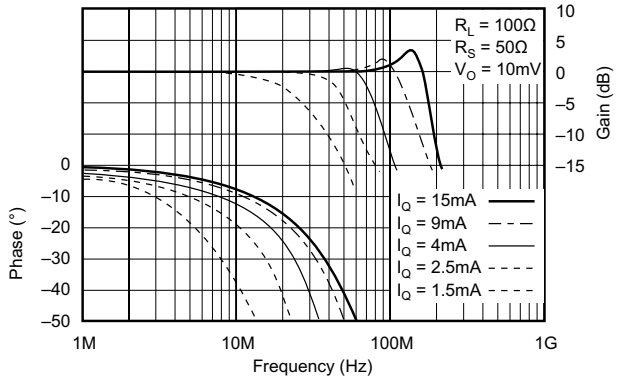

Figure 1. Gain and Phase vs Frequency vs Quiescent Current

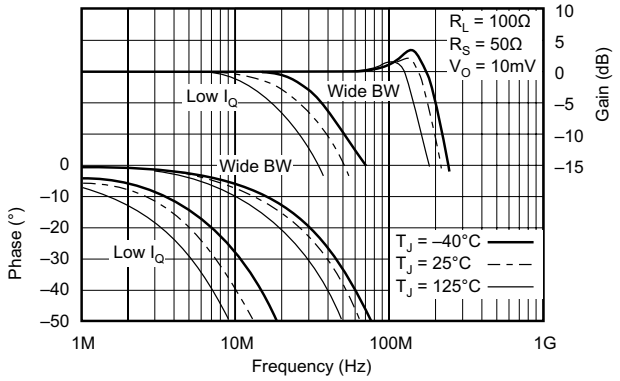

Figure 2. Gain and Phase vs Frequency vs Temperature

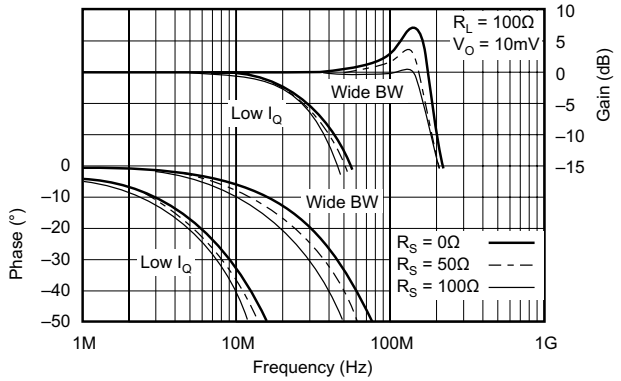

Figure 3. Gain and Phase vs Frequency vs Source Resistance

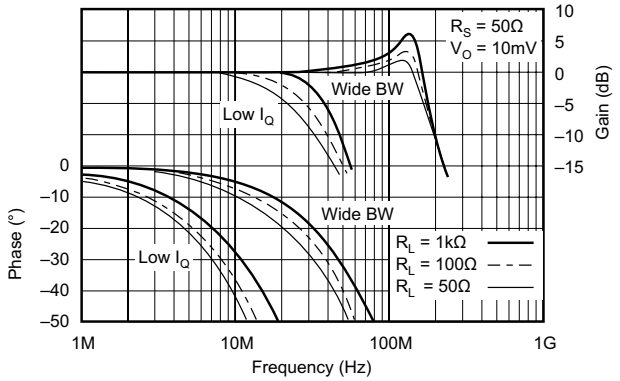

Figure 4. Gain and Phase vs Frequency vs Load Resistance

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Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

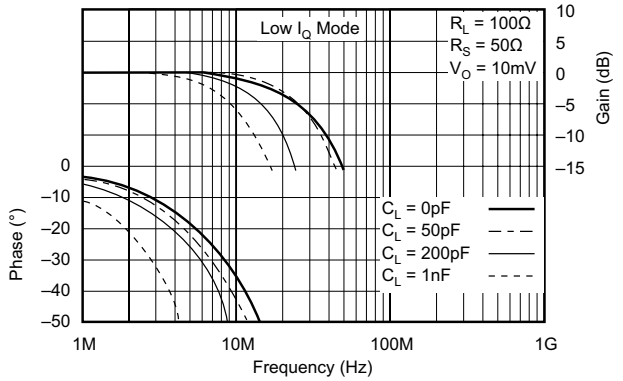

Figure 5. Gain and Phase vs Frequency vs Load Capacitance

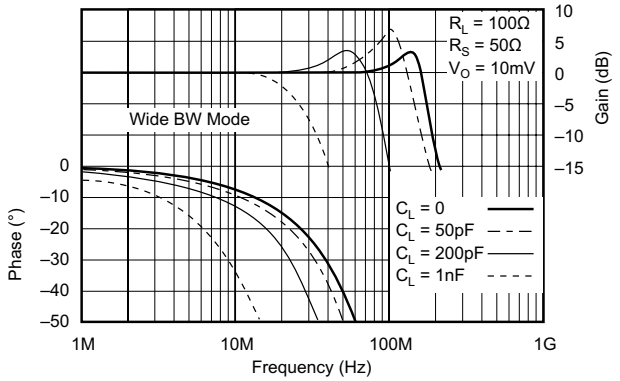

Figure 6. Gain and Phase vs Frequency vs Load Capacitance

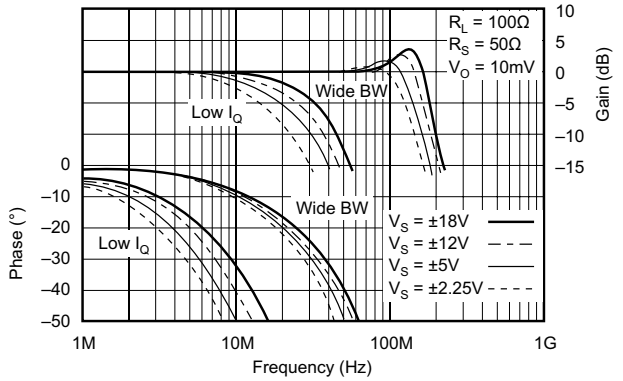

Figure 7. Gain and Phase vs Frequency vs Power Supply Voltage

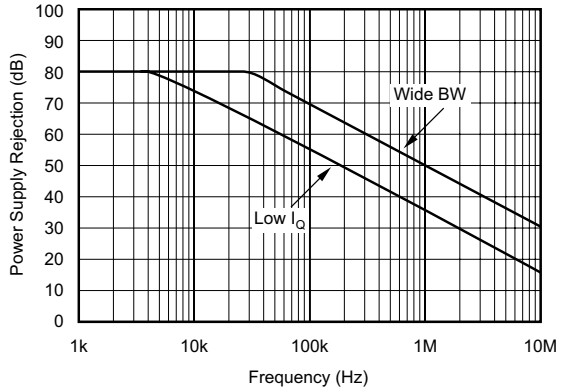

Figure 8. Power Supply Rejection vs Frequency

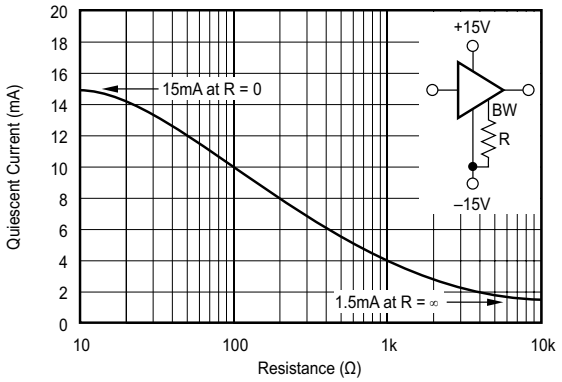

Figure 9. Quiescent Current vs Bandwidth Control Resistance

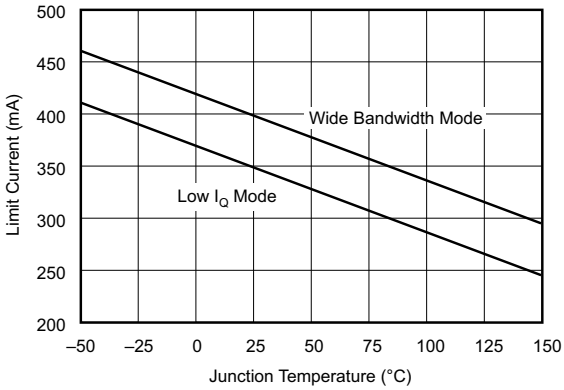

Figure 10. Short-Circuit Current vs Temperature

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Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

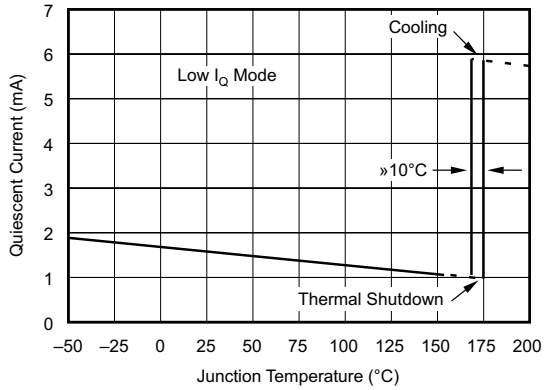

Figure 11. Quiescent Current vs Temperature

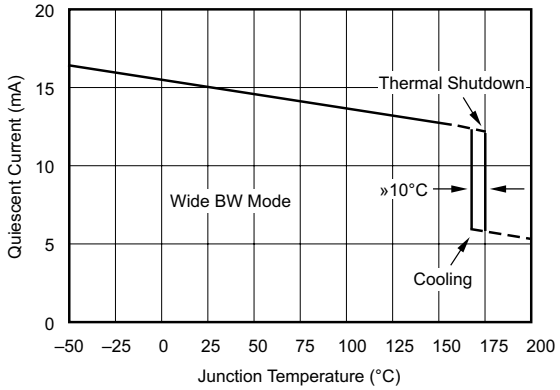

Figure 12. Quiescent Current vs Temperature

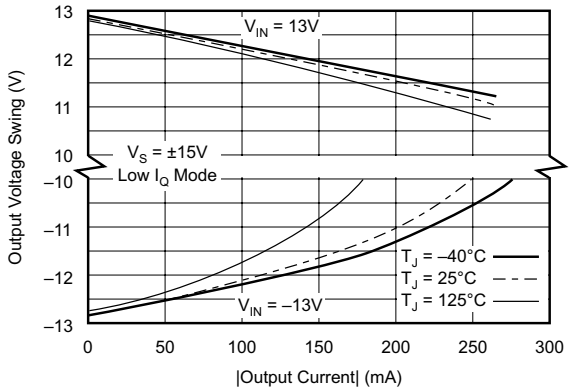

Figure 13. Output Voltage Swing vs Output Current

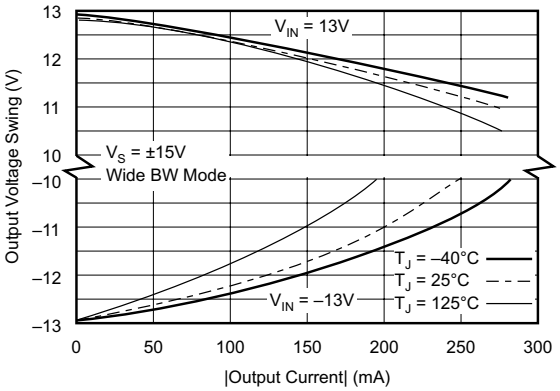

Figure 14. Output Voltage Swing vs Output Current

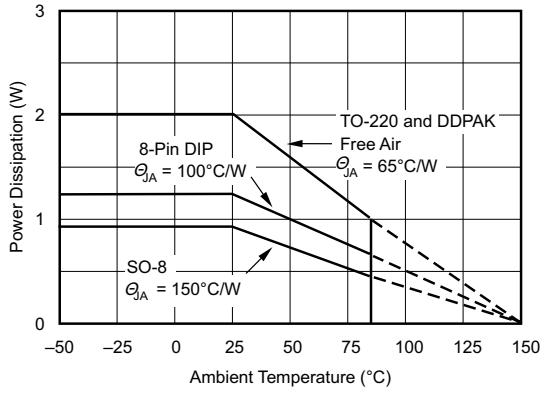

Figure 15. Maximum Power Dissipation vs Temperature

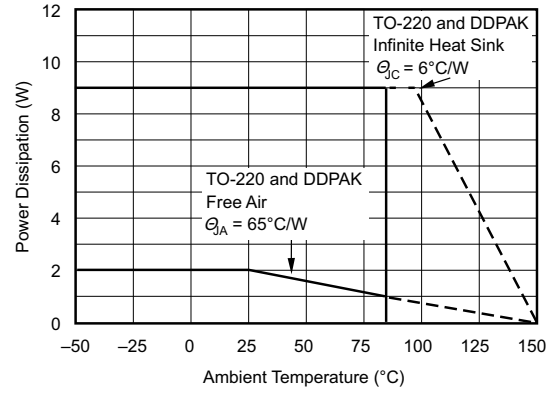

Figure 16. Maximum Power Dissipation vs Temperature

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Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

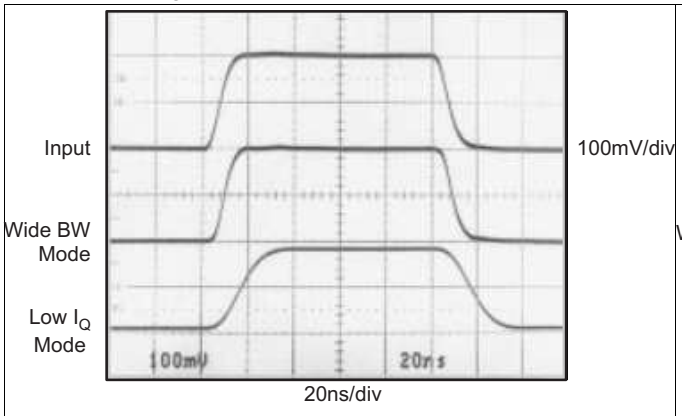

Figure 17. Small-Signal Response
R_S = 50 Ω, R_L = 100 Ω

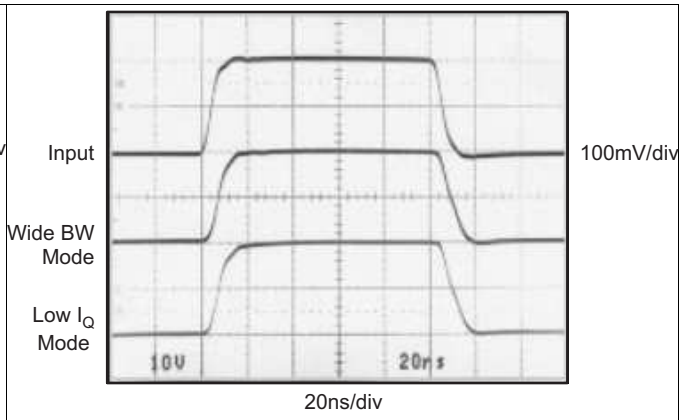

Figure 18. Large-Signal Response
R_S = 50 Ω, R_L = 100 Ω

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7 Detailed Description

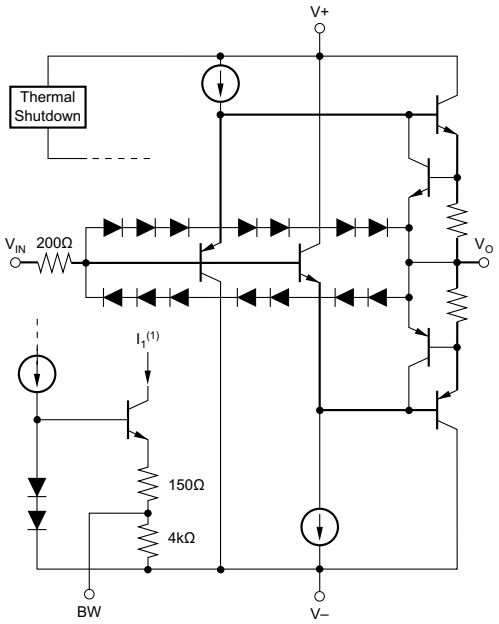
7.1 Overview

The BUF634 device is a high speed, unity-gain open-loop buffer recommended for a wide range of applications. The BUF634 device can be used inside the feedback loop of op amps to increase output current, eliminate thermal feedback, and improve capacitive load drive.

For low power applications, the BUF634 device operates on 1.5-mA quiescent current with 250-mA output, 2000-V/µs slew rate, and 30-MHz bandwidth. Bandwidth can be adjusted from 30 MHz to 180 MHz by connecting a resistor between V– and the BW Pin refer to Figure 9 and Figure 1. Output circuitry is fully protected by internal current limit and thermal shut-down, making it rugged and easy to use.

See the *Functional Block Diagram* section for a simplified circuit diagram of the BUF634 showing its open-loop complementary follower design.

7.2 Functional Block Diagram



Signal path indicated in bold.
Note: (1) Stage currents are set by I_1.

7.3 Feature Description

7.3.1 Output Current

The BUF634 device can deliver up to ±250-mA continuous output current. Internal circuitry limits output current to approximately ±350 mA; see Figure 10. For many applications, however, the continuous output current will be limited by thermal effects.

The output voltage swing capability varies with junction temperature and output current (see Figure 14). Although all four package types are tested for the same output performance using a high speed test, the higher junction temperatures with the DIP and SO-8 package types often provide less output voltage swing. Junction temperature is reduced in the DDPAK surface-mount power package because it is soldered directly to the circuit board. The TO-220 package used with a good heat sink further reduces junction temperature, allowing maximum possible output swing.

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7.4 Device Functional Modes

The BUF634 is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the BUF634 is 36 V (±18 V). At low power supply conditions, such as ±2.25 V, the output swing may be limited. Refer to *Electrical Characteristics* for additional information.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Figure 19 shows the BUF634 device connected as an open-loop buffer. The source impedance and optional input resistor, R_S, influence frequency response: see *Typical Characteristics*. Power supplies should be bypassed with capacitors connected close to the device pins. Capacitor values as low as 0.1 µF assure stable operation in most applications, but high output current and fast output slewing can demand large current transients from the power supplies. Solid tantalum 10-µF capacitors are recommended. High frequency open-loop applications may benefit from special bypassing and layout considerations. See *High Frequency Applications* for more information.

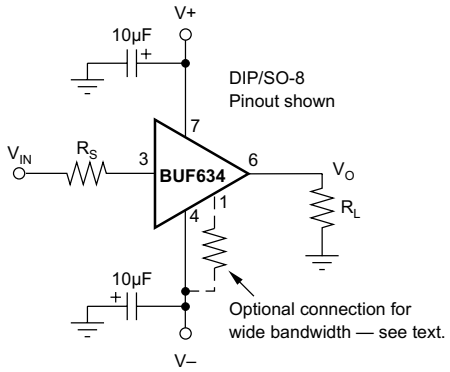

Figure 19. Buffer Connections

8.1.1 High Frequency Applications

The excellent bandwidth and fast slew rate of the BUF634 device are useful in a variety of high frequency open-loop applications. When operated open-loop, printed-circuit-board layout and bypassing technique can affect dynamic performance.

For best results, use a ground plane-type circuit board layout and bypass the power supplies with 0.1-µF ceramic chip capacitors at the device pins in parallel with solid tantalum 10-µF capacitors. Source resistance affects high-frequency peaking, step-response overshoot and ringing. Best response is usually achieved with a series input resistor of 25 Ω to 200 Ω, depending on the signal source. Response with some loads (especially capacitive) can be improved with a resistor of 10 Ω to 150 Ω in series with the output.

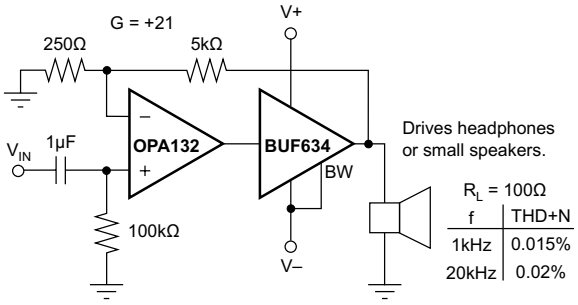

Figure 20. High Performance Headphone Driver

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Application Information (continued)

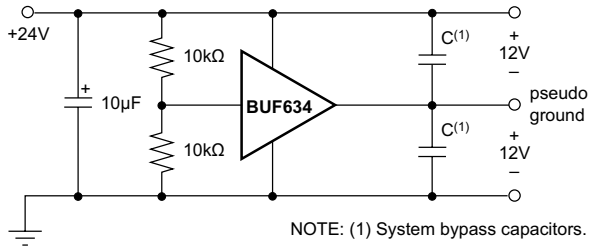


Figure 21. Pseudo-Ground Driver

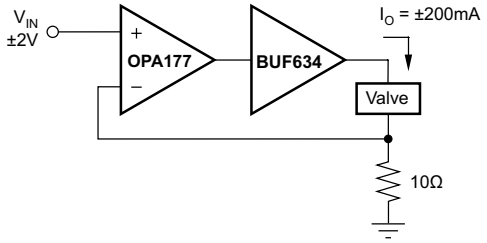


Figure 22. Current-Output Valve Driver

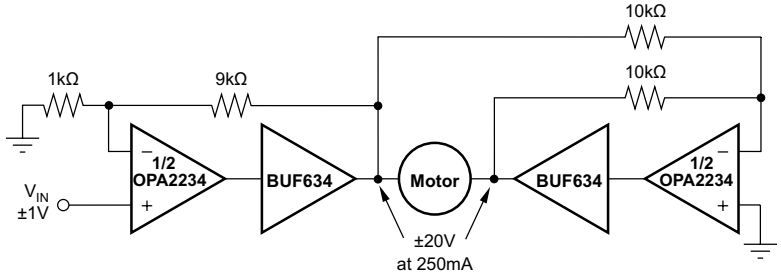
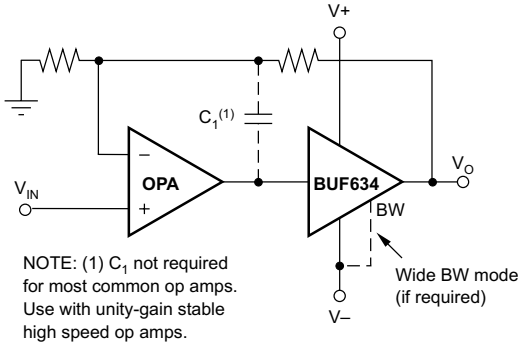


Figure 23. Bridge-Connected Motor Driver

8.2 Typical Application

8.2.1 Boosting Op Amp Output Current

The BUF634 device can be connected inside the feedback loop of most op amps to increase output current (see Figure 24). When connected inside the feedback loop, the offset voltage of the BUF634 device and other errors are corrected by the feedback of the op amp.



OP AMP	RECOMMENDATIONS
OPA177, OPA1013 OPA111, OPA2111 OPA121, OPA234(1), OPA130(1)	Use Low I_Q mode. G = 1 stable.
OPA27, OPA2107 OPA602, OPA131(1)	Low I_Q mode is stable. Increasing C_L may cause excessive ringing or instability. Use Wide BW mode.
OPA627, OPA132(1)	Use Wide BW mode, C_1 = 200pF. G = 1 stable.
OPA637, OPA37	Use Wide BW mode. These op amps are not G = 1 stable. Use in G > 4.

NOTE: (1) Single, dual, and quad versions.

Figure 24. Boosting Op Amp Output Current

Typical Application (continued)

8.2.1.1 Design Requirements

- Boost the output current of an OPA627
- Operate from ±15V power supplies
- Operate from -40°C to +85°C
- Gain = 23.5 V/V
- Output current = ±250 mA
- Bandwidth greater than 100 kHz

8.2.1.2 Detailed Design Procedure

To assure that the composite amplifier remains stable, the phase shift of the BUF634 device must remain small throughout the loop gain of the circuit. For a G=+1 op amp circuit, the BUF634 device must contribute little additional phase shift (approximately 20° or less) at the unity-gain frequency of the op amp. Phase shift is affected by various operating conditions that may affect stability of the op amp; see *Typical Characteristics*.

Most general-purpose or precision op amps remain unity-gain stable with the BUF634 device connected inside the feedback loop as shown. Large capacitive loads may require the BUF634 device to be connected for wide bandwidth for stable operation. High speed or fast-settling op amps generally require the wide bandwidth mode to remain stable and to assure good dynamic performance. To check for stability with an op amp, look for oscillations or excessive ringing on signal pulses with the intended load, and worst-case conditions that affect phase response of the buffer. Connect the circuit as shown in Figure 24. Choose resistors to provide a voltage gain of 23.5 V/V. Select the feedback resistor to be 2.7 kΩ. Choose the input resistor to be 120 Ω.

8.2.1.3 Application Curve

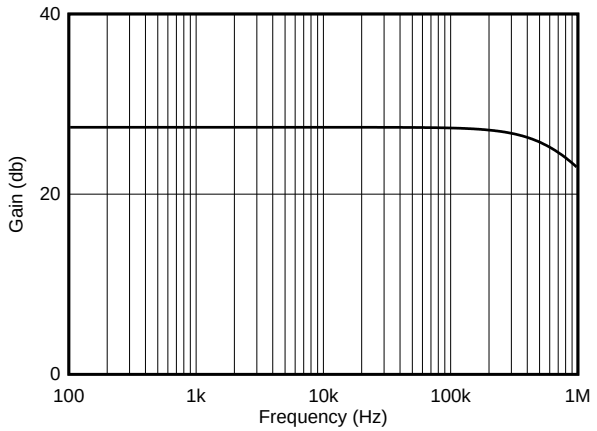


Figure 25. Frequency Response of Composite Amplifier

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9 Power Supply Recommendations

The BUF634 is specified for operation from 4.5V to 36 V (±2.25 V to ±18 V). Many specifications apply from –40°C to +85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques*, SLOA089.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 27
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

Power dissipated in the BUF634 device causes the junction temperature to rise. A thermal protection circuit in the BUF634 device disables the output when the junction temperature reaches approximately 175°C. When the thermal protection is activated, the output stage is disabled, allowing the device to cool. Quiescent current is approximately 6 mA during thermal shutdown. When the junction temperature cools to approximately 165°C, the output circuitry is again enabled. This can cause the protection circuit to cycle on and off with a period ranging from a fraction of a second to several minutes or more, depending on package type, signal, load and thermal environment.

The thermal protection circuit is designed to prevent damage during abnormal conditions. Any tendency to activate the thermal protection circuit during normal operation is a sign of an inadequate heat sink or excessive power dissipation for the package type.

The TO-220 package provides the best thermal performance. When the TO-220 is used with a properly sized heat sink, output is not limited by thermal performance. See Application Bulletin AB-037 for details on heat sink calculations. The DDPAK also has excellent thermal characteristics. Its mounting tab should be soldered to a circuit board copper area for good heat dissipation. Figure 26 shows typical thermal resistance from junction to ambient as a function of the copper area. The mounting tab of the TO-220 and DDPAK packages is electrically-connected to the V– power supply.

The DIP and SO-8 surface-mount packages are excellent for applications requiring high output current with low average power dissipation. To achieve the best possible thermal performance with the DIP or SO-8 packages, solder the device directly to a circuit board. Because much of the heat is dissipated by conduction through the package pins, sockets will degrade thermal performance. Use wide circuit board traces on all the device pins, including pins that are not connected. With the DIP package, use traces on both sides of the printed circuit board if possible.

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Layout Guidelines (continued)

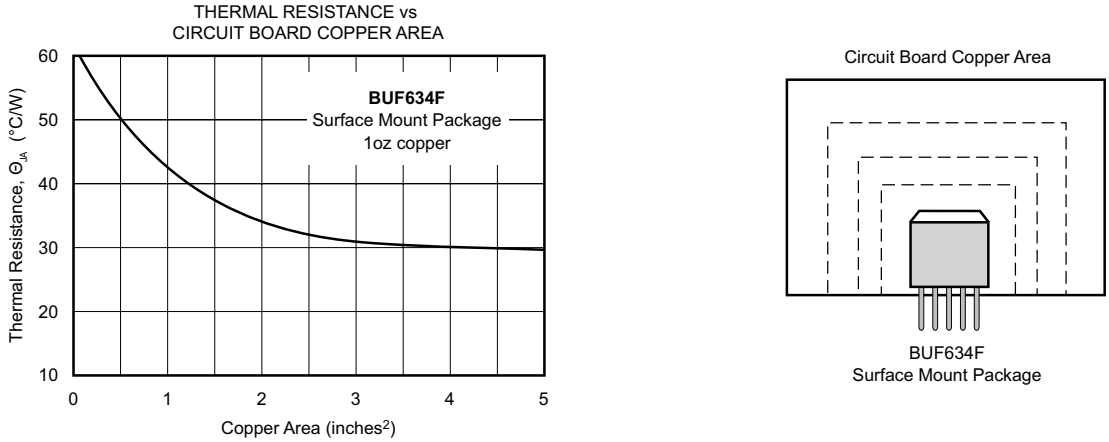

Figure 26. Thermal Resistance vs Circuit Board Copper Area

10.2 Layout Example

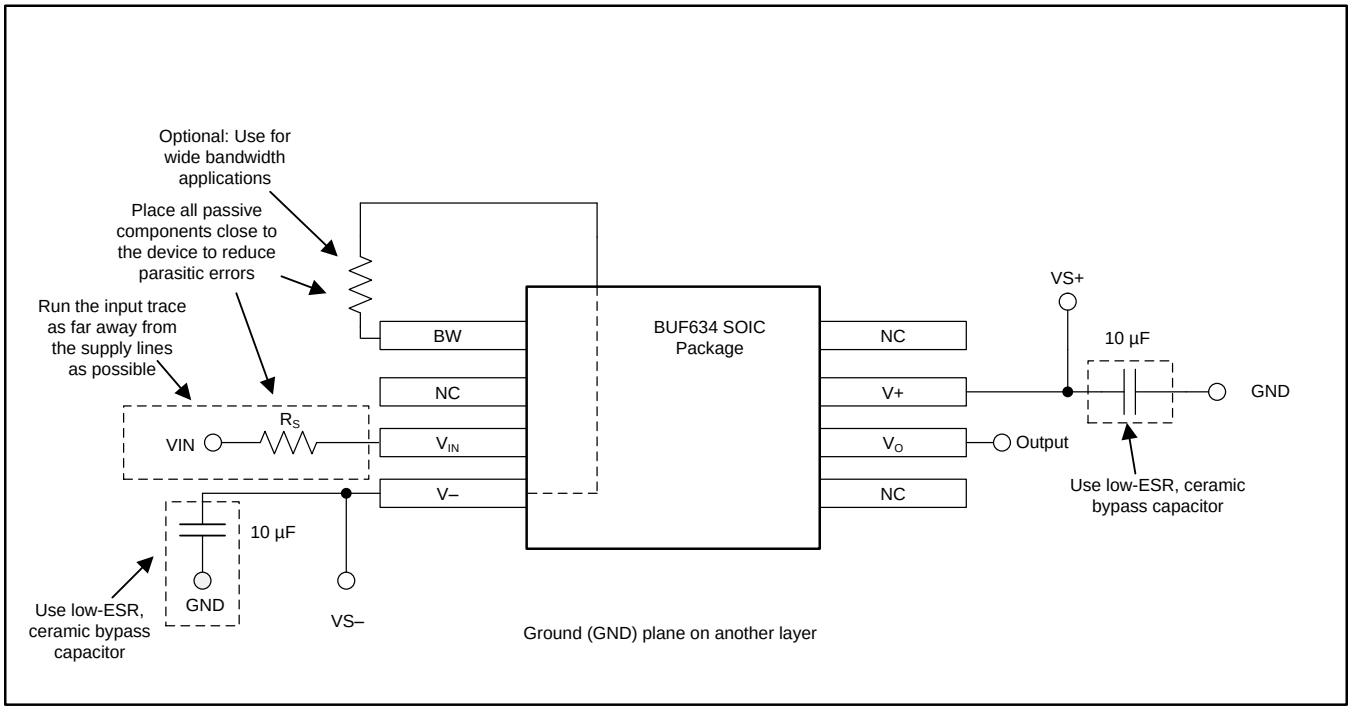

Figure 27. BUF634 Layout Example

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10.1 Power Dissipation

Power dissipation depends on power supply voltage, signal, and load conditions. With DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor, $V_S - V_O$. Power dissipation can be minimized by using the lowest possible power supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power supply voltage. Dissipation with AC signals is lower. Application Bulletin SBOS022 explains how to calculate or measure power dissipation with unusual signals and loads.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 150°C, maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered. The thermal protection should trigger more than 45°C above the maximum expected ambient condition of your application.

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11 Device and Documentation Support

11.1 Device Support

11.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.2 TI Precision Designs

The BUF634 is featured in several TI Precision Designs, available online at http://www.ti.com/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, please see the following:

Circuit Board Layout Techniques, SLOA089.

Combining an Amplifier with the BUF634, SBOA065

Add Current Limit to the BUF634, SBOA042

Power Amplifier Stress and Power Handling Limitations , SBOA022

Shelf-Life Evaluation of Lead-Free Component Finishes, SZZA046

11.3 Community Resource

The following links connect TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support **TI's Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BUF634F/500	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS)	CU SN	Level-2-260C-1 YEAR	-40 to 125	BUF634F	Samples
BUF634F/500E3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS)	CU SN	Level-2-260C-1 YEAR	-40 to 125	BUF634F	Samples
BUF634FKTTT	ACTIVE	DDPAK/ TO-263	KTT	5	250	Pb-Free (RoHS)	CU SN	Level-2-260C-1 YEAR	-40 to 125	BUF634F	Samples
BUF634FKTTTE3	ACTIVE	DDPAK/ TO-263	KTT	5	250	Pb-Free (RoHS)	CU SN	Level-2-260C-1 YEAR	-40 to 125	BUF634F	Samples
BUF634P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 125	BUF634P	Samples
BUF634PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 125	BUF634P	Samples
BUF634T	ACTIVE	TO-220	KC	5	49	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	BUF634T	Samples
BUF634TG3	ACTIVE	TO-220	KC	5	49	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	BUF634T	Samples
BUF634U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	BUF 634U	Samples
BUF634U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	BUF 634U	Samples
BUF634UE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	BUF 634U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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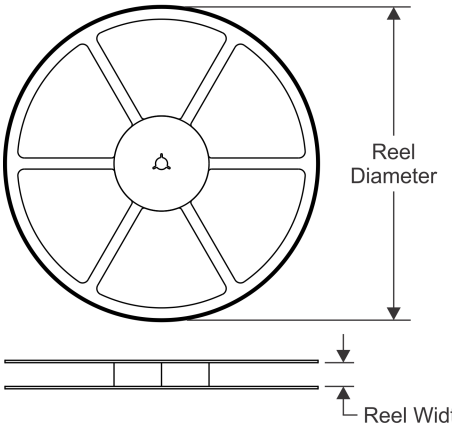
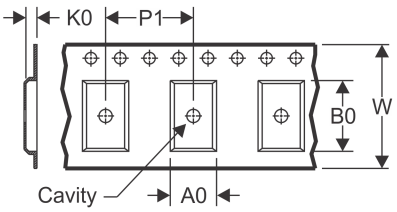
TAPE AND REEL INFORMATION

REEL DIMENSIONS

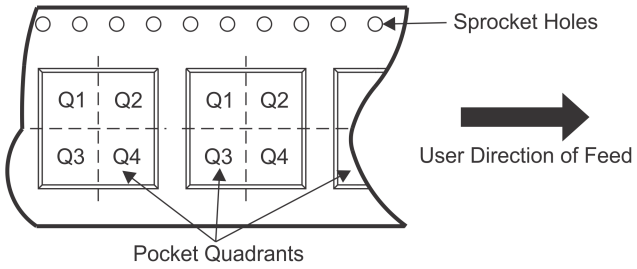


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

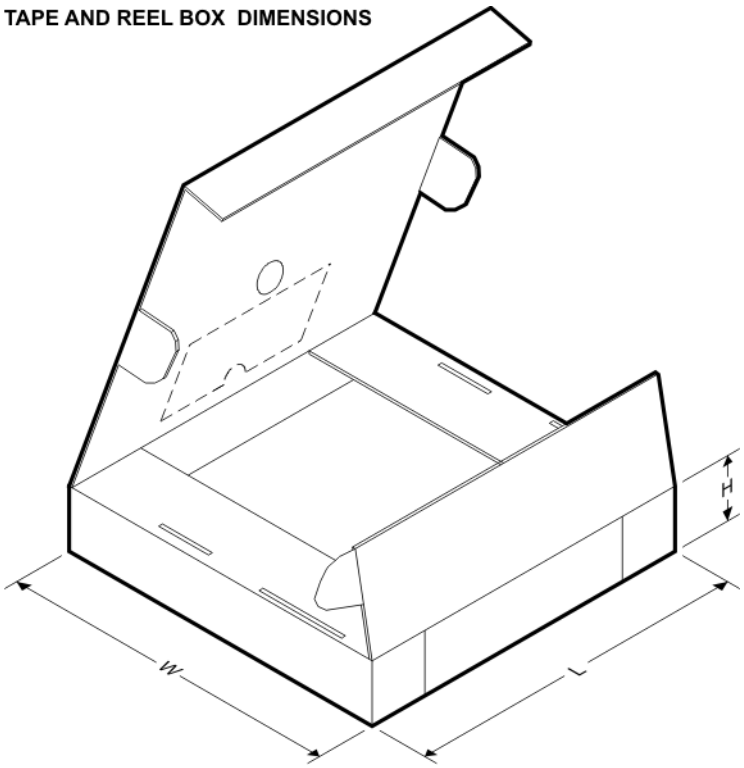
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF634F/500	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
BUF634FKTTT	DDPAK/ TO-263	KTT	5	250	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
BUF634U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

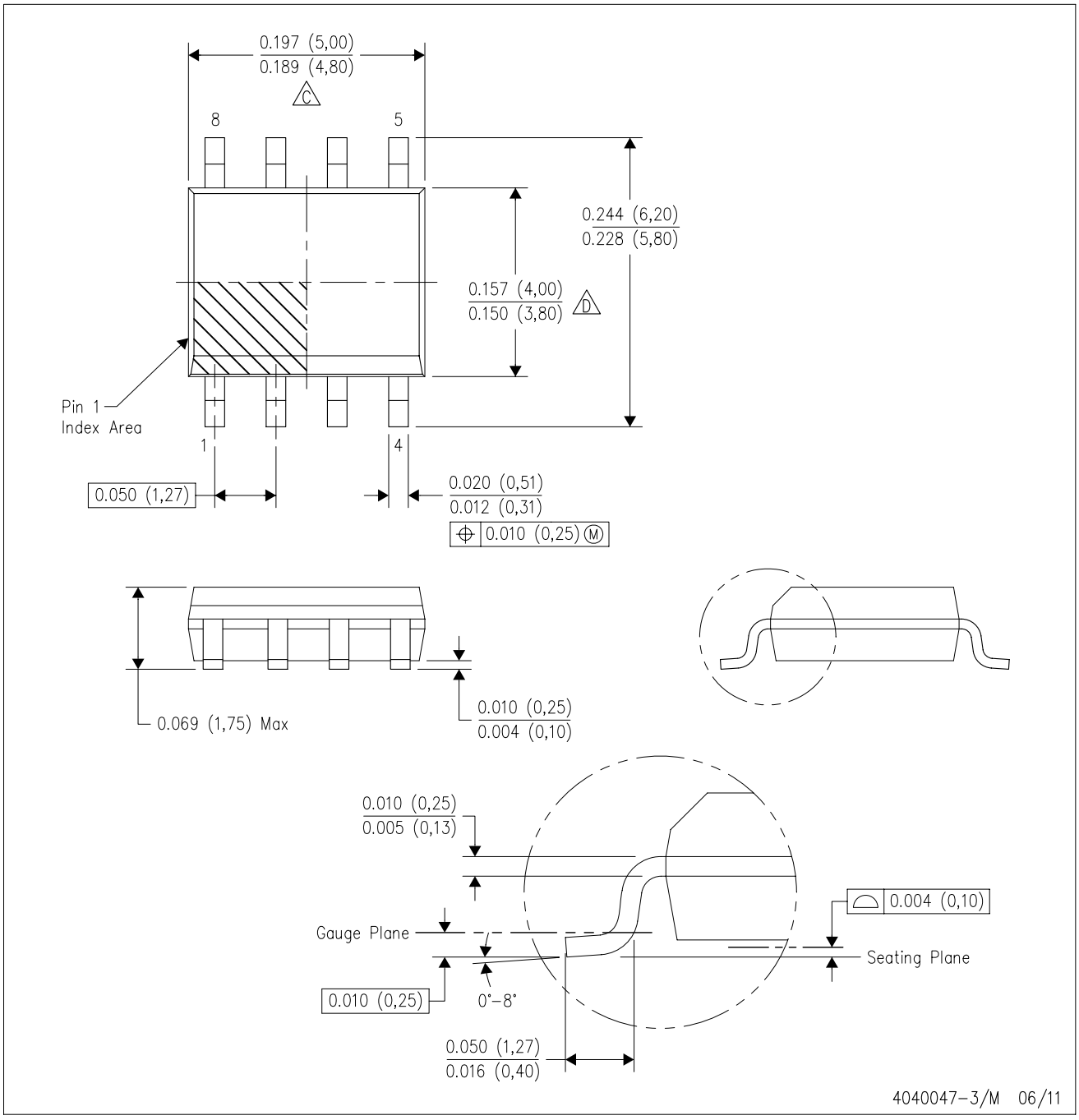
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

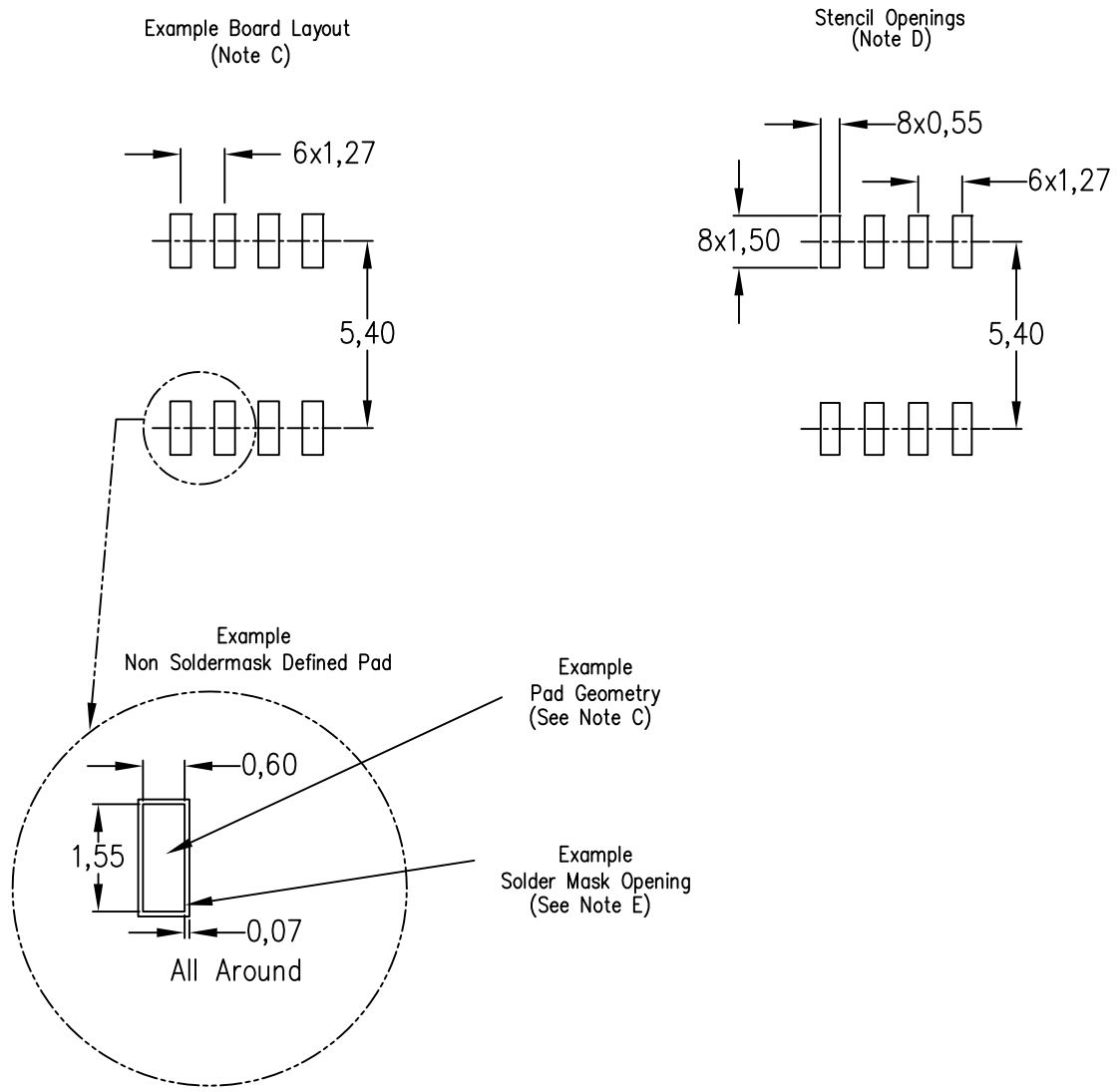
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF634F/500	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
BUF634FKTTT	DDPAK/TO-263	KTT	5	250	367.0	367.0	45.0
BUF634U/2K5	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



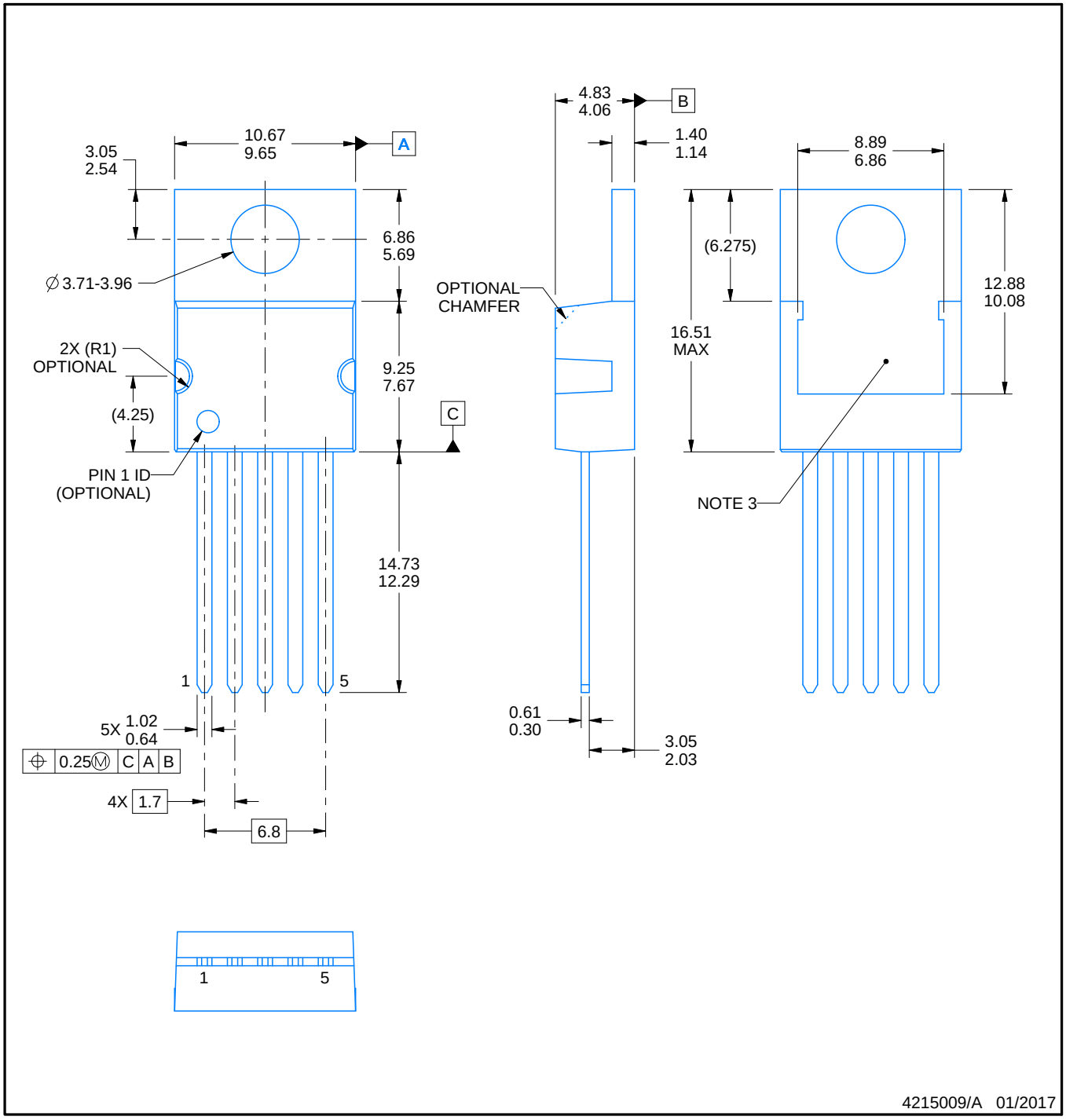
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

KC0005A

PACKAGE OUTLINE

TO-220 - 16.51 mm max height

TO-220



NOTES:

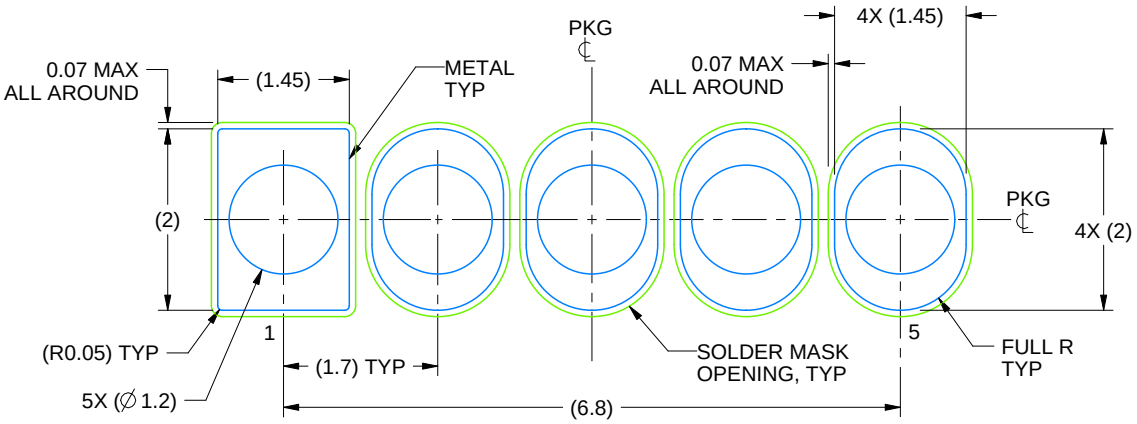
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.

EXAMPLE BOARD LAYOUT

KC0005A

TO-220 - 16.51 mm max height

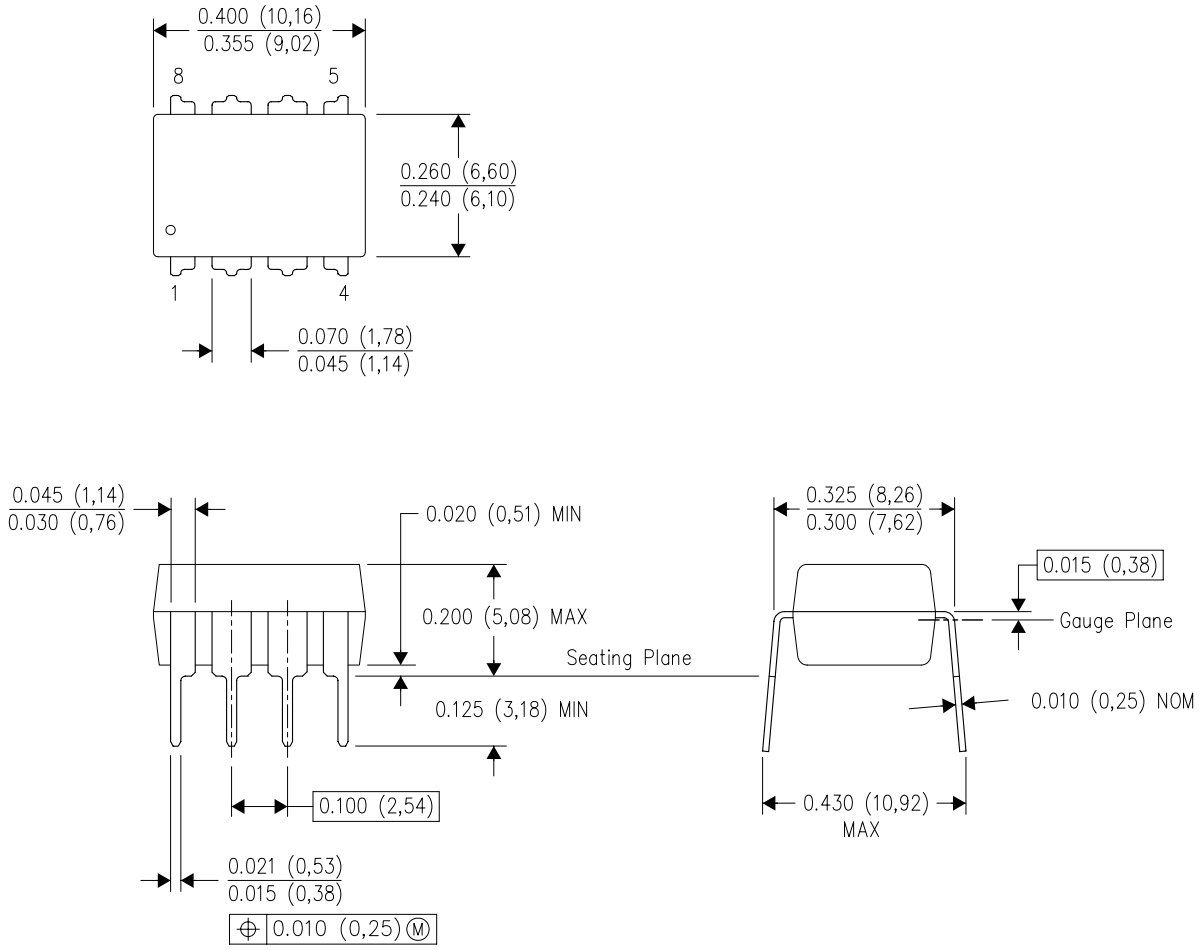
TO-220



LAND PATTERN
NON-SOLDER MASK DEFINED
SCALE:12X

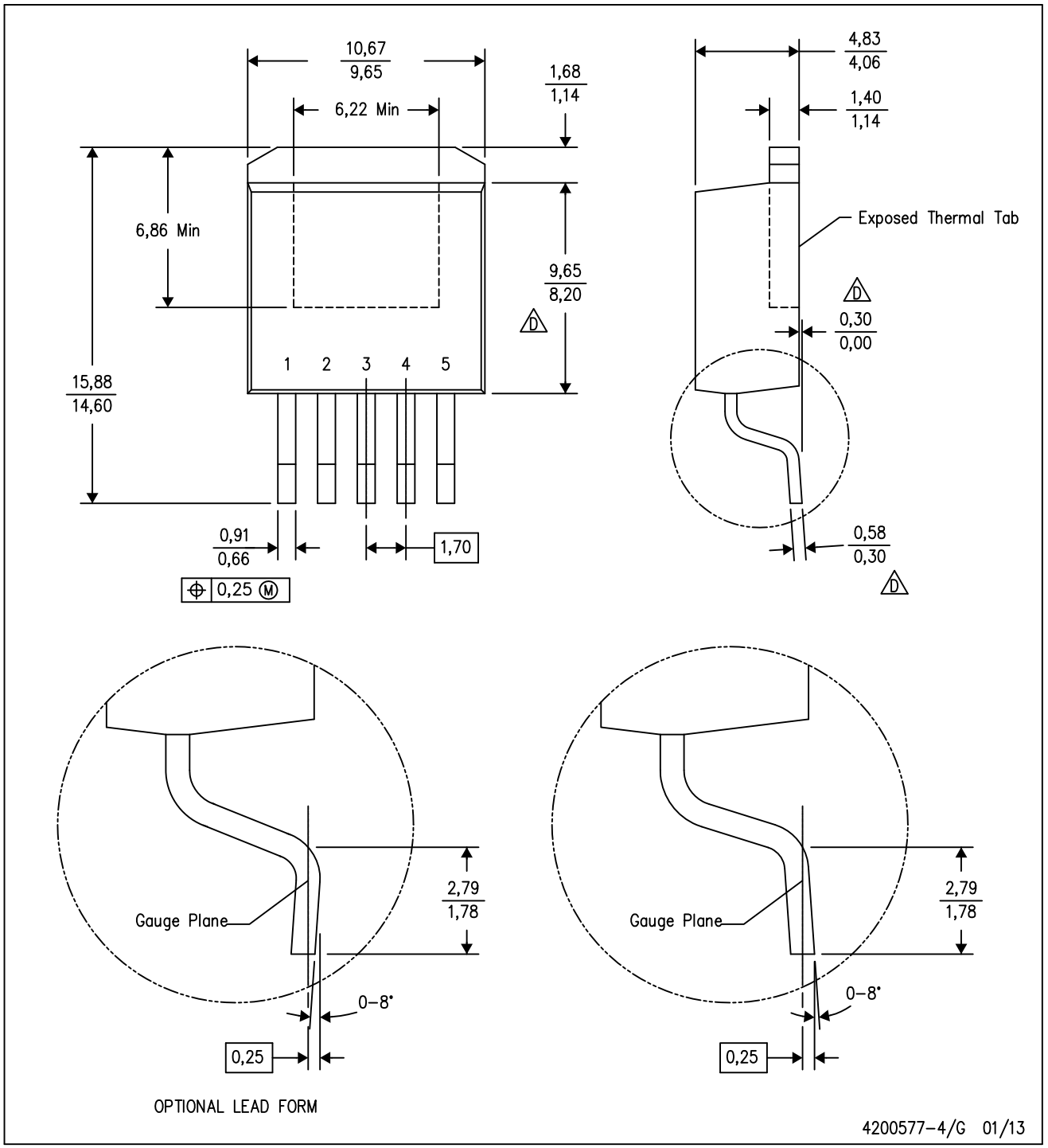
4215009/A 01/2017

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



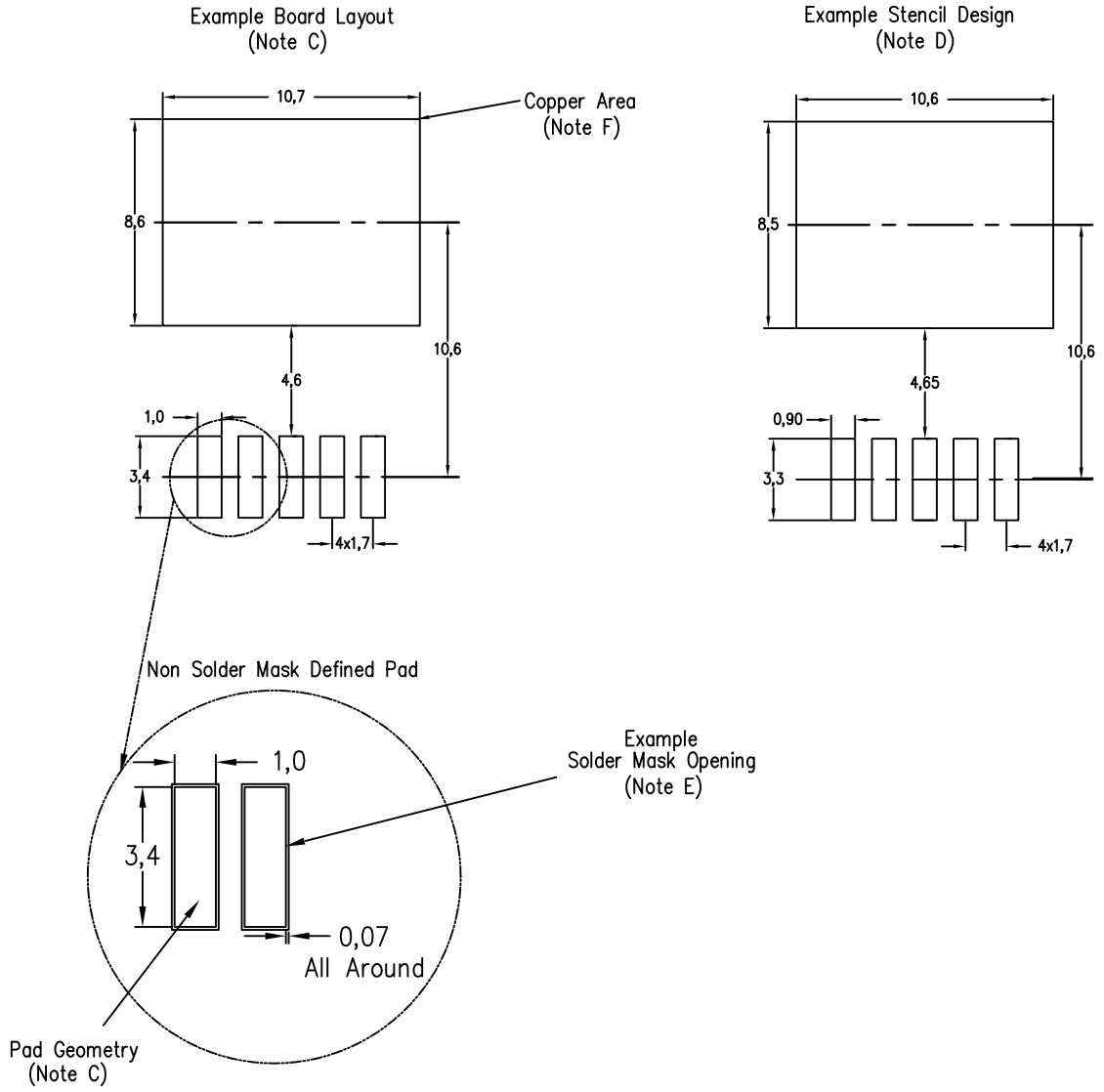
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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