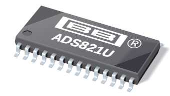


SBAS040B – DECEMBER 1995 – REVISED FEBRUARY 2005

10-Bit, 40MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **NO MISSING CODES**
- **INTERNAL REFERENCE**
- **LOW POWER: 380mW**
- **HIGH SNR: 58dB**
- **INTERNAL TRACK-AND-HOLD**

APPLICATIONS

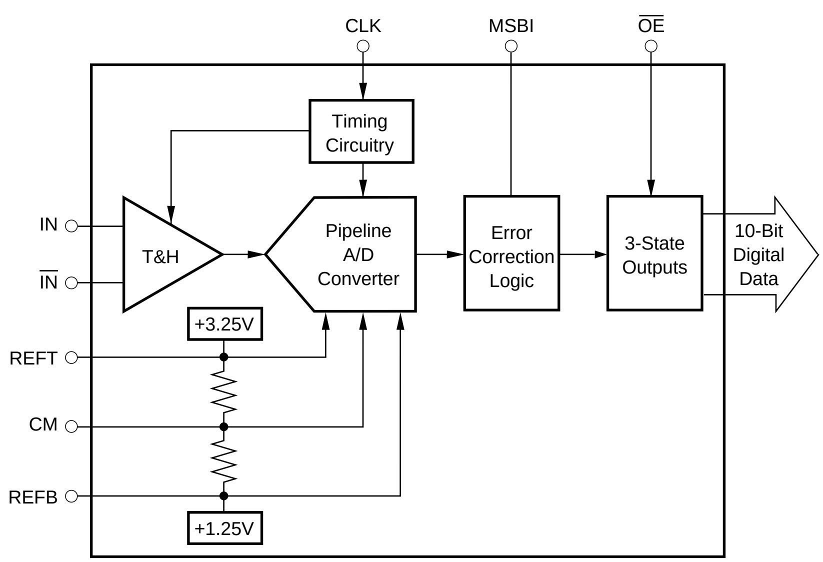
- **VIDEO DIGITIZING**
- **ULTRASOUND IMAGING**
- **GAMMA CAMERAS**
- **SET-TOP BOXES**
- **CABLE MODEMS**
- **CCD IMAGING**
  - **Color Copiers**
  - **Scanners**
  - **Camcorders**
  - **Security Cameras**
  - **Fax Machines**
- **IF AND BASEBAND DIGITIZATION**
- **TEST INSTRUMENTATION**

DESCRIPTION

The ADS821 is a low-power, monolithic 10-bit, 40MHz Analog-to-Digital (A/D) converter utilizing a small geometry CMOS process. This complete converter includes a 10-bit quantizer with internal track-and-hold, reference, and a power-down feature. It operates from a single +5V power supply and can be configured to accept either differential or single-ended input signals.

The ADS821 employs digital error correction to provide excellent Nyquist differential linearity performance for demanding imaging applications. Its low distortion, high SNR, and high oversampling capability give it the extra margin needed for telecommunications and video applications.

This high-performance converter is specified for AC and DC-performance at a 40MHz sampling rate. The ADS821 is available in an SO-28 package.



ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$	+6V
Analog Input	0V to ($+V_S$ + 300mV)
Logic Input	0V to ($+V_S$ + 300mV)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+125°C
External Top Reference Voltage (REFT)	+3.4V max
External Bottom Reference Voltage (REFB)	+1.1V min

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS821	SO-8	DW	–40°C to +85°C	ADS821U	ADS821U	Rails, 28
"	"	"	"	"	ADS821U/1K	Tape and Reel, 1000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, and with a 50% duty cycle clock having a 2ns rise-and-fall time, unless otherwise noted.

PARAMETER	CONDITIONS	TEMP	ADS821U MIN	ADS821U TYP	ADS821U MAX	UNITS
RESOLUTION					10	Bits
Specified Temperature Range	$T_{AMBIENT}$		–40		+85	°C
ANALOG INPUT						
Differential Full-Scale Input Range			+1.25		+3.25	V
Common-Mode Voltage					+2.25	V
Analog Input Bandwidth (–3dB)						
Small-Signal	–20dBFS[1] Input	+25°C		400		MHz
Full-Power	0dBFS Input	+25°C		65		MHz
Input Impedance				1.25 || 4		MΩ || pF
DIGITAL INPUT						
Logic Family				TTL/HCT Compatible CMOS		
Convert Command	Start Conversion			Falling Edge		
ACCURACY[2]						
Gain Error		+25°C		±0.6	±1.5	%
		Full		±1.1	±2.5	%
Gain Drift				±85		ppm/°C
Power-Supply Rejection of Gain	$\Delta +V_S = \pm5\%$	+25°C		0.01	0.15	%FSR/%
Input Offset Error		Full		±2.1	±3.5	%
Power-Supply Rejection of Offset	$\Delta +V_S = \pm5\%$	+25°C		0.02	0.15	%FSR/%
CONVERSION CHARACTERISTICS						
Sample Rate			10k		40M	Sample/s
Data Latency				6.5		Convert Cycle
DYNAMIC CHARACTERISTICS						
Differential Linearity Error	t_H = 13ns[3]					
f = 500kHz		+25°C		±0.5	±1.0	LSB
		0°C to +70°C		±0.6	±1.0	LSB
f = 12MHz		+25°C		±0.5	±1.0	LSB
		0°C to +70°C		±0.6	±1.0	LSB
No Missing Codes		0°C to +70°C		Tested		
Integral Linearity Error at f = 500kHz		0°C to +70°C		±0.5	±2.0	LSB
Spurious-Free Dynamic Range (SFDR)						
f = 500kHz (–1dBFS input)		+25°C	60	70		dBFS
		Full	54	67		dBFS
f = 12MHz (–1dBFS input)		+25°C	58	63		dBFS
		Full	54	62		dBFS

NOTES: (1) dBFS refers to dB below Full-Scale. (2) Percentage accuracies are referred to the internal A/D converter Full-Scale Range of 4Vp-p. (3) Refer to Timing Diagram footnotes for the differential linearity performance conditions for the SO and SSOP packages. (4) IMD is referred to the larger of the two input signals. If referred to the peak envelope signal (≈ 0dB), the intermodulation products will be 7dB lower. (5) Based on (SINAD – 1.76)/6.02. (6) No "rollover" of bits.

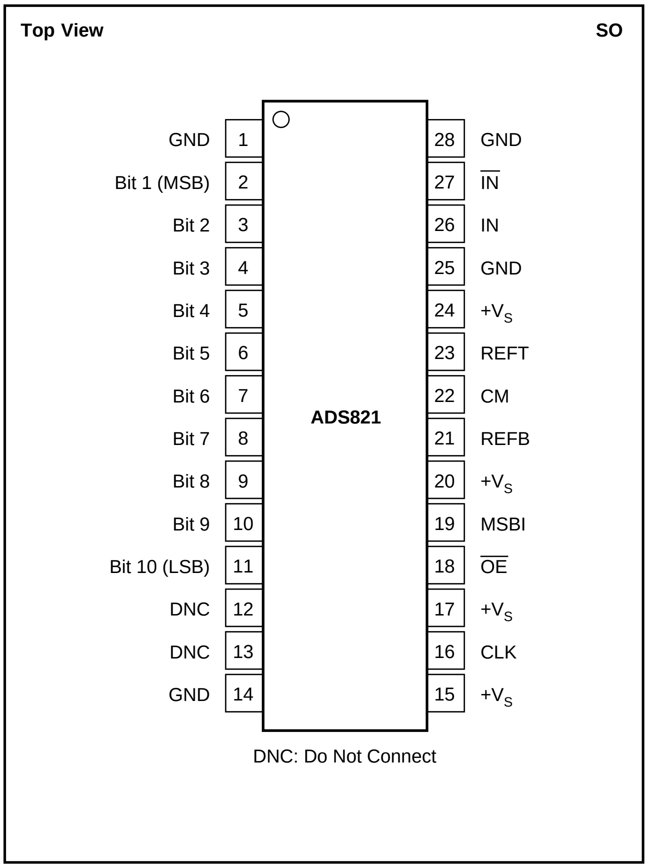
ELECTRICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, and with a 50% duty cycle clock having a 2ns rise-and-fall time, unless otherwise noted.

			ADS821U			
PARAMETER	**CONDITIONS**	**TEMP**	**MIN**	**TYP**	**MAX**	**UNITS**
DYNAMIC CHARACTERISTICS (Cont.)						
2-Tone Intermodulation Distortion (IMD)(4)						
f = 4.4MHz and 4.5MHz (–7dBFS each tone)		+25°C		–61		dBc
		Full		–60		dBc
Signal-to-Noise Ratio (SNR)						
f = 500kHz (–1dBFS input)		+25°C	57	59		dB
		Full	55	59		dB
f = 12MHz (–1dBFS input)		+25°C	56	58		dB
		Full	54	58		dB
Signal-to-(Noise + Distortion) (SINAD)						
f = 500kHz (–1dBFS input)		+25°C	56	58.5		dB
		Full	52	58		dB
f = 12MHz (–1dBFS input)		+25°C	53	57		dB
		Full	50	56		dB
Differential Gain Error	NTSC or PAL	+25°C		0.5		%
Differential Phase Error		NTSC or PAL	+25°C		0.1	
Degrees						
Effective Bits(5)	f_{IN} = 3.58MHz	+25°C		9.3		Bits
Aperture Delay Time		+25°C		2		ns
Aperture Jitter			+25°C		7	
ps rms						
Over-Voltage Recovery Time(6)	1.5x Full-Scale Input	+25°C		2		ns
OUTPUTS						
Logic Family				TTL/HCT Compatible CMOS		
Logic Coding	Logic Selectable			SOB or BTC		
Logic Levels	Logic LOW, C_L = 15pF max	Full	0		0.4	V
	Logic HIGH, C_L = 15pF max	Full	+2.5		$+V_S$	V
3-State Enable Time				20	40	ns
3-State Disable Time		Full		2	10	ns
POWER-SUPPLY REQUIREMENTS						
Supply Voltage: $+V_S$	Operating	Full	+4.75	+5	+5.25	V
Supply Current: $+I_S$	Operating	+25°C		76	88	mA
	Operating	Full		78	90	mA
Power Consumption	Operating	+25°C		380	440	mW
	Operating	Full		390	450	mW
Thermal Resistance, θ_{JA}					75	°C/W

NOTES: (1) dBFS refers to dB below Full Scale. (2) Percentage accuracies are referred to the internal A/D converter Full-Scale Range of 4Vp-p. (3) Refer to Timing Diagram footnotes for the differential linearity performance conditions for the SO and SSOP packages. (4) IMD is referred to the larger of the two input signals. If referred to the peak envelope signal (≈ 0dB), the intermodulation products will be 7dB lower. (5) Based on (SINAD – 1.76)/6.02. (6) No “rollover” of bits.

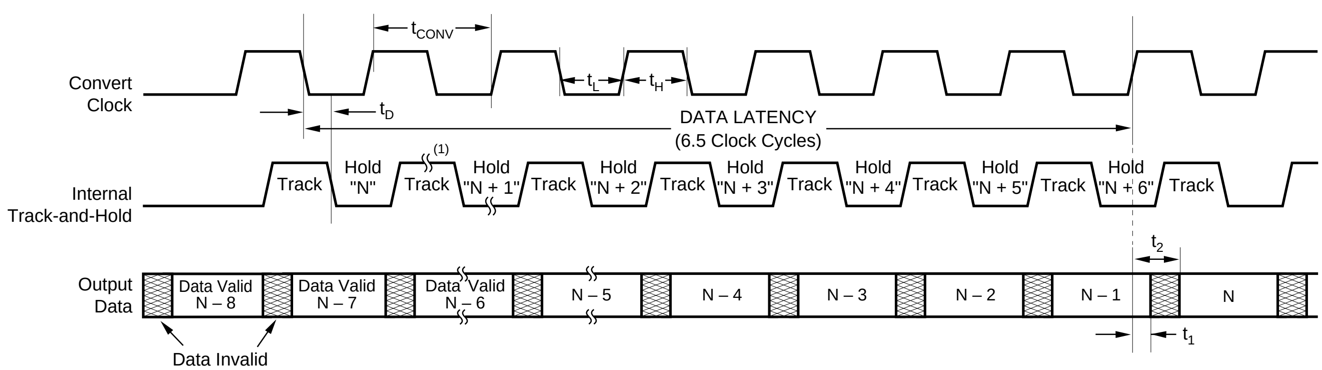
PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	GND	Ground
2	B1	Bit 1, Most Significant Bit (MSB)
3	B2	Bit 2
4	B3	Bit 3
5	B4	Bit 4
6	B5	Bit 5
7	B6	Bit 6
8	B7	Bit 7
9	B8	Bit 8
10	B9	Bit 9
11	B10	Bit 10, Least Significant Bit (LSB)
12	DNC	Do Not Connect
13	DNC	Do Not Connect
14	GND	Ground
15	$+V_S$	+5V Power Supply
16	CLK	Convert Clock Input, 50% Duty Cycle
17	$+V_S$	+5V Power Supply
18	$\overline{OE}$	HIGH: High-Impedance State. LOW or Floating: Normal Operation. Internal pull-down resistor.
19	MSBI	Most Significant Bit Inversion, HIGH: MSB inverted for complementary output. LOW or Floating: Straight output. Internal pull-down resistor.
20	$+V_S$	+5V Power Supply
21	REFB	Bottom Reference Bypass. For external bypassing of internal +1.25V reference.
22	CM	Common-Mode Voltage. It is derived by (REFT + REFB)/2.
23	REFT	Top Reference Bypass. For external bypassing of internal +3.25V reference.
24	$+V_S$	+5V Power Supply
25	GND	Ground
26	IN	Input
27	$\overline{IN}$	Complementary Input
28	GND	Ground

TIMING DIAGRAM

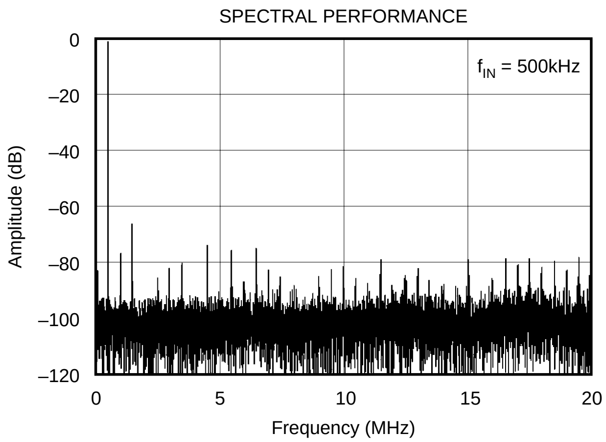


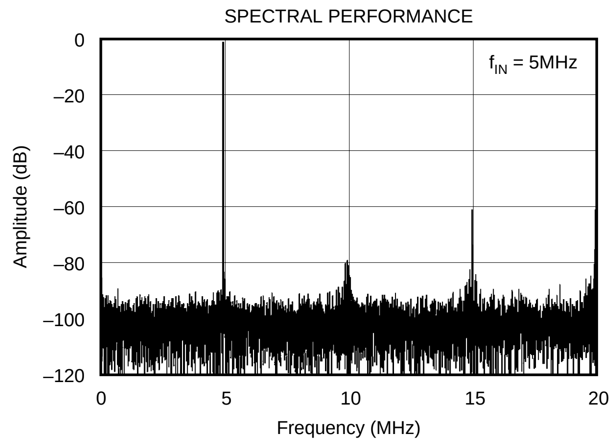
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	25		100µs	ns
t_L	Clock Pulse LOW	12	12.5		ns
t_H	Clock Pulse HIGH	12(2)	12.5		ns
t_D	Aperture Delay		2		ns
t_1	Data Hold Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max			12.5	ns

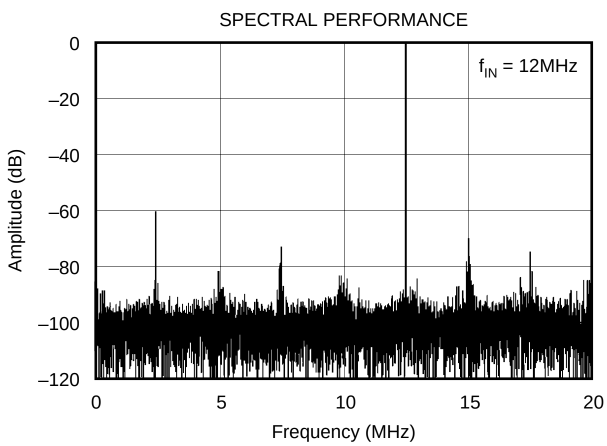
NOTES: (1) "⸾" indicates the portion of the waveform that will stretch out at slower sample rates. (2) t_H must be 13ns minimum if no missing codes is desired only for the conditions of $t_{CONV} \leq 28$ns and $f_{IN} < 2$MHz for the SO package. For best performance in the SSOP package, t_H must be 13ns minimum for all input frequencies and $t_{CONV} \leq 28$ns. Refer to the Clock Requirements for a possible clock skew circuit for this condition.

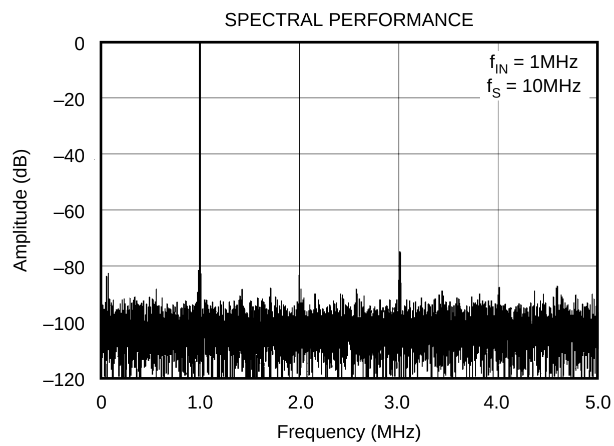
TYPICAL CHARACTERISTICS

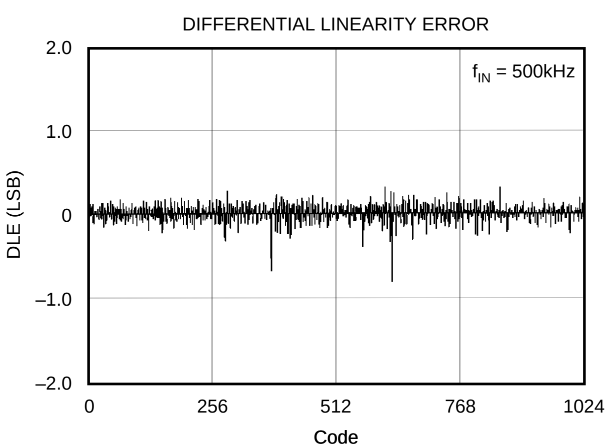
At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, and with a 50% duty cycle clock having a 2ns rise-and-fall time, unless otherwise noted.

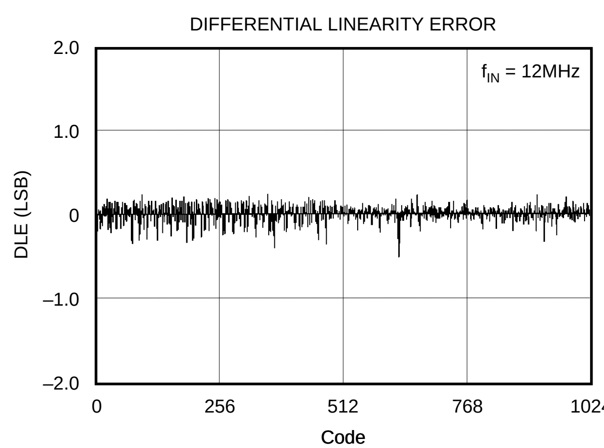












TYPICAL CHARACTERISTICS (Cont.)

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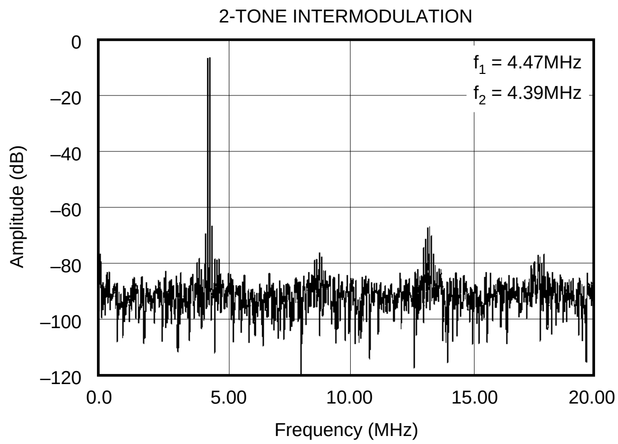
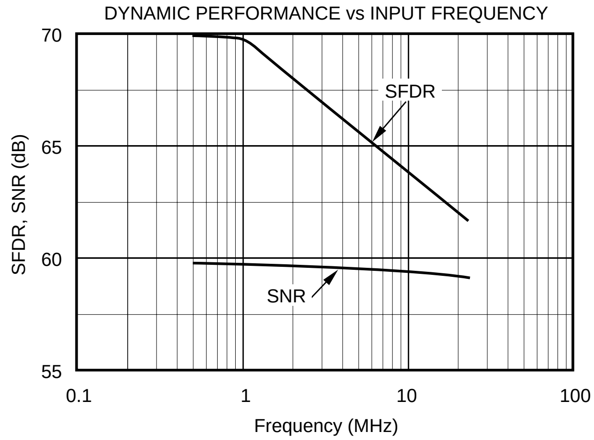
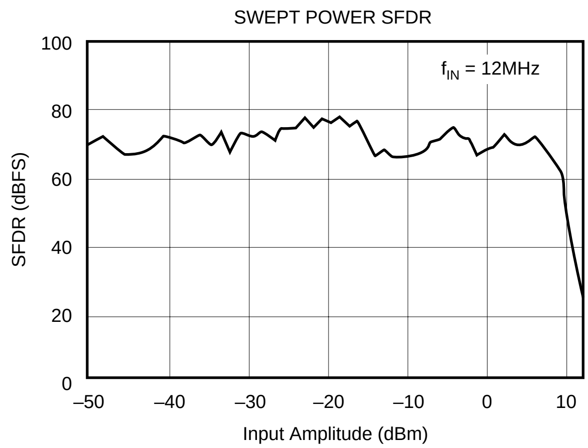
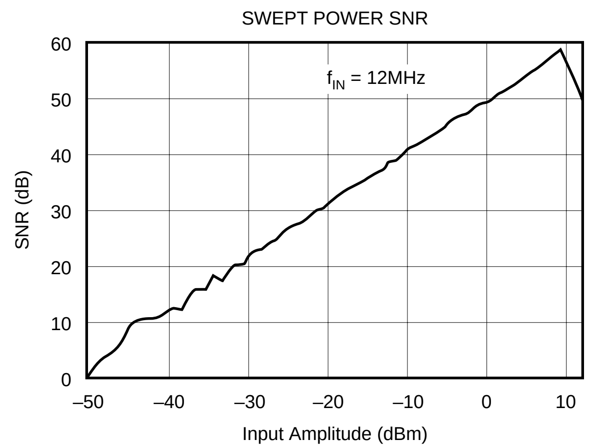
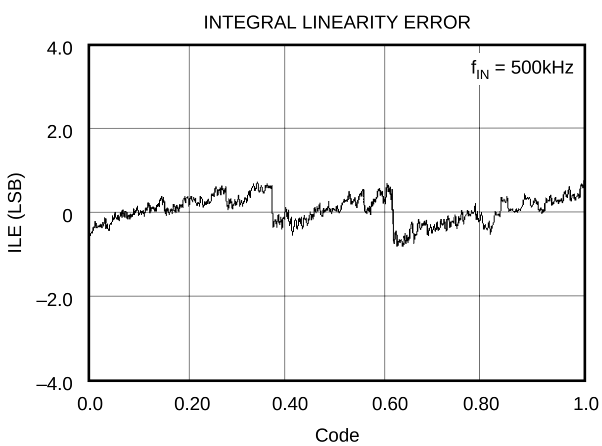
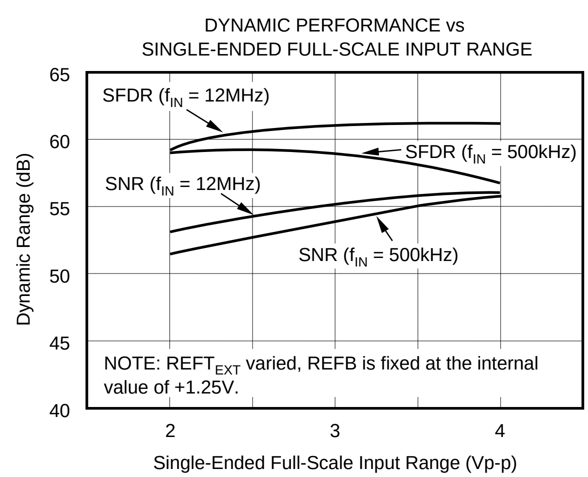




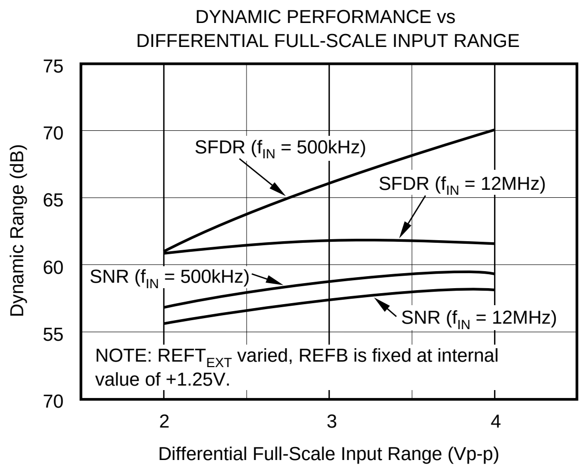


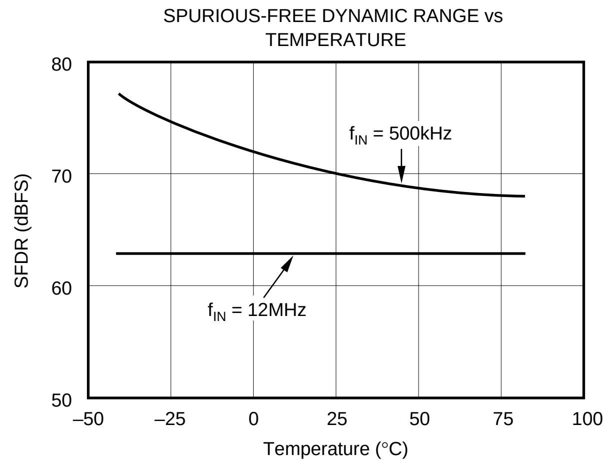


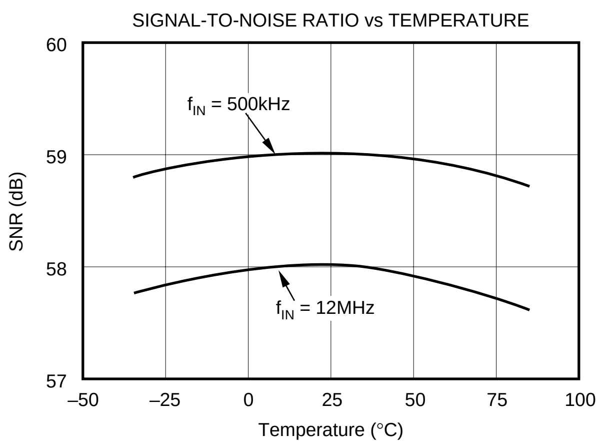


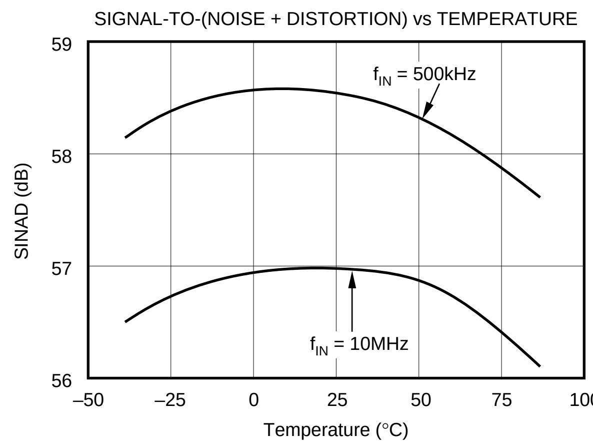


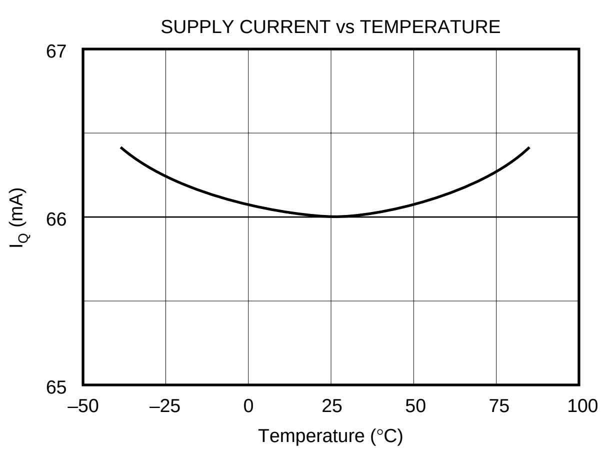
At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, and with a 50% duty cycle clock having a 2ns rise-and-fall time, unless otherwise noted.

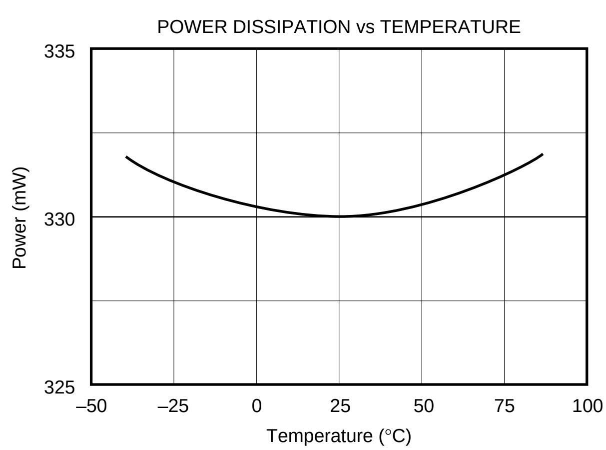




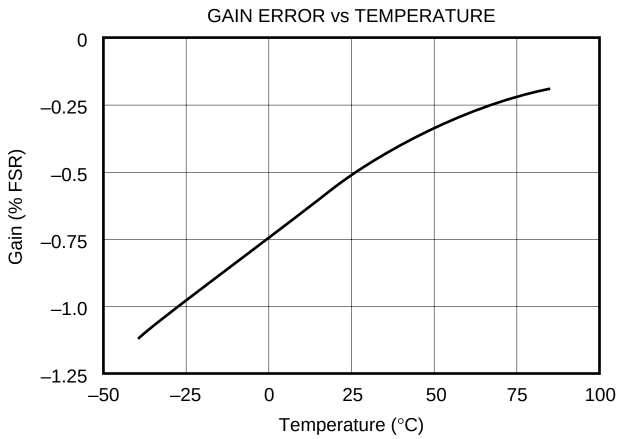


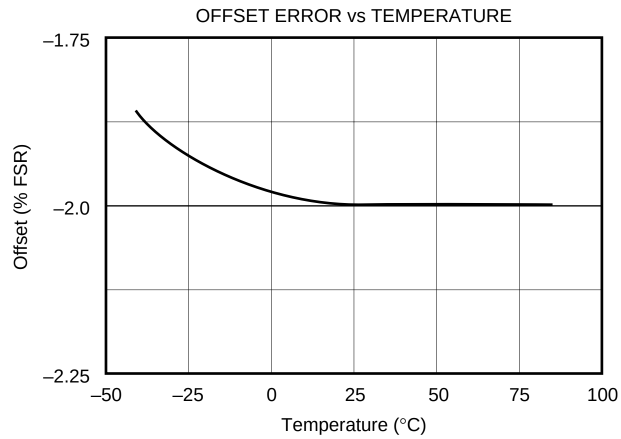


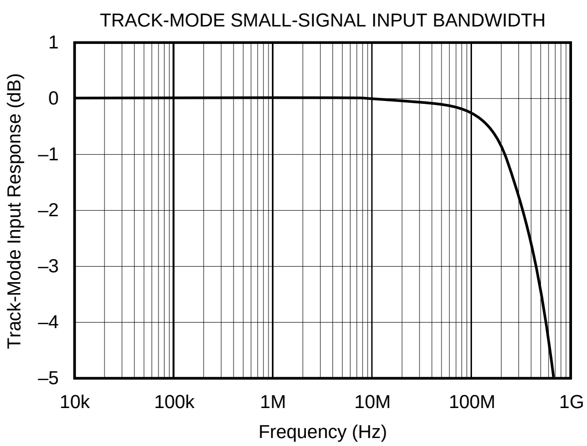


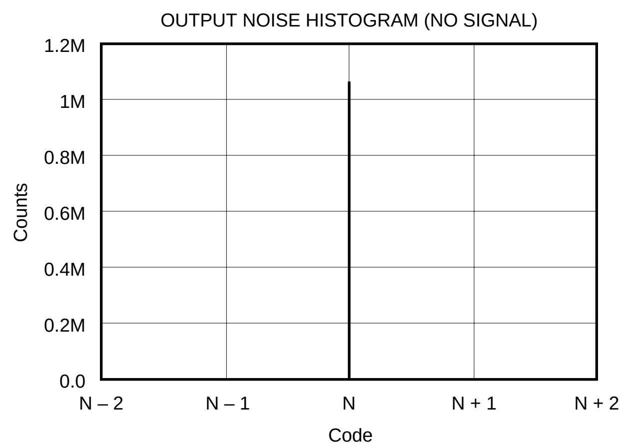


At T_A = +25°C, V_S = +5V, Sampling Rate = 40MHz, and with a 50% duty cycle clock having a 2ns rise-and-fall time, unless otherwise noted.









THEORY OF OPERATION

The ADS821 is a high-speed, sampling A/D converter with pipelining. It uses a fully differential architecture and digital error correction to ensure 10-bit resolution. The differential track-and-hold circuit is shown in Figure 1. The switches are controlled by an internal clock that has a non-overlapping 2-phase signal, $\phi 1$ and $\phi 2$. At the sampling time, the input signal is sampled on the bottom plates of the input capacitors. In the next clock phase, $\phi 2$, the bottom plates of the input capacitors are connected together and the feedback capacitors are switched to the op amp output. At this time, the charge redistributes between C_I and C_H, completing one track-and-hold cycle. The differential output is a held DC representation of the analog input at the sample time. The track-and-hold circuit can also convert a single-ended input signal into a fully differential signal for the quantizer.

The pipelined quantizer architecture has 9 stages with each stage containing a 2-bit quantizer and a 2-bit Digital-to-Analog Converter (DAC), as shown in Figure 2. Each 2-bit quantizer stage converts on the edge of the sub-clock, which is twice the frequency of the externally applied clock. The output of each quantizer is fed into its own delay line to

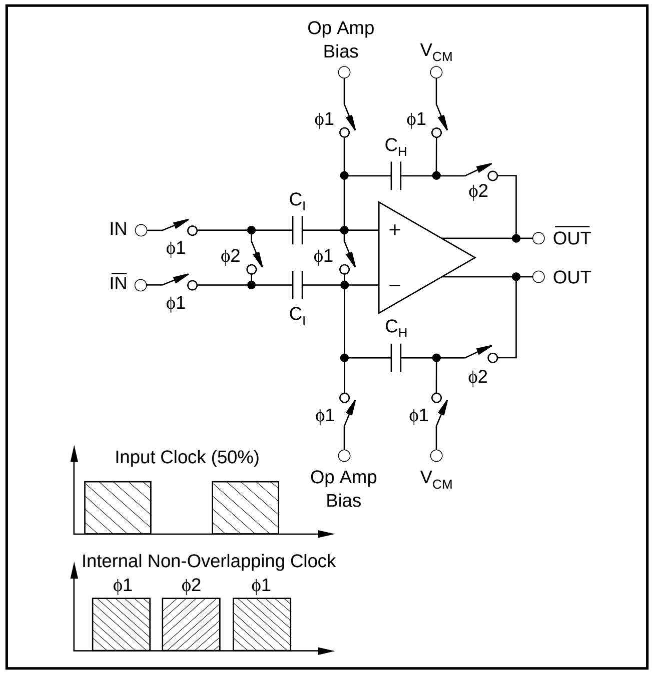


FIGURE 1. Input Track-and-Hold Configuration with Timing Signals.

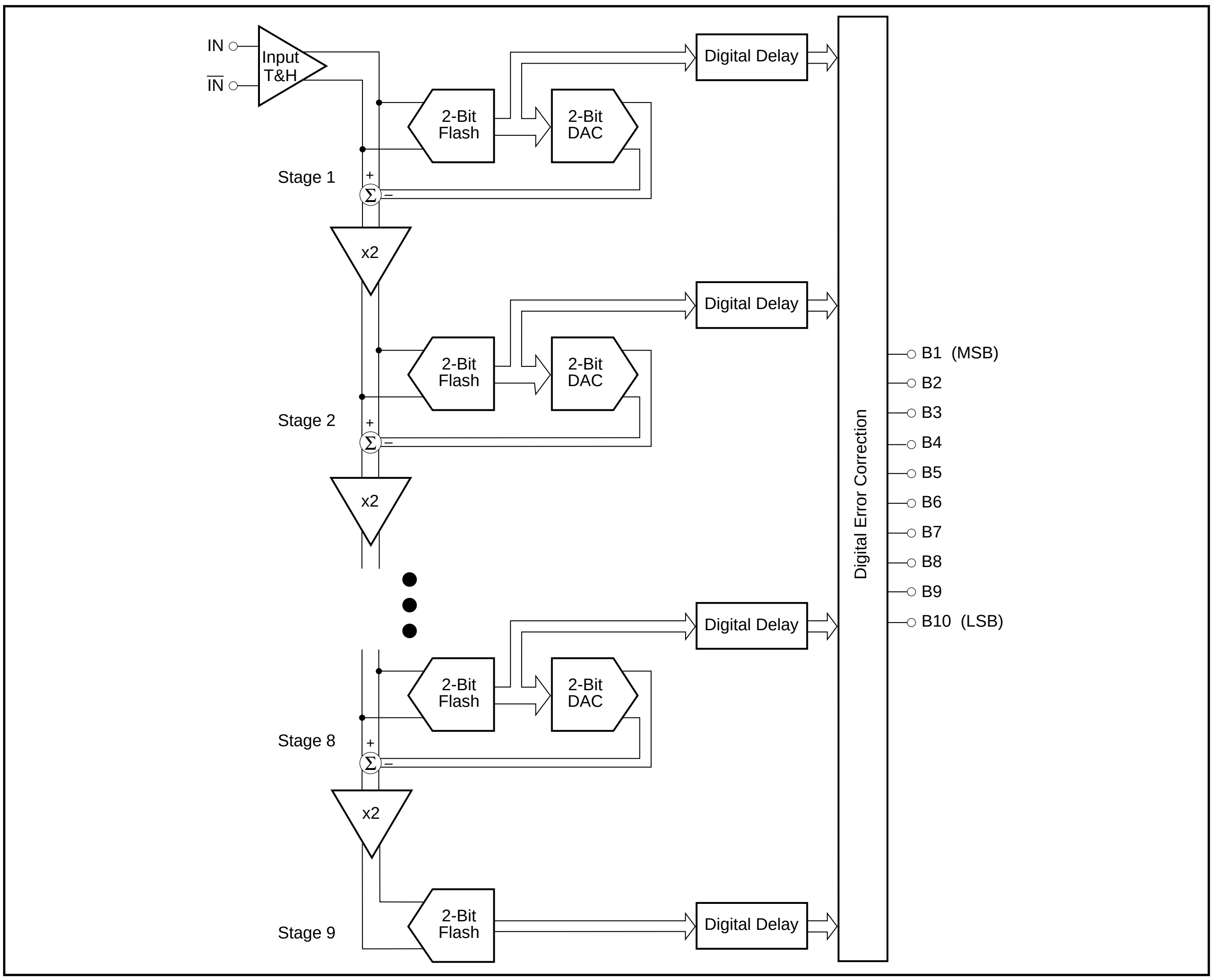


FIGURE 2. Pipeline A/D Converter Architecture.

time-align it with the data created from the following quantizer stages. This aligned data is fed into a digital error correction circuit that can adjust the output data based on the information found on the redundant bits. This technique gives the ADS821 excellent differential linearity and ensures no missing-codes at the 10-bit level.

The output data is available in Straight Offset Binary (SOB) or Binary Two's Complement (BTC) format.

THE ANALOG INPUT AND INTERNAL REFERENCE

The analog input of the ADS821 can be configured in various ways and driven with different circuits, depending on the nature of the signal and the level of performance desired. The ADS821 has an internal reference that sets the full-scale input range of the A/D converter. The differential input range has each input centered around the common-mode of +2.25V, with each of the two inputs having a full-scale range of +1.25V to +3.25V. Since each input is 2Vp-p and 180° out-of-phase with the other, a 4V differential input signal to the quantizer results. As shown in Figure 3, the positive full-scale reference (REFT) and the negative full-scale reference (REFB) are brought out for external bypassing. In addition, the common-mode (CM) voltage may be used as a reference to provide the appropriate offset for the driving circuitry. However, care must be taken not to appreciably load this reference node. For more information regarding external references, single-ended inputs, and ADS821 drive circuits, refer to the applications section.

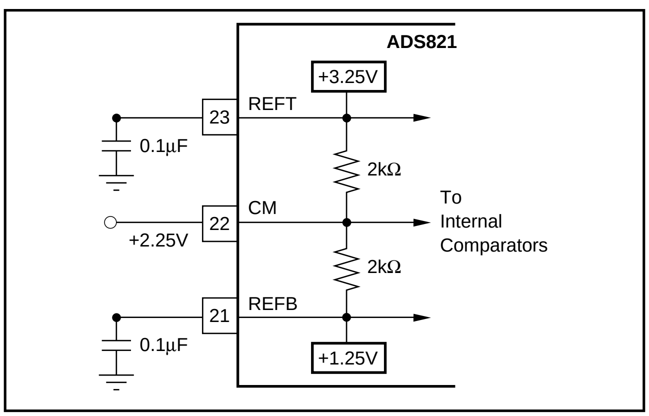


FIGURE 3. Internal Reference Structure.

CLOCK REQUIREMENTS

The CLK pin accepts a CMOS level clock input. Both the rising and falling edges of the externally applied clock controls the various interstage conversions in the pipeline. Therefore, the clock signal's jitter, rise-and-fall times and duty cycle can affect conversion performance.

- Low clock **jitter** is critical to SNR performance in frequency-domain signal environments.
- Clock **rise and fall times** should be as short as possible (< 2ns for best performance).
- For most applications, the clock duty should be set to 50%. For applications requiring no missing codes, however, a slight skew in the duty cycle will improve DNL performance for conversion rates > 35MHz and input frequencies < 2MHz (see Timing Diagram) in the SO package. For the best performance in the SSOP package, the clock should be skewed under all input frequencies with conversion rates > 35MHz. A possible method for skewing the 50% duty cycle source is shown in Figure 4.

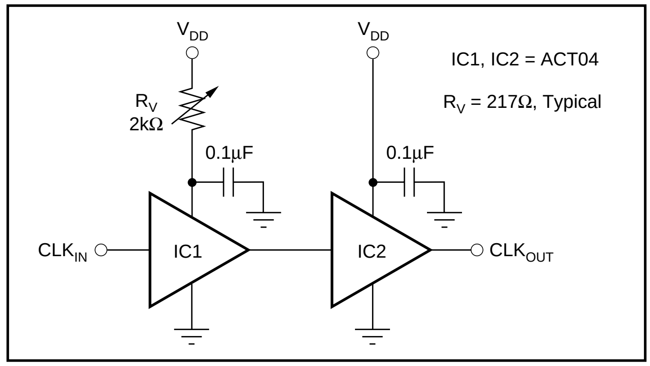


FIGURE 4. Clock Skew Circuit.

DIGITAL OUTPUT DATA

The 10-bit output data is provided at CMOS logic levels. There is a 6.5 clock cycle data latency from the start convert signal to the valid output data. The standard output coding is Straight Offset Binary where a full-scale input signal corresponds to all "1's" at the output. This condition is met with pin 19 LOW or Floating due to an internal pull-down resistor. By applying a high voltage to this pin, a BTC output will be provided where the most significant bit is inverted. The digital outputs of the ADS821 can be set to a high impedance state by driving $\overline{OE}$ (pin 18) with a logic HIGH. Normal operation is achieved with pin 18 LOW or Floating due to internal pull-down resistors. This function is provided for testability purposes and is not meant to drive digital buses directly or be dynamically changed during the conversion process.

	OUTPUT CODE	
DIFFERENTIAL INPUT(1)	**SOB PIN 19 FLOATING or LOW**	**BTC PIN 19 HIGH**
+FS (IN = +3.25V, $\overline{IN}$ = +1.25V)	1111111111	0111111111
+FS – 1LSB	1111111111	0111111111
+FS – 2LSB	1111111110	0111111110
+3/4 Full-Scale	1110000000	0110000000
+1/2 Full-Scale	1100000000	0100000000
+1/4 Full-Scale	1010000000	0010000000
+1LSB	1000000001	0000000001
Bipolar Zero (IN = $\overline{IN}$ = +2.25V)	1000000000	0000000000
–1LSB	0111111111	1111111111
–1/4 Full-Scale	0110000000	1110000000
–1/2 Full-Scale	0100000000	1100000000
–3/4 Full-Scale	0010000000	1010000000
–FS + 1LSB	0000000001	1000000001
–FS (IN = +1.25V, $\overline{IN}$ = +3.25V)	0000000000	1000000000

NOTE: (1) In the single-ended input mode, +FS = +4.25V and –FS = +0.25V.

TABLE I. Coding Table for the ADS821.

APPLICATIONS

DRIVING THE ADS821

The ADS821 has a differential input with a common-mode of +2.25V. For AC-coupled applications, the simplest way to create this differential input is to drive the primary winding of a transformer with a single-ended input. A differential output is created on the secondary if the center tap is tied to the common-mode (CM) voltage of +2.25V, as per Figure 5. This transformer-coupled input arrangement provides good high-frequency AC performance. It is important to select a transformer that gives low distortion and does not exhibit core saturation at full-scale voltage levels. Since the transformer does not appreciably load the ladder, there is no need to buffer the CM output in this instance. In general, it is advisable to keep the current draw from the CM output pin below 0.5µA to avoid nonlinearity in the internal reference ladder. A FET input operational amplifier such as the OPA130 can provide a buffered reference for driving external circuitry. The analog IN and $\overline{\text{IN}}$ inputs should be bypassed with 22pF capacitors to minimize track-and-hold glitches and to improve high-input frequency performance.

Figure 6 shows an AC-coupled single-ended input interface circuit using the low-cost, current feedback OPA694 as the active gain stage. When testing this configuration in gains of +4, +5.8, and +8.2, it was noted that reducing the feedback resistor of the OPA694 from the typical 402Ω to 360Ω resulted in a wider bandwidth, thus improving distortion at higher gains. The gain resistor was scaled to 120Ω, 75Ω, and 50Ω for each of the three gain settings. The two 330Ω resistors set the RC time constant and the values can be varied, although higher values will have the effect of moving the corner frequency of the created high-pass filter down. In Figure 6, the –3dB point is set at 4.2kHz.

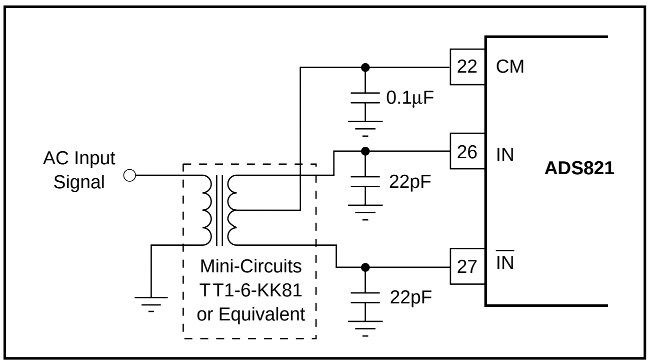


FIGURE 5. AC-Coupled, Single-Ended to Differential Drive Circuit Using a Transformer.

Figure 7 illustrates another possible low-cost interface circuit that utilizes resistors and capacitors in place of a transformer. Depending on the signal bandwidth, the component values should be carefully selected in order to maintain the performance outlined in the data sheet. The input capacitors, C_{IN}, and the input resistors, R_{IN}, create a high-pass filter with the lower corner frequency at $f_C = 1/(2\pi R_{IN} C_{IN})$. The corner frequency can be reduced by either increasing the value of R_{IN} or C_{IN}. If the circuit operates with a 50Ω or 75Ω impedance level, the resistors are fixed and only the value of the capacitor can be increased. Usually AC-coupling capacitors are electrolytic or tantalum capacitors with values of 1mF or higher. It should be noted that these large capacitors become inductive with increased input frequency, which could lead to signal amplitude errors or oscillation. To maintain a low AC-coupling impedance throughout the signal band, a small value (e.g. 1µF) ceramic capacitor could be added in parallel with the polarized capacitor.

Capacitors C_{SH1} and C_{SH2} are used to minimize current glitches resulting from the switching in the input track-and-hold stage and to improve signal-to-noise performance. These capacitors can also be used to establish a low-pass filter and effectively reduce the noise bandwidth. In order to create a real pole, resistors R_{SER1} and R_{SER2} were added in series with each input. The cut off frequency of the filter is determined by $f_C = 1/(2\pi R_{SER} \bullet (C_{SH} + C_{ADC}))$ where R_{SER} is the resistor in series with the input, C_{SH} is the external capacitor from the input to ground, and C_{ADC} is the internal input capacitance of the A/D converter (typically 4pF).

Resistors R_1 and R_2 are used to derive the necessary common-mode voltage from the buffered top and bottom references. The total load of the resistor string should be selected

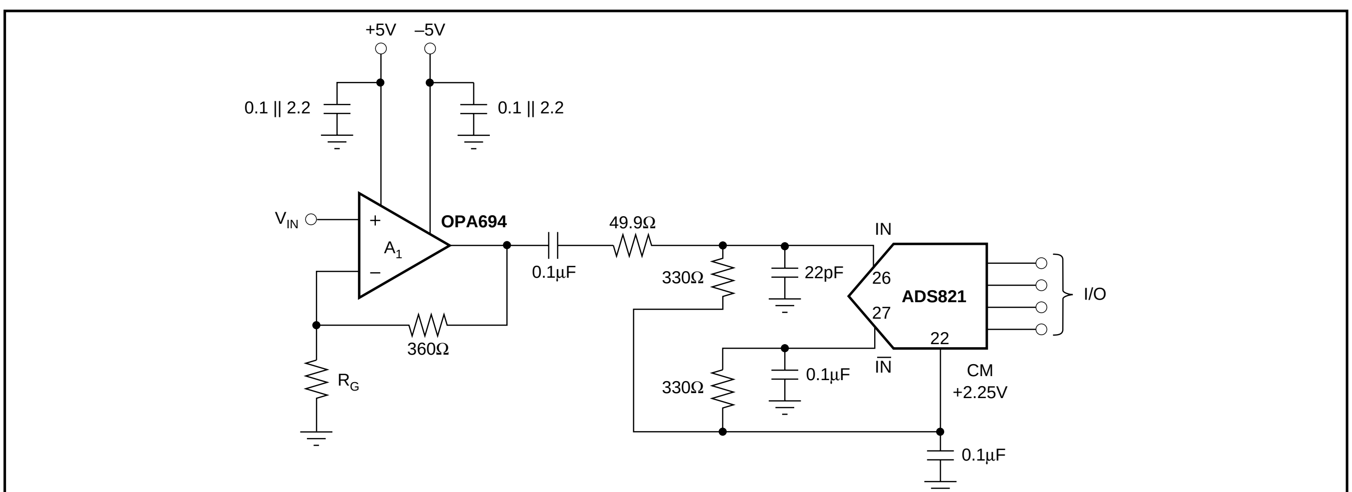


FIGURE 6. Low-Cost, AC-Coupled, Single-Ended Input Circuit.

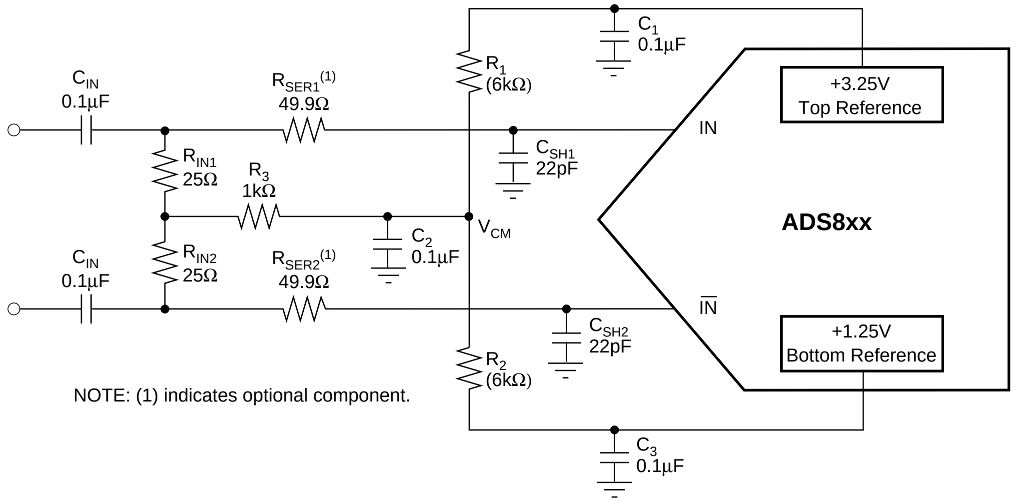


FIGURE 7. AC-Coupled Differential Input Circuit.

so that the current does not exceed 1mA. Although the circuit in Figure 7 uses two resistors of equal value so that the common-mode voltage is centered between the top and bottom reference (+2.25V), it is not necessary to do so. In all cases the center point, V_{CM}, should be bypassed to ground in order to provide a low-impedance AC ground.

If the signal needs to be DC-coupled to the input of the ADS821, an operational amplifier input circuit is required. In the differential input mode, any single-ended signal must be modified to create a differential signal. This can be accomplished by using two operational amplifiers, one in the noninverting mode for the input and the other amplifier in the inverting mode for the complementary input. The low-distortion circuit in Figure 8 will provide the necessary input shifting required for signals centered around ground. It also employs a diode for output level shifting to ensure a low-distortion +3.25V output swing. See Figure 9 for another DC-coupled circuit. Other amplifiers can be used in place of the OPA860 if the lowest distortion is not necessary. If output level shifting circuits are not used, care must be taken to select operational amplifiers that give the necessary performance when swinging to +3.25V with a ±5V supply operational amplifier. The OPA620 and OPA621, or the lower power OPA650 or OPA820 can be used in place of the OPA860 in Figure 8. In that configuration, the OPA820 will typically swing to within 100mV of positive full scale.

The ADS821 can also be configured with a single-ended input full-scale range of +0.25V to +4.25V by tying the complementary input to the common-mode reference voltage, see Figure 10. This configuration will result in increased even-order harmonics, especially at higher input frequencies. This tradeoff, however, may be quite acceptable for time-domain applications. The driving amplifier must give adequate performance with a +0.25V to +4.25V output swing in this case.

EXTERNAL REFERENCES AND ADJUSTMENT OF FULL-SCALE RANGE

The internal-reference buffers are limited to approximately 1mA of output current. As a result, these internal +1.25V and +3.25V references may be overridden by external references that have at least 18mA (at room temperature) of output drive capability. In this instance, the common-mode voltage will be set halfway between the two references. This feature can be used to adjust the gain error, improve gain drift, or to change the full-scale input range of the ADS821. Changing the full-scale range to a lower value has the benefit of easing the swing requirements of external input amplifiers. The external references can vary as long as the value of the external top reference ($REFT_{EXT}$) is less than or equal to +3.4V, the value of the external bottom reference ($REFB_{EXT}$) is greater than or equal to +1.1V, and the difference between the external references are greater than or equal to 800mV.

For the differential configuration, the full-scale input range will be set to the external reference values that are selected. For the single-ended mode, the input range is $2 \bullet (REFT_{EXT} – REFB_{EXT})$, with the common-mode being centered at $(REFT_{EXT} + REFB_{EXT})/2$. Refer to the Typical Characteristics for expected performance versus full-scale input range.

The circuit in Figure 11 works completely on a single +5V supply. As a reference element, it uses the *micro*Power reference REF1004-2.5, which is set to a quiescent current of 0.1mA. Amplifier A_2 is configured as a follower to buffer the +1.25V generated from the resistor divider. To provide the necessary current drive, a pull-down resistor (R_P) is added.

Amplifier A_1 is configured as an adjustable gain stage, with a range of approximately 1 to 1.32. The pull-up resistor again relieves the op amp from providing the full current drive. The value of the pull-up, pull-down resistors is not critical and can be varied to optimize power consumption. The need for pull-up, pull-down resistors depends only on the drive capability of the selected drive amplifier and thus can be omitted.

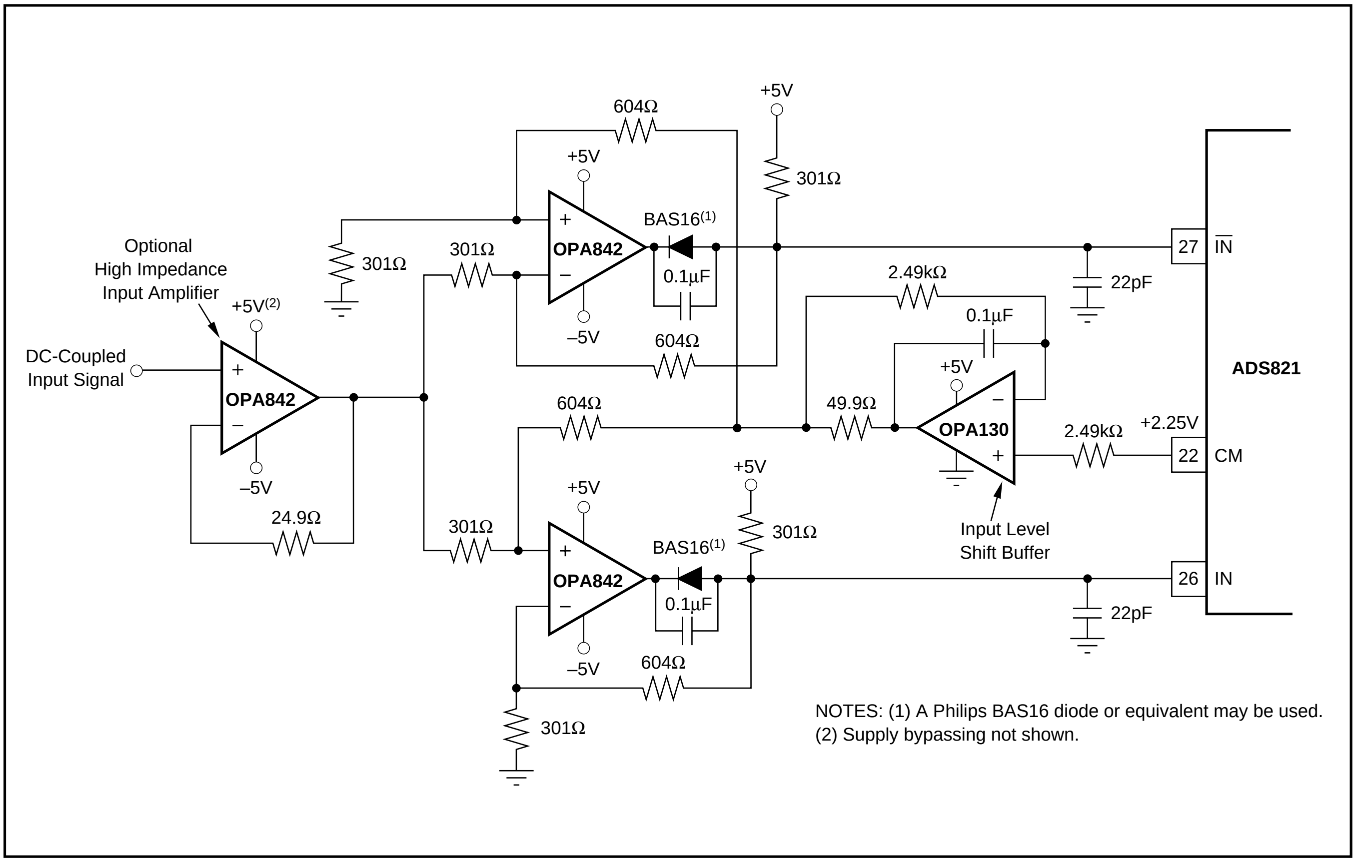


FIGURE 8. A Low-Distortion DC-Coupled, Single-Ended to Differential Input Driver Circuit.

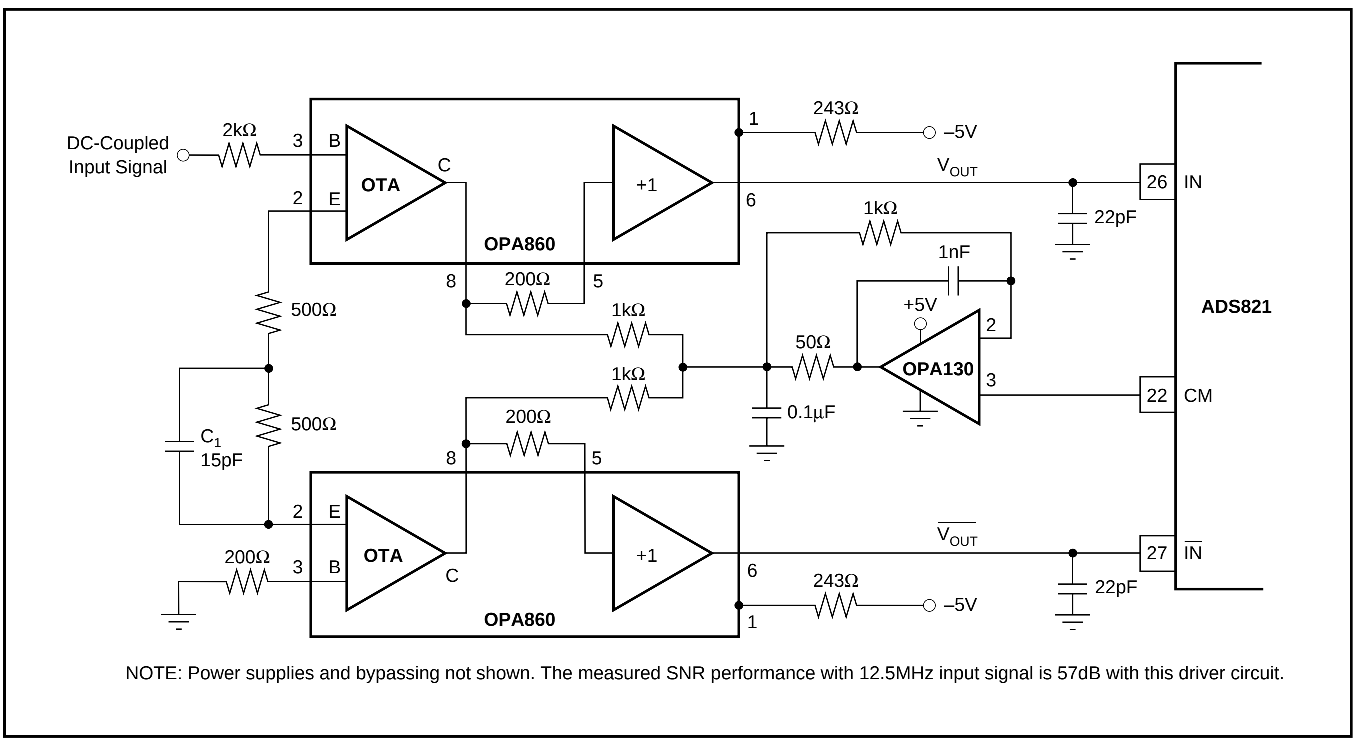


FIGURE 9. A Wideband DC-Coupled, Single-Ended to Differential Input Driver Circuit.

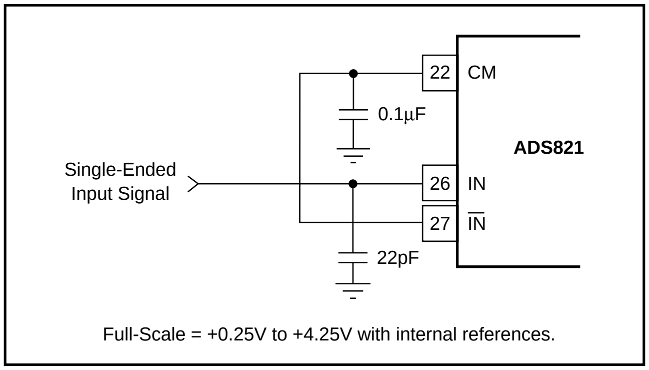


FIGURE 10. Single-Ended Input Connection.

PC-BOARD LAYOUT AND BYPASSING

A well-designed, clean PC-board layout will assure proper operation and clean spectral response. Proper grounding and bypassing, short lead lengths, and the use of ground planes are particularly important for high-frequency circuits. Multilayer PC-boards are recommended for best performance but if carefully designed, a two-sided PC-board with large, heavy ground planes can give excellent results. It is recommended that the analog and digital ground pins of the ADS821 be connected directly to the analog ground plane. In our experience, this gives the most consistent results. The A/D converter power-supply commons should be tied together at the analog ground plane. Power supplies should be bypassed with 0.1µF ceramic capacitors as close to the pin as possible.

DYNAMIC PERFORMANCE TESTING

The ADS821 is a high-performance converter and careful attention to test techniques is necessary to achieve accurate results. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using data windowing functions. A low jitter signal generator, such as the HP8644A for the test signal, phase-locked with a low jitter HP8022A pulse generator for the A/D converter clock, gives excellent results. Low-pass filtering (or bandpass filtering) of test signals is absolutely necessary to test the low distortion of the ADS821. Using a signal amplitude slightly lower than full scale will allow a small amount of “headroom” so that noise or DC offset voltage will not overrange the A/D converter and cause clipping on signal peaks.

DYNAMIC PERFORMANCE DEFINITIONS

1. Signal-to-Noise-and-Distortion Ratio (SINAD):

$$10\log\frac{\text{Sinewave Signal Power}}{\text{Noise} + \text{Harmonic Power (first 15 harmonics)}}$$

2. Signal-to-Noise Ratio (SNR):

$$10\log\frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Intermodulation Distortion (IMD):

$$10\log\frac{\text{Highest IMD Product Power (to 5th-order)}}{\text{Sinewave Signal Power}}$$

IMD is referenced to the larger of the test signals f_1 or f_2. Five “bins” either side of peak are used for calculation of fundamental and harmonic power. The “0” frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

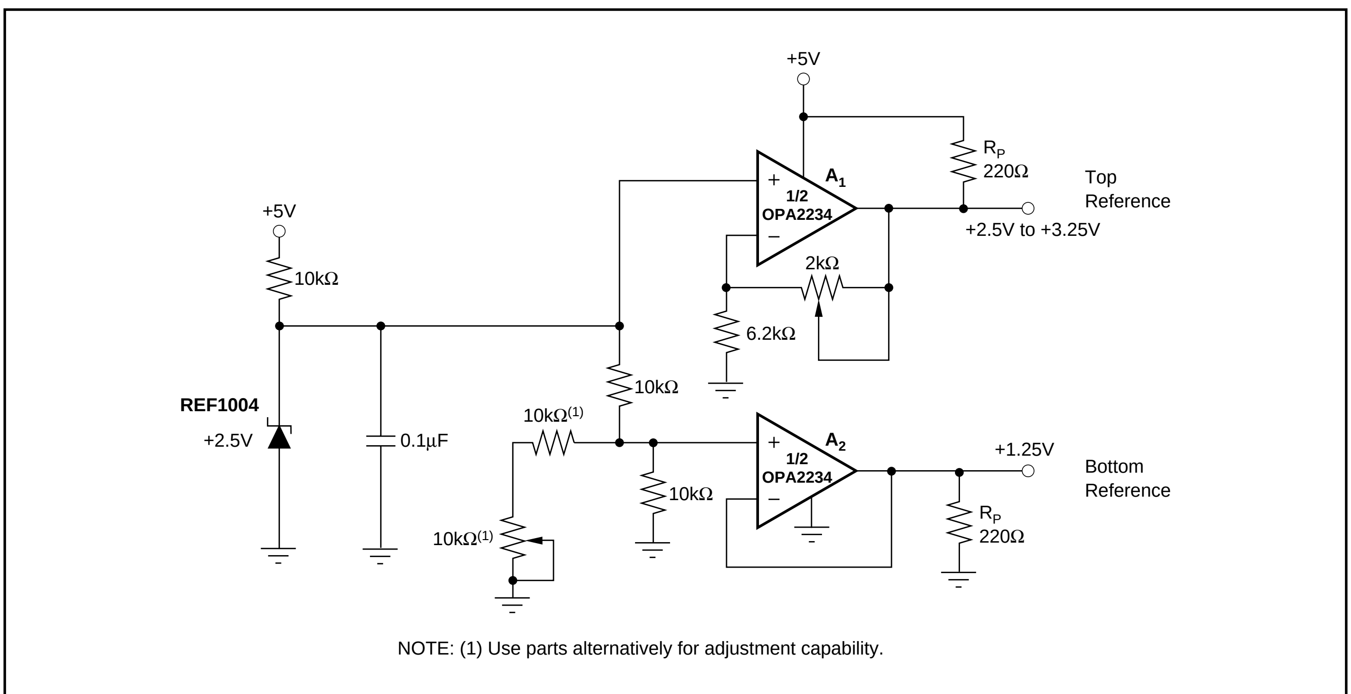


FIGURE 11. Optional External Reference to Set the Full-Scale Range Utilizing a Dual, Single-Supply Op Amp.

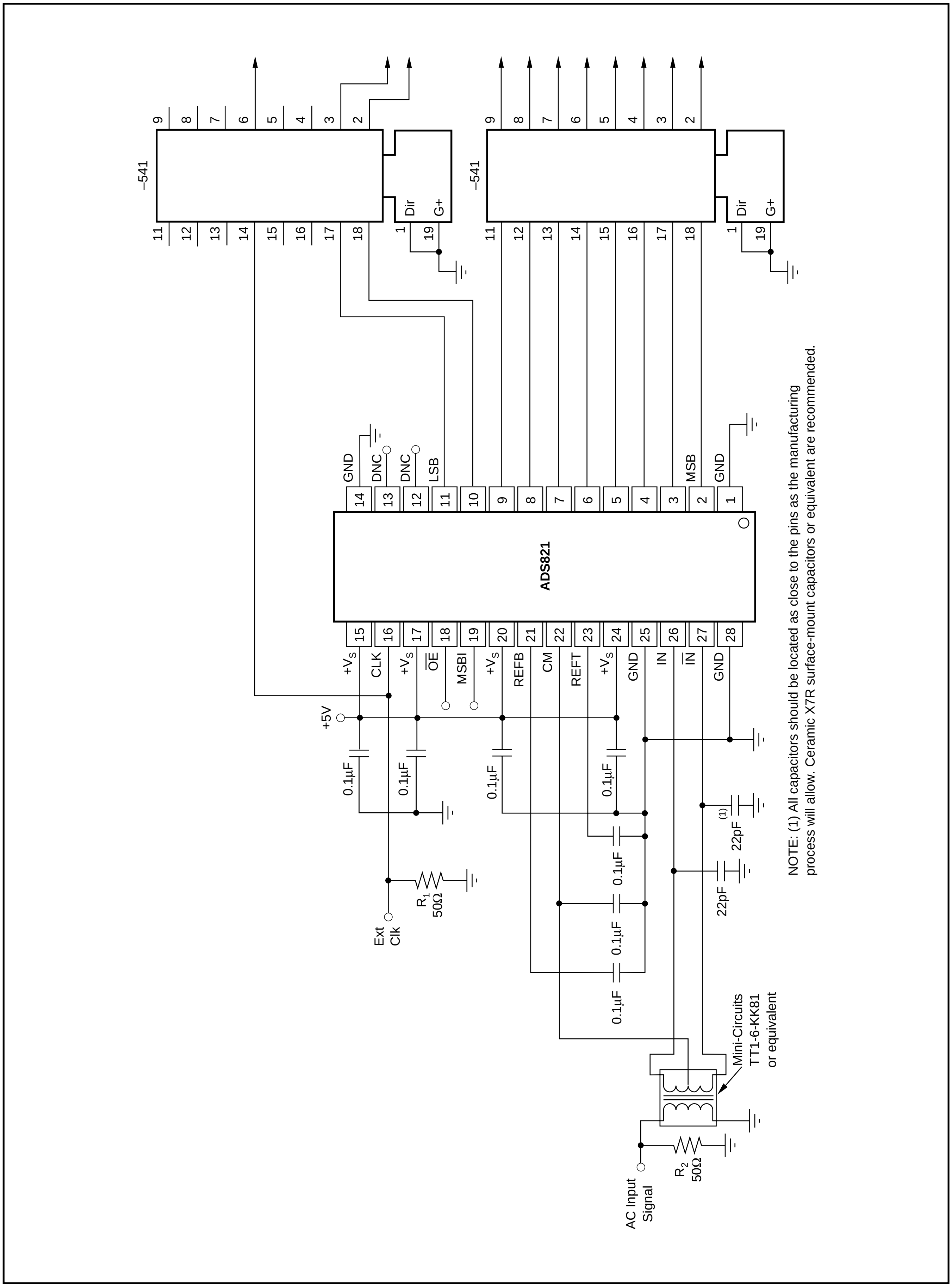


FIGURE 12. ADS821 Interface Schematic with AC-Coupling and External Buffers.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS821U	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS821U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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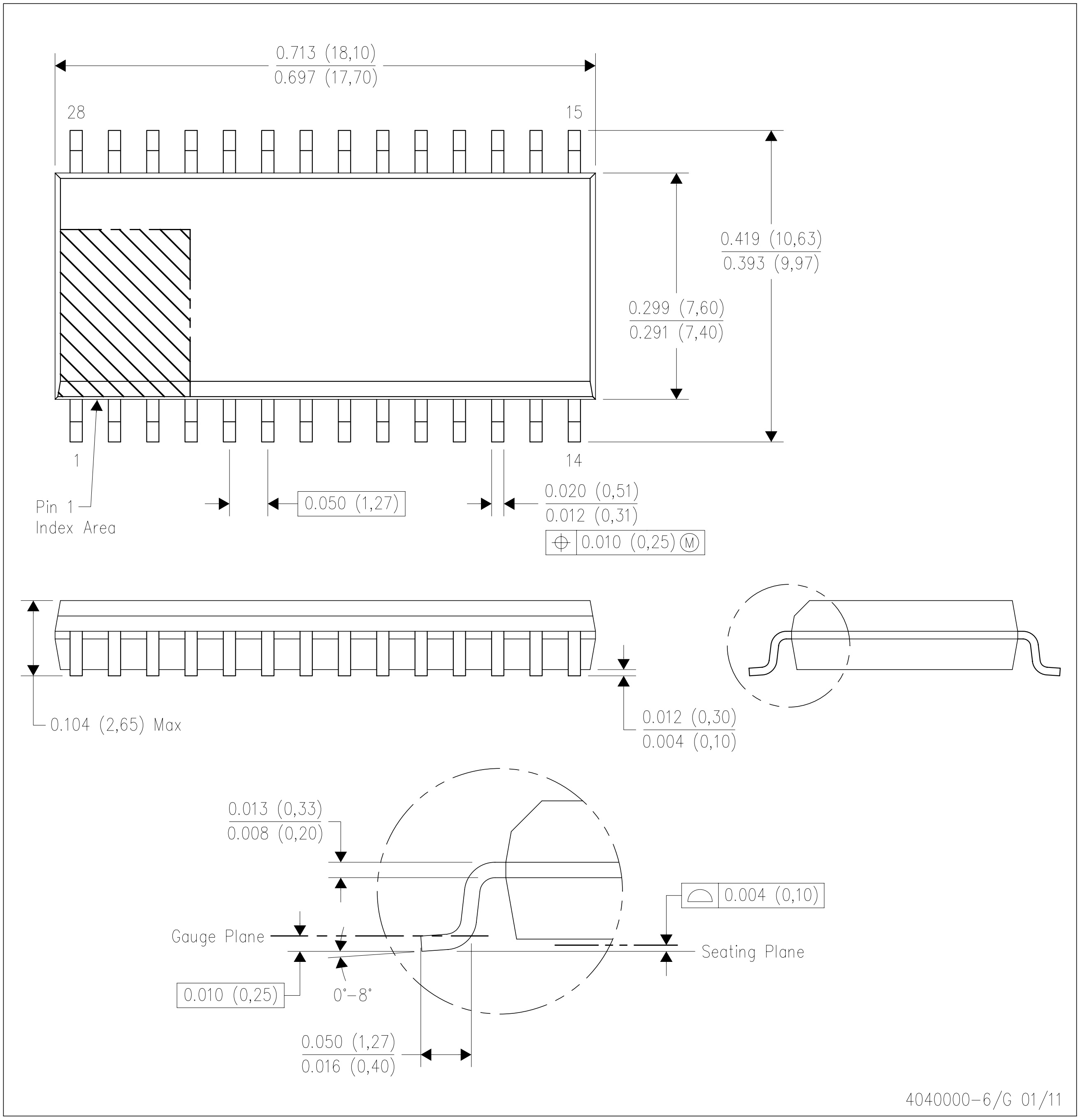
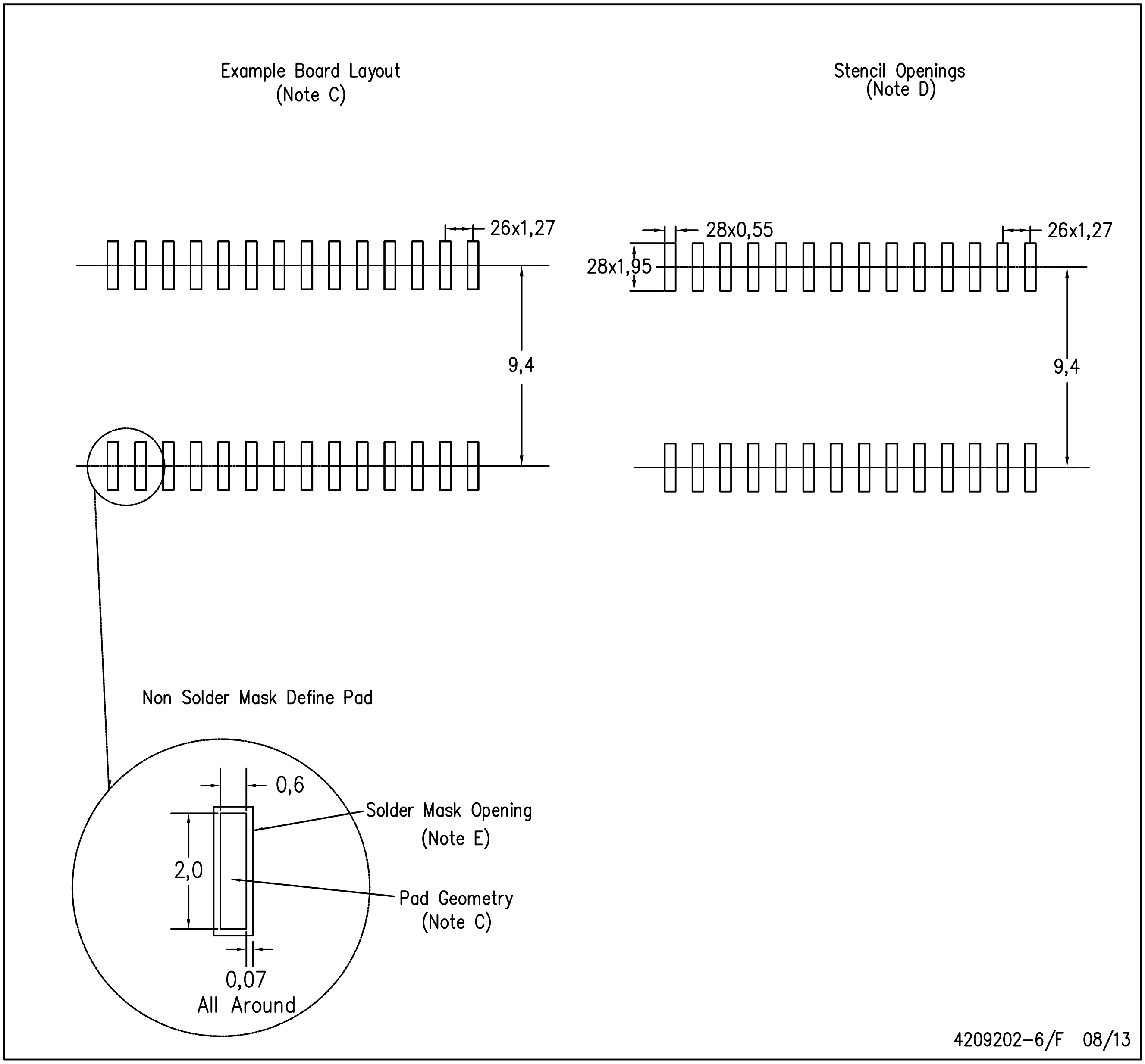
DW (R-PDSO-G28) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AE.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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