Ultra-Low On-Resistance, 4-A Integrated Load Switch with Controlled Turn-on

Check for Samples: TPS22920

FEATURES

- **Integrated Load Switch**
- **Input Voltage Range: 0.75-V to 3.6-V**
- **Integrated Pass-FET r_{DSON} = 2mΩ (typ) at 3.6-V**
- **Ultra-Low ON-Resistance**
  - **r_{ON} = 5.3-mΩ at 3.6-V**
  - **r_{ON} = 5.4-mΩ at 2.5-V**
  - **r_{ON} = 5.5-mΩ at 1.8-V**
  - **r_{ON} = 5.8-mΩ at 1.2-V**
  - **r_{ON} = 6.1-mΩ at 1.05-V**
  - **r_{ON} = 7.3-mΩ at 0.75-V**
- **Ultra Small CSP-8 package 0.9mm×1.9mm, 0.5mm pitch**
- **4-A Maximum Continuous Switch Current**
- **Shutdown Current 5.5-µA max**
- **Low Threshold Control Input**
- **Controlled slew- rate to avoid inrush current**
- **Quick Output Discharge Transistor**
- **ESD Performance Tested Per JESD 22**
  - **4000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

APPLICATIONS

- **Notebook / Netbook Computer**
- **Tablet PC**
- **PDAs / Smartphones**
- **GPS Navigation Devices**
- **MP3 Players**

DESCRIPTION

The TPS22920 is a small, ultra-low r_{ON} load switch with controlled turn on. The device contains a N-channel MOSFET that can operate over an input voltage range of 0.75 V to 3.6 V and switch currents up to 4-A. An integrated charge pump biases the NMOS switch in order to achieve a minimum switch ON resistance (r_{ON}). The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals.

The TPS22920 has a 1250-Ω on-chip load resistor for quick output discharge when the switch is turned off.

The TPS22920 has an internally controlled rise time in order to reduce inrush current. The TPS22920 features a rise time of 880µS at 3.6-V.

The TPS22920 is available in an ultra-small, space-saving 8-pin CSP package and is characterized for operation over the free-air temperature range of –40°C to 85°C.

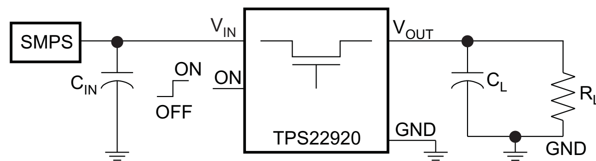


Figure 1. Typical Application

FEATURE LIST

	r_{ON} (typ) at 3.6 V	RISE TIME (typ) at 3.6V	QUICK OUTPUT DISCHARGE(1)	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22920	5.3- mΩ	880 µS	Yes	4-A	Active High

(1) This feature discharges the output of the switch to ground through a 1250-Ω resistor, preventing the output from floating. See Application section 'Output Pull-Down'

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

YZP PACKAGE

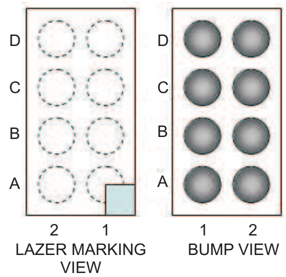


Figure 2. Bump Assignments

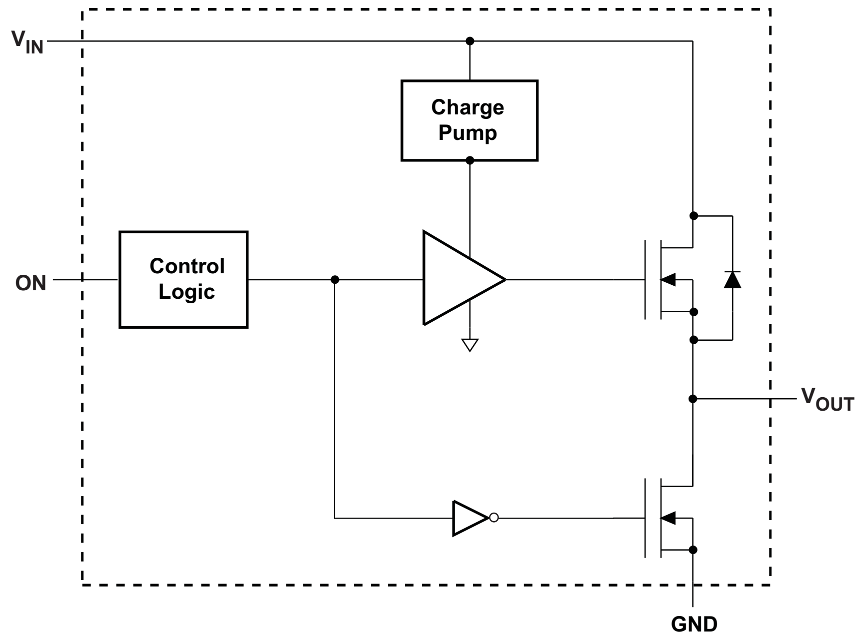
Bump Assignments (YZP Package)

D	GND	ON
C	V_{OUT}	V_{IN}
B	V_{OUT}	V_{IN}
A	V_{OUT}	V_{IN}
	1	**2**

Pin Description

TPS22920	**PIN NAME**	**DESCRIPTION**
YZP		
D1	GND	Ground
D2	ON	Switch control input, active high. Do not leave floating
A1, B1, C1	VOUT	Switch output
A2, B2, C2	VIN	Switch input, bypass this input with a ceramic capacitor to ground

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

ON	VIN to VOUT	VOUT to GND(1)
L	OFF	ON
H	ON	OFF

(1) See Application section 'Output Pull-Down'

ABSOLUTE MAXIMUM RATINGS(1)

			VALUE	UNIT
V_{IN}	Input voltage range		–0.3 to 4	V
V_{OUT}	Output voltage range		VIN + 0.3	V
V_{ON}	Input voltage range		–0.3 to 4	V
I_{MAX}	Maximum Continuous Switch Current		4	A
I_{PLS}	Maximum Pulsed Switch Current, pulse <300µS, 2% duty cycle		6	A
T_A	Operating free-air temperature range		–40 to 85	°C
T_J	Maximum junction temperature		125	°C
T_{STG}	Storage temperature range		–65 to 150	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM)	4000	V
		Charged Device Model (CDM)	1000	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC[1]		TPS22920 CS130P (8 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	130	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	54	
θ_{JB}	Junction-to-board thermal resistance	51	
ψ_{JT}	Junction-to-top characterization parameter	1	
ψ_{JB}	Junction-to-board characterization parameter	50	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{IN}	Input voltage range		0.75	3.6	V
V_{OUT}	Output voltage range			V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{IN} = 2.5-V to 3.6 V	1.2	3.6	V
		V_{IN} = 0.75-V to 2.49 V	0.9	3.6	V
V_{IL}	Low-level input voltage, ON	V_{IN} = 2.5-V to 3.6 V		0.6	V
		V_{IN} = 0.75-V to 2.49 V		0.4	V
C_{IN}	Input Capacitor		1[1]		µF

(1) See *Input Capacitor* section in Application Information.

ELECTRICAL CHARACTERISTICS

V_{IN} = 0.75 V to 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP[1]	MAX	UNIT
I_{IN}	Quiescent Current	I_{OUT} = 0, V_{IN} = V_{ON}	V_{IN} = 3.6 V	Full		68	160	µA
			V_{IN} = 2.5 V			40	70	
			V_{IN} = 1.8 V			25	350	µA
			V_{IN} = 1.2 V			103	200	
			V_{IN} = 1.05 V			78	110	µA
			V_{IN} = 0.75 V			37	70	
$I_{IN(leak)}$	Off Supply Current (After Pull Down)	V_{ON} = GND, V_{OUT} = 0		Full			5.5	µA
r_{ON}	On-Resistance	V_{IN} = 3.6 V, I_{OUT} = –200 mA		25°C		5.3	8.8	mΩ
				Full			9.8	
		V_{IN} = 2.5 V, I_{OUT} = –200 mA		25°C		5.4	8.9	mΩ
				Full			9.9	
		V_{IN} = 1.8 V, I_{OUT} = –200 mA		25°C		5.5	9.1	mΩ
				Full			10.1	
		V_{IN} = 1.2 V, I_{OUT} = –200 mA		25°C		5.8	9.4	mΩ
				Full			10.4	
		V_{IN} = 1.05 V, I_{OUT} = –200 mA		25°C		6.1	9.7	mΩ
				Full			10.8	
		V_{IN} = 0.75 V, I_{OUT} = –200 mA		25°C		7.3	11.0	mΩ
				Full			12.4	
RPD	Output pull down resistance[2]	V_{IN} = 3.3 V, V_{ON} = 0, I_{OUT} = 3 mA		Full		1250	1500	Ω
I_{ON}	ON input leakage current	V_{ON} = 0.9 V to 3.6 V or GND		Full			0.1	µA

(1) Typical values are at V_{IN} = 3.3 V and T_A = 25°C.
(2) See Output Pulldown in *Application Information*.

SWITCHING CHARACTERISTICS

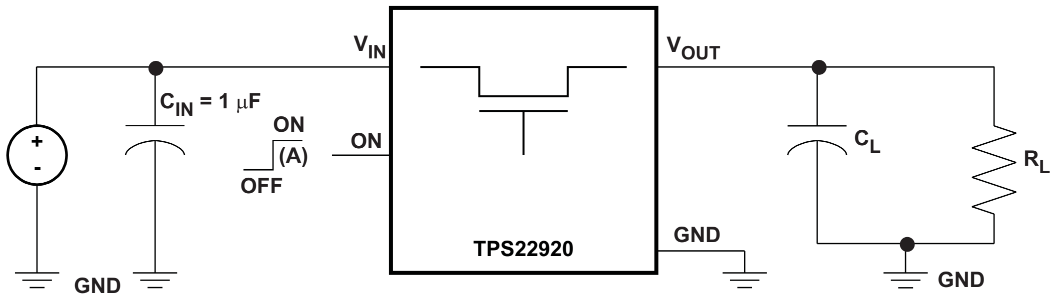
V_{IN} = 3.6 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 3.6 V		970		µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 3.6 V		3		
t_r	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 3.6 V		880		
t_f	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 3.6 V		2		

V_{IN} = 0.9 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 0.9 V		840		µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 0.9 V		16		
t_r	VOUT Rise time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 0.9 V		470		
t_f	VOUT Fall time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 0.9 V		5		

PARAMETRIC MEASUREMENT INFORMATION



TEST CIRCUIT

t_{ON}/t_{OFF} WAVEFORMS

(A) Rise and fall times of the control signal is 100 ns.

Figure 3. Test Circuit and t_{ON}/t_{OFF} Waveforms

TYPICAL CHARACTERISTICS

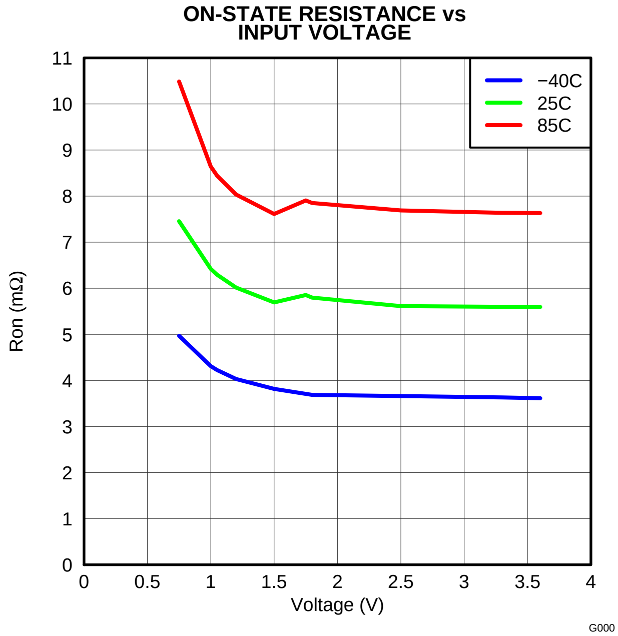


Figure 4.

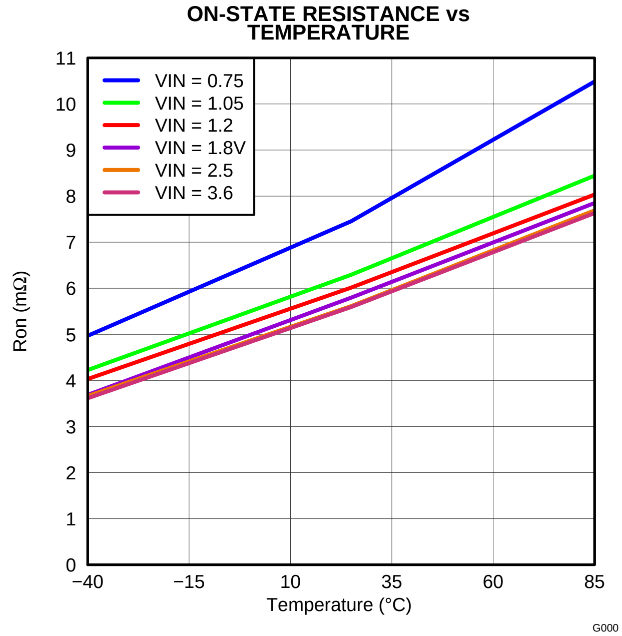


Figure 5.

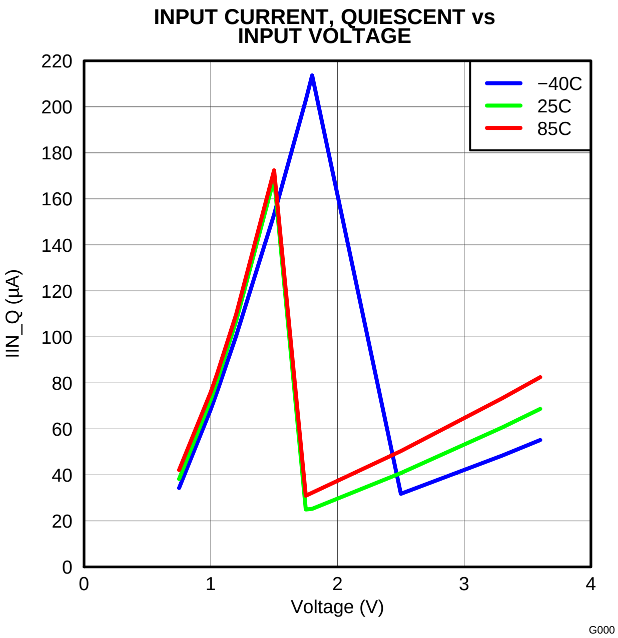


Figure 6.

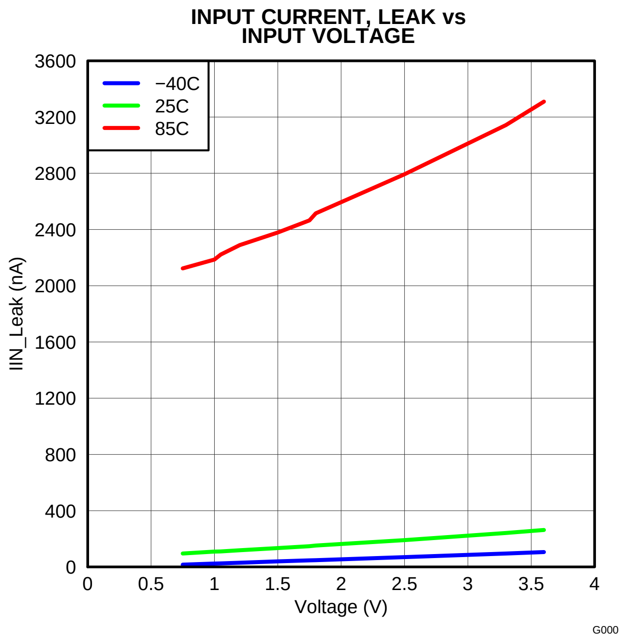


Figure 7.

TYPICAL CHARACTERISTICS (continued)

ON INPUT THRESHOLD

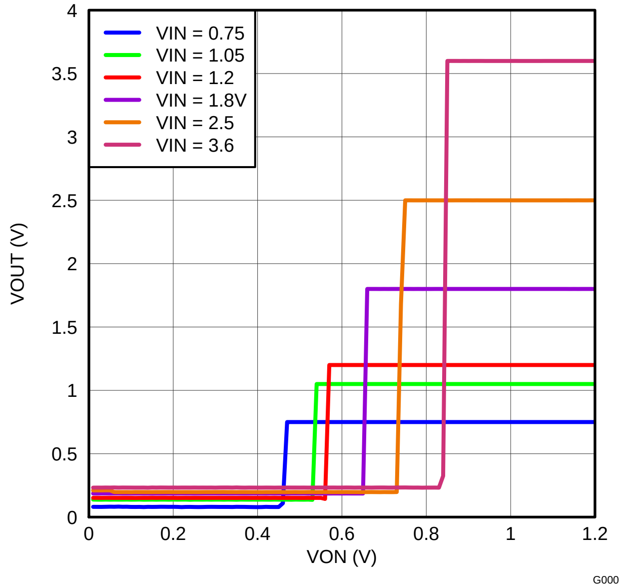


Figure 8.

TURN-ON TIME vs TEMPERATURE

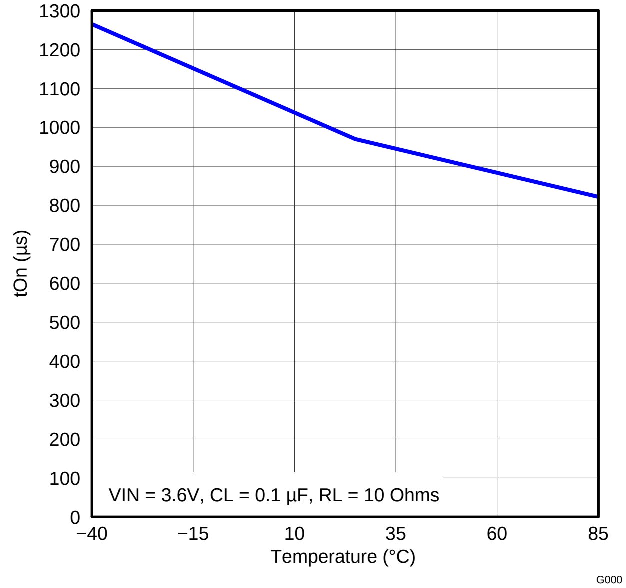


Figure 9.

TURN-OFF TIME vs TEMPERATURE

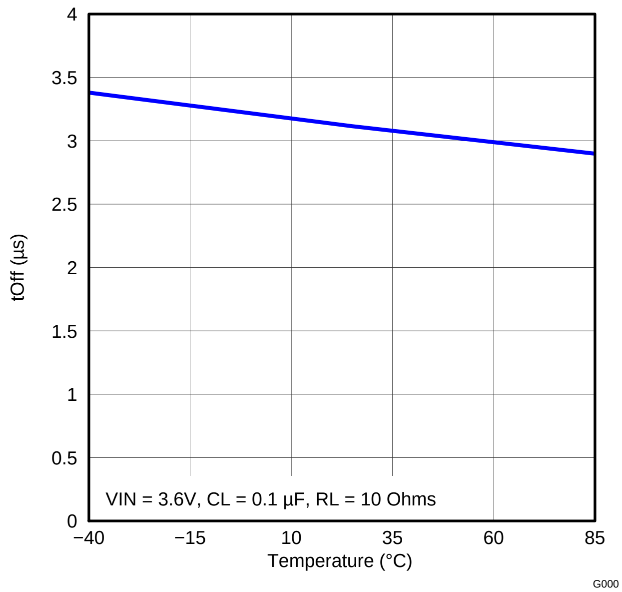


Figure 10.

RISE TIME vs TEMPERATURE

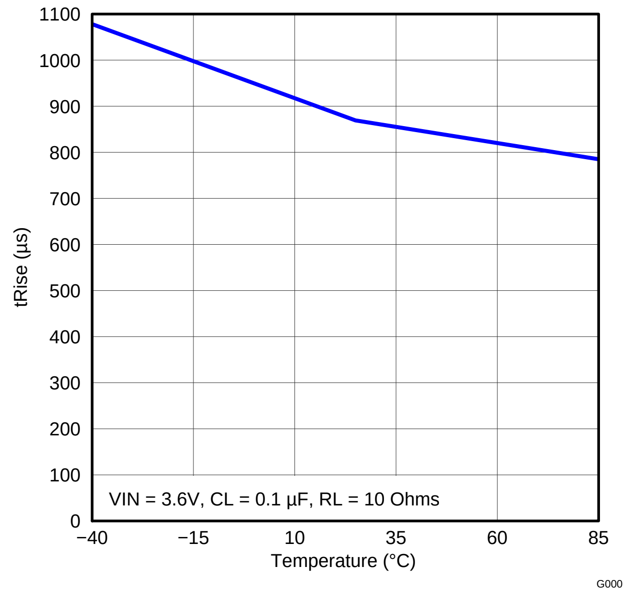


Figure 11.

TYPICAL CHARACTERISTICS (continued)

FALL TIME vs TEMPERATURE

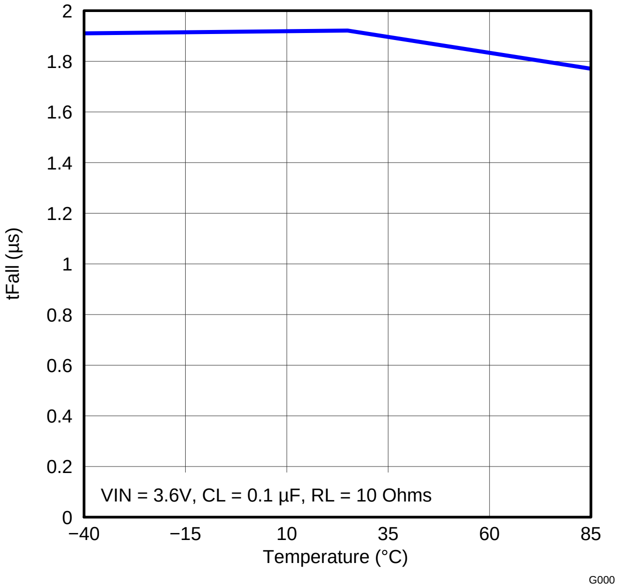


Figure 12.

TURN-ON TIME vs TEMPERATURE

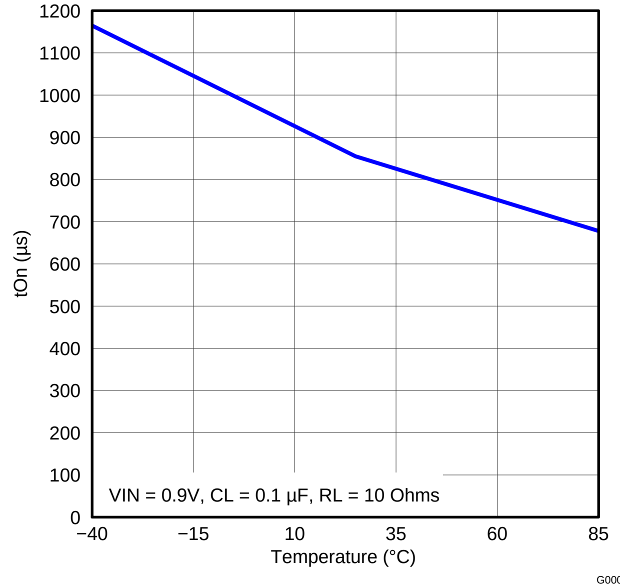


Figure 13.

TURN-OFF TIME vs TEMPERATURE

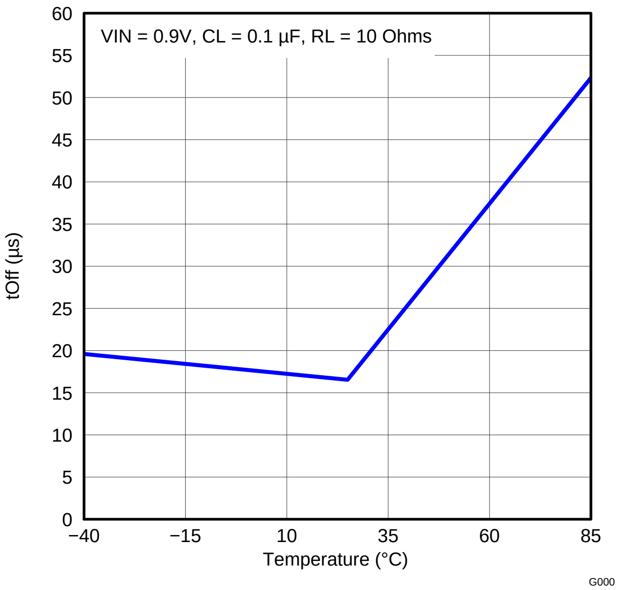


Figure 14.

RISE TIME vs TEMPERATURE

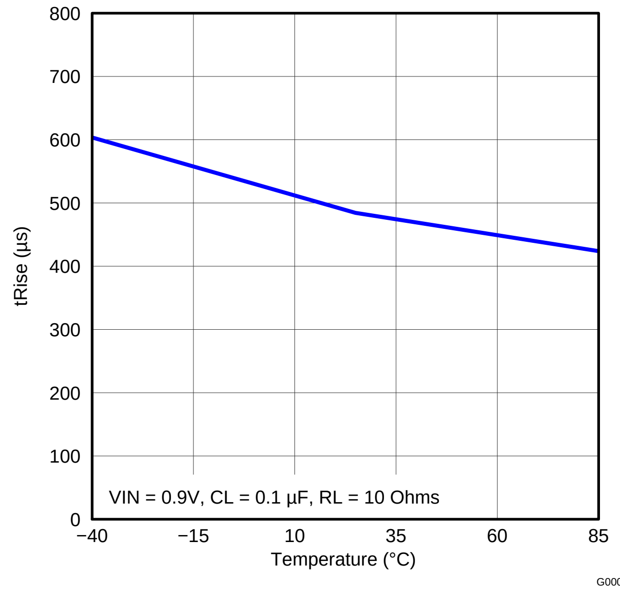


Figure 15.

TYPICAL CHARACTERISTICS (continued)

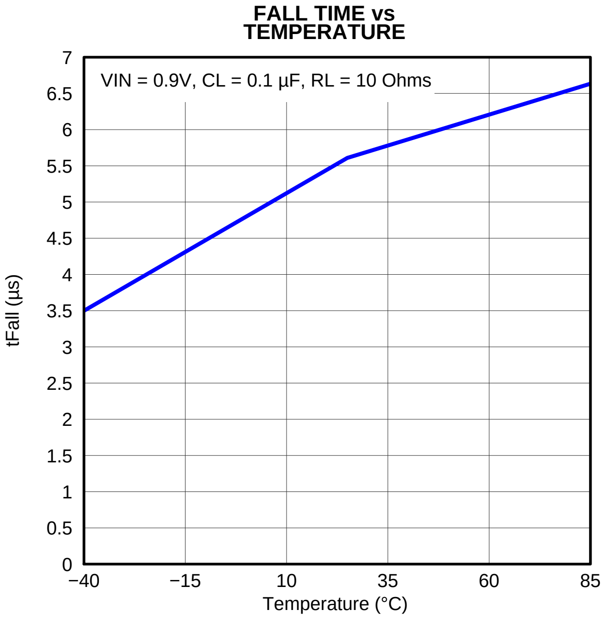


Figure 16.

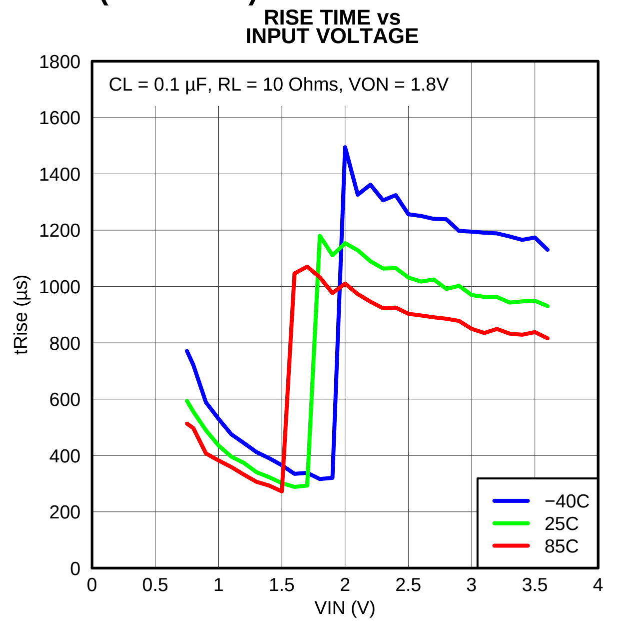


Figure 17.

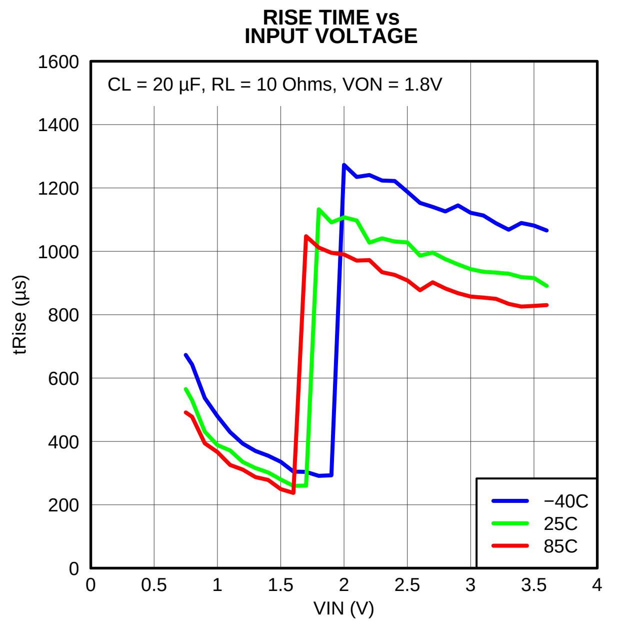


Figure 18.

TYPICAL CHARACTERISTICS (continued)

TURN-ON RESPONSE
V_{IN} = 0.9V, T_A = 25°C, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω

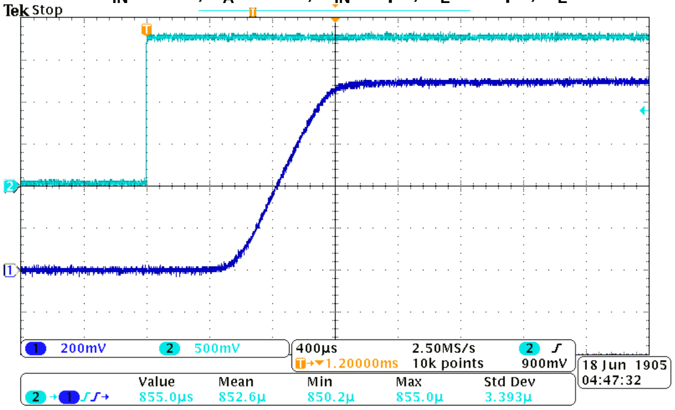


Figure 19.

TURN-OFF RESPONSE
V_{IN} = 0.9V, T_A = 25°C, C_{IN} = 1µF, C_L =0.1µF, R_L = 10Ω

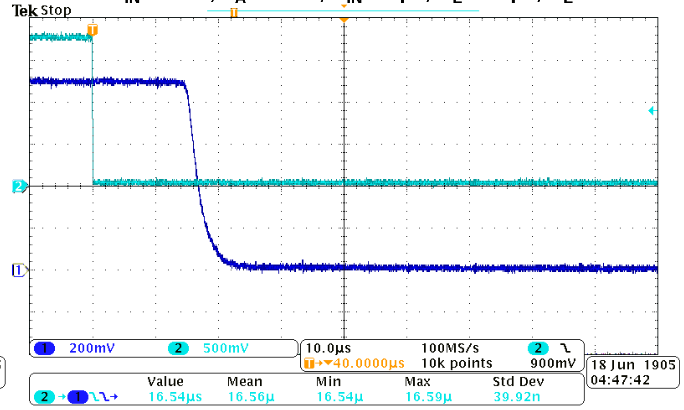


Figure 20.

TURN-ON RESPONSE
V_{IN} = 0.9V, T_A = 25°C, C_{IN} = 47µF, C_L = 20µF, R_L = 10Ω

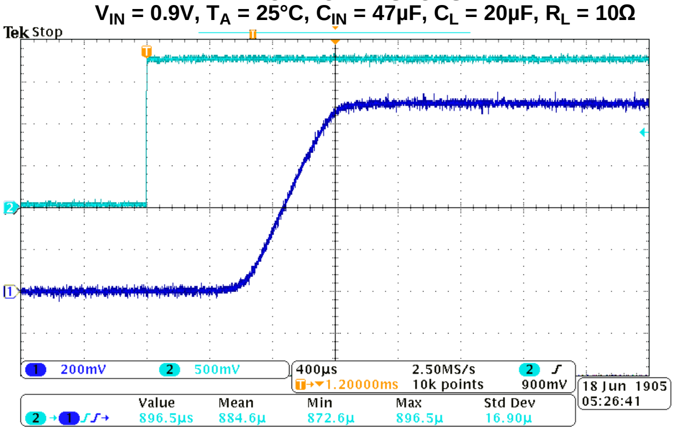


Figure 21.

TURN-OFF RESPONSE
V_{IN} = 0.9V, T_A = 25°C, C_{IN} = 47µF, C_L = 20µF, R_L = 10Ω

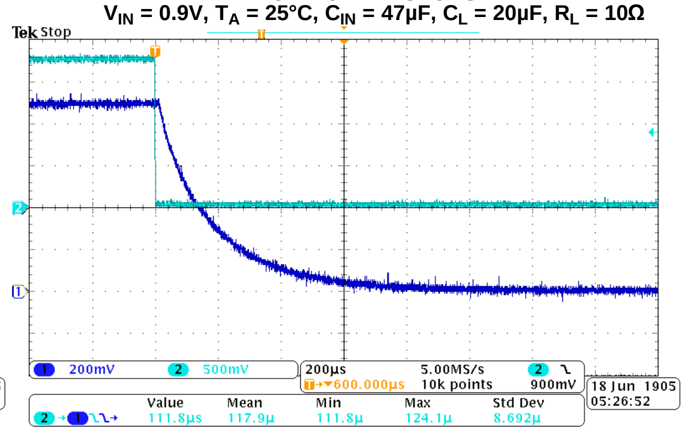


Figure 22.

TURN-ON RESPONSE
V_{IN} = 3.6V, T_A = 25°C, C_{IN} = 1µF, C_L =0.1µF, R_L = 10Ω

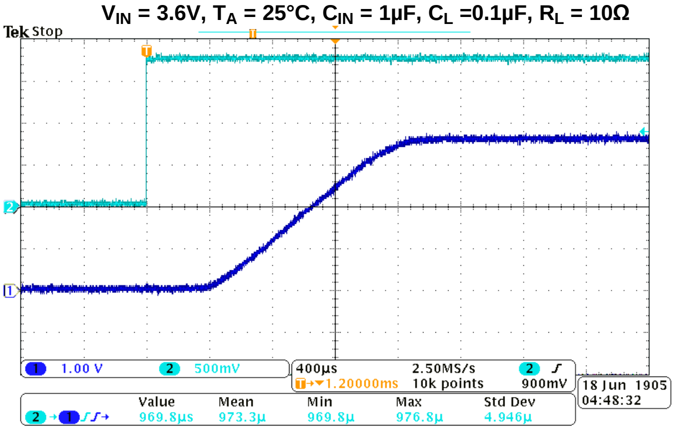


Figure 23.

TURN-OFF RESPONSE
V_{IN} = 3.6V, T_A = 25°C, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω

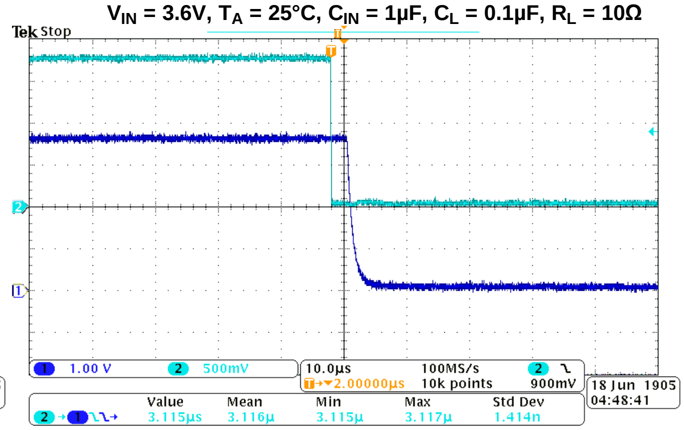


Figure 24.

TYPICAL CHARACTERISTICS (continued)

TURN-ON RESPONSE
V_{IN} = 3.6V, T_A = 25°C, C_{IN} = 47µF, C_L = 20µF, R_L = 10Ω

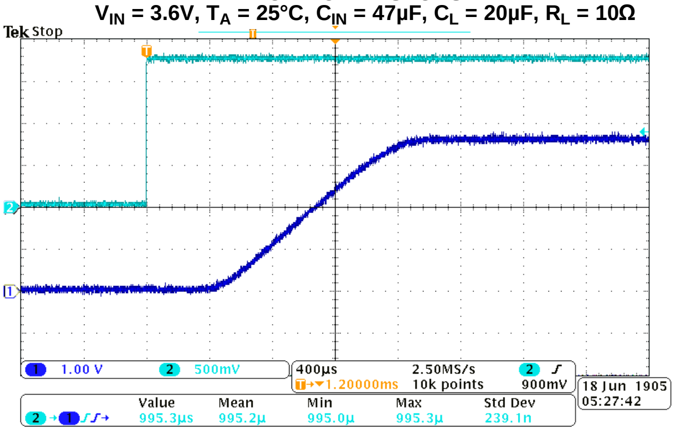


Figure 25.

TURN-OFF RESPONSE
V_{IN} = 3.6V, T_A = 25°C, C_{IN} = 47µF, C_L = 20µF, R_L = 10Ω

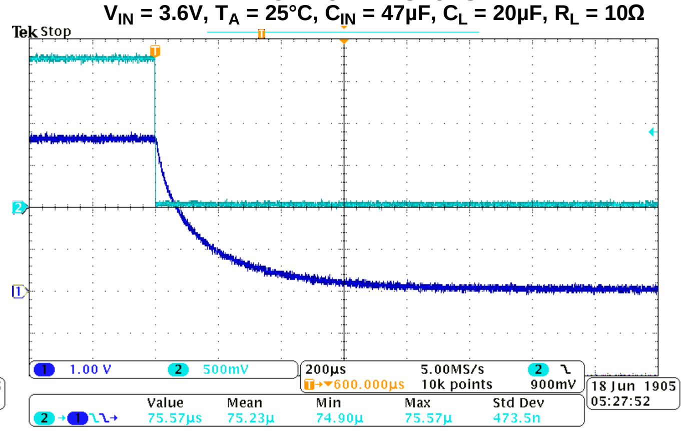


Figure 26.

APPLICATION INFORMATION

ON/OFF CONTROL

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIOs.

INPUT CAPACITOR

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{IN} and GND. A 1-μF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop.

OUTPUT CAPACITOR

Due to the integral body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed VIN when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup.

OUTPUT PULL-DOWN

The output pulldown is active when the user is turning off the main pass FET. The pulldown discharges the output rail to approximately 10% of the rail, and then the output pulldown is automatically disconnected to optimize the shutdown current.

BOARD LAYOUT

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN}, V_{OUT}, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

REVISION HISTORY

Changes from Original (June 2011) to Revision A	Page
• Updated swapped image issue.	8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22920YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	6Z	Samples
TPS22920YZPRB	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	6Z S	Samples
TPS22920YZPT	ACTIVE	DSBGA	YZP	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	6Z	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

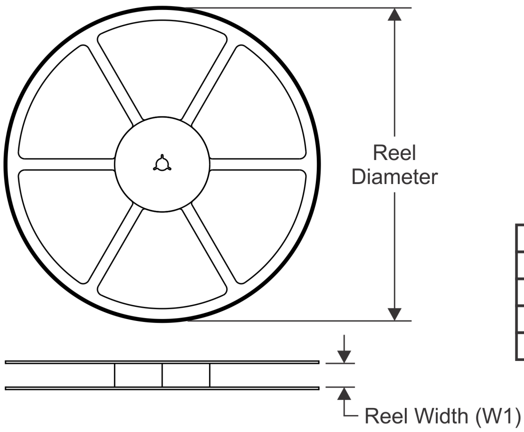
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

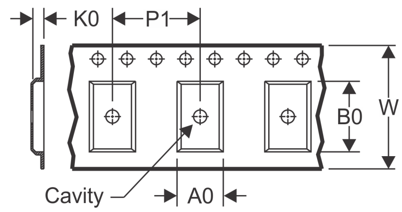
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

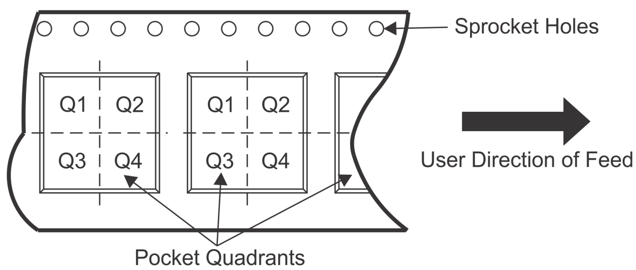


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

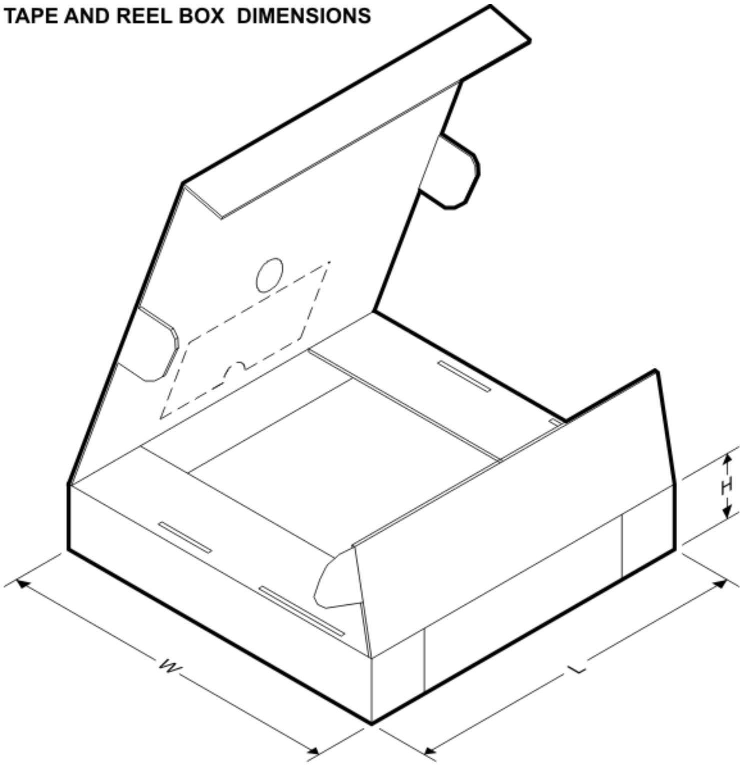
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22920YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1
TPS22920YZPRB	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1
TPS22920YZPT	DSBGA	YZP	8	250	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

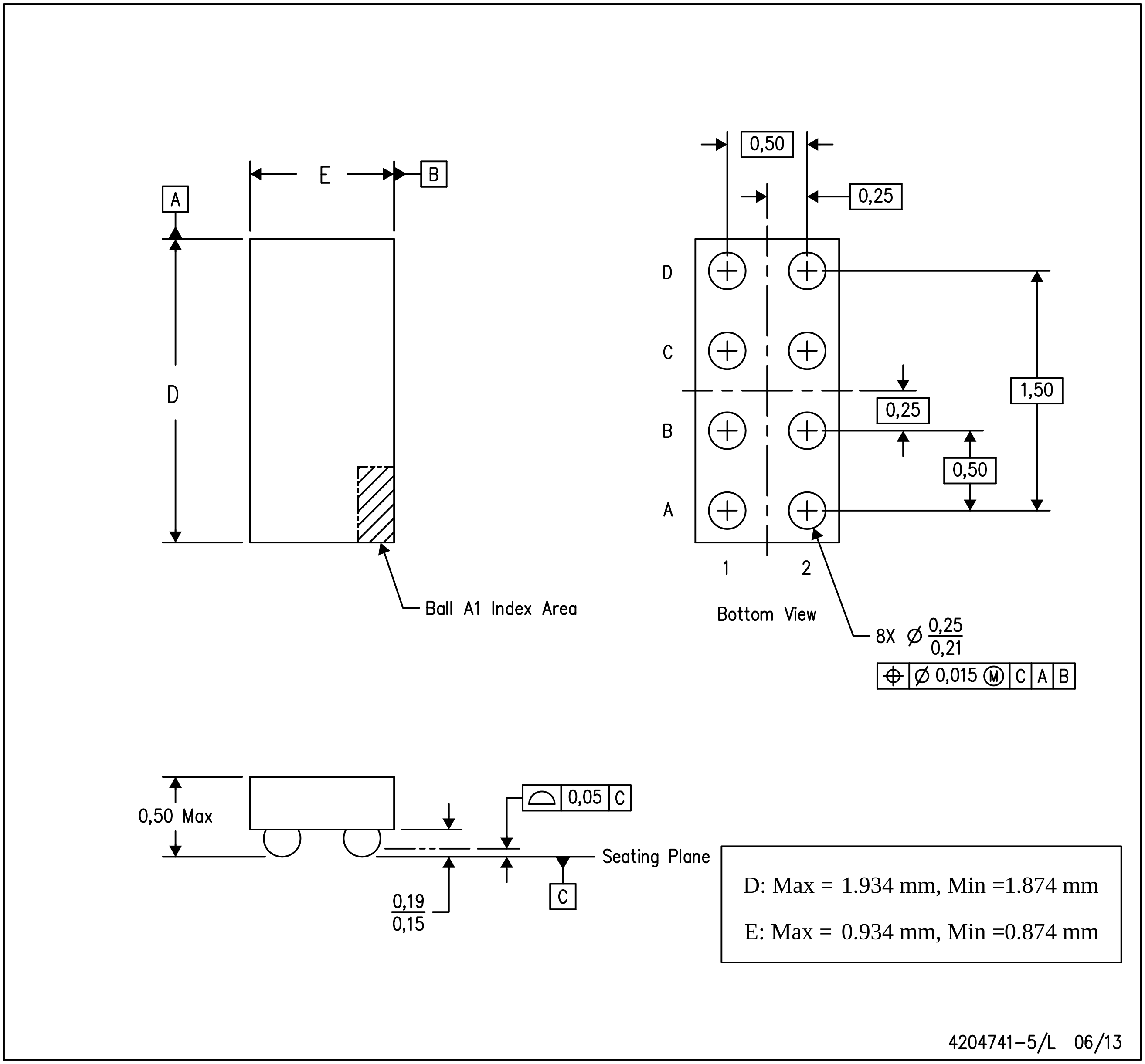
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22920YZPR	DSBGA	YZP	8	3000	182.0	182.0	17.0
TPS22920YZPRB	DSBGA	YZP	8	3000	182.0	182.0	17.0
TPS22920YZPT	DSBGA	YZP	8	250	182.0	182.0	17.0

YZP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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