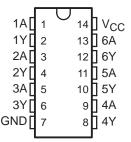
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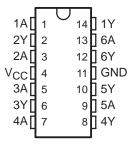
#### description/ordering information

These devices contain six independent inverters.

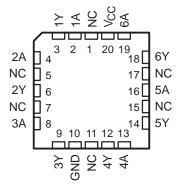
SN5404 ... J PACKAGE
SN54LS04, SN54S04 ... J OR W PACKAGE
SN7404, SN74S04 ... D, N, OR NS PACKAGE
SN74LS04 ... D, DB, N, OR NS PACKAGE
(TOP VIEW)



# SN5404 . . . W PACKAGE (TOP VIEW)



# SN54LS04, SN54S04 ... FK PACKAGE (TOP VIEW)



NC - No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



#### **ORDERING INFORMATION**

TA	PAC	KAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
		Tube	SN7404N	SN7404N
	PDIP – N	Tube	SN74LS04N	SN74LS04N
		Tube	SN74S04N	SN74S04N
		Tube	SN7404D	7404
		Tape and reel	SN7404DR	7404
	SOIC - D	Tube	SN74LS04D	1.004
0°C to 70°C	SOIC - D	Tape and reel	SN74LS04DR	LS04
		Tube	SN74S04D	004
		Tape and reel	SN74S04DR	S04
		Tape and reel	SN7404NSR	SN7404
	SOP - NS	Tape and reel	SN74LS04NSR	74LS04
		Tape and reel	SN74S04NSR	74S04
	SSOP – DB	Tape and reel	SN74LS04DBR	LS04
		Tube	SN5404J	SN5404J
		Tube	SNJ5404J	SNJ5404J
	CDIP – J	Tube	SN54LS04J	SN54LS04J
	CDIP – J	Tube	SN54S04J	SN54S04J
		Tube	SNJ54LS04J	SNJ54LS04J
-55°C to 125°C		Tube	SNJ54S04J	SNJ54S04J
		Tube	SNJ5404W	SNJ5404W
	CFP – W	Tube	SNJ54LS04W	SNJ54LS04W
		Tube	SNJ54S04W	SNJ54S04W
	LCCC – FK	Tube	SNJ54LS04FK	SNJ54LS04FK
	LCCC - FK	Tube	SNJ54S04FK	SNJ54S04FK

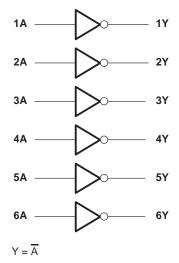
<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE** (each inverter)

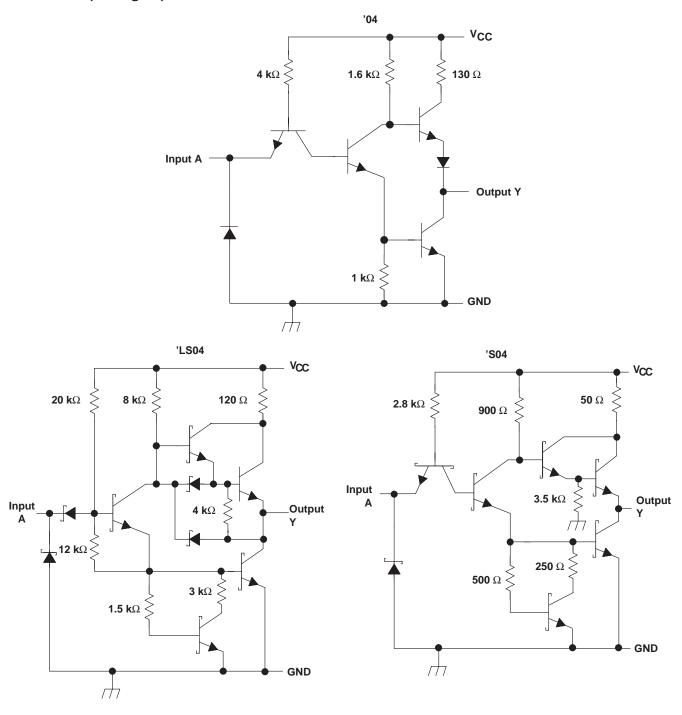
(	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
INPUT	OUTPUT
Α	Υ
Н	L
L	Н



## logic diagram (positive logic)



#### schematics (each gate)



Resistor values shown are nominal.



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V <sub>CC</sub> (see Note 1)		
Input voltage, V <sub>I</sub> : '04, 'S04		5.5 V
'LS04		
Package thermal impedance, θ <sub>JA</sub> (see Note	2): D package	86°C/W
, , , , , , , , , , , , , , , , , , ,	DB package	96°C/W
	N package	80°C/W
	NS package	
Storage temperature range, T <sub>stg</sub>		–65°C to 150°C

#### recommended operating conditions (see Note 3)

			SN5404		;	SN7404		UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
VCC	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
ІОН	High-level output current			-0.4			-0.4	mA
loL	Low-level output current			16			16	mA
TA	Operating free-air temperature	-55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		TEOT 001101TH	augt		SN5404				UNIT	
PARAMETER	TEST CONDITIONS‡			MIN	TYP§	MAX	MIN	TYP§	MAX	UNII
VIK	V <sub>CC</sub> = MIN,	I <sub>I</sub> = –12 mA				-1.5			-1.5	V
Voн	$V_{CC} = MIN,$	$V_{IL} = 0.8 V$ ,	$I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V
VOL	$V_{CC} = MIN,$	V <sub>IH</sub> = 2 V,	$I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
lį	$V_{CC} = MAX$ ,	V <sub>I</sub> = 5.5 V				1			1	mA
I <sub>IH</sub>	$V_{CC} = MAX$ ,	$V_{ } = 2.4 \text{ V}$				40			40	μΑ
I <sub>IL</sub>	$V_{CC} = MAX$ ,	$V_{ } = 0.4 V$				-1.6			-1.6	mA
IOS¶	$V_{CC} = MAX$			-20		-55	-18		-55	mA
ICCH	$V_{CC} = MAX$ ,	V <sub>I</sub> = 0 V			6	12		6	12	mA
ICCL	$V_{CC} = MAX$ ,	V <sub>I</sub> = 4.5 V	_		18	33		18	33	mA

<sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

<sup>§</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

 $<sup>\</sup>P$  Not more than one output should be shorted at a time.

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## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$ (see Figure 1)

PARAMETER FROM TO TEST CONDITIONS			SN5404 SN7404		UNIT			
	(INFOT)	(001701)			MIN	TYP	MAX	
<sup>t</sup> PLH	۸	V	P 400 O	C 15 pE		12	22	20
<sup>t</sup> PHL	A	ſ	$R_L = 400 \Omega$ ,	C <sub>L</sub> = 15 pF		8	15	ns

#### recommended operating conditions (see Note 3)

		S	N54LS04	4	S	N74LS04	4	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
VCC	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{\text{IH}}$	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.7			0.8	V
ІОН	High-level output current			-0.4			-0.4	mA
lOL	Low-level output current			4			8	mA
TA	Operating free-air temperature	-55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	TTOT COMPLETENCE		S	SN54LS04			SN74LS04			
PARAMETER	TEST CONDITIONS†			MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	UNIT
VIK	$V_{CC} = MIN,$	$I_{I} = -18 \text{ mA}$				-1.5			-1.5	V
VOH	$V_{CC} = MIN,$	$V_{IL} = MAX$ ,	$I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
Va	V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V	$I_{OL} = 4 \text{ mA}$		0.25	0.4			0.4	V
VoL	ACC = MINA	VIH = 2 V	I <sub>OL</sub> = 8 mA					0.25	0.5	V
lį	$V_{CC} = MAX$ ,	V <sub>I</sub> = 7 V				0.1			0.1	mA
lіН	$V_{CC} = MAX$ ,	V <sub>I</sub> = 2.7 V				20			20	μΑ
Ι <sub>ΙL</sub>	$V_{CC} = MAX$ ,	V <sub>I</sub> = 0.4 V				-0.4			-0.4	mA
I <sub>OS</sub> §	VCC = MAX			-20		-100	-20		-100	mA
ICCH	$V_{CC} = MAX$ ,	V <sub>I</sub> = 0 V			1.2	2.4		1.2	2.4	mA
ICCL	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 4.5 V			3.6	6.6		3.6	6.6	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see Figure 2)

PARAMETER	FROM (INPUT)	TEST CONDITIONS		TEST CONDITIONS			SN54LS04 SN74LS04			
	(IIVI O1)	(0011 01)		MIN	TYP	MAX				
t <sub>PLH</sub>	^	V	D. 210	C: 45 pF		9	15			
<sup>t</sup> PHL	А	Ť	$R_L = 2 k\Omega$ ,	C <sub>L</sub> = 15 pF		10	15	ns		



<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

#### recommended operating conditions (see Note 3)

		8	N54S04		9	N74S04		LINUT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			8.0			8.0	V
lOH	High-level output current			-1			-1	mA
lOL	Low-level output current			20			20	mA
TA	Operating free-air temperature	-55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEGT COMPLETIONS!			SN54S04		5		LINUT		
PARAMETER	TEST CONDITIONS <sup>†</sup>			MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIK	$V_{CC} = MIN,$	$I_{I} = -18 \text{ mA}$				-1.2			-1.2	V
Voн	$V_{CC} = MIN,$	$V_{IL} = 0.8 V$ ,	$I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
VOL	$V_{CC} = MIN,$	V <sub>IH</sub> = 2 V,	$I_{OL} = 20 \text{ mA}$			0.5			0.5	V
lį	$V_{CC} = MAX$ ,	$V_{I} = 5.5 V$				1			1	mA
lіН	$V_{CC} = MAX$ ,	V <sub>I</sub> = 2.7 V				50			50	μΑ
Ι <sub>Ι</sub> L	$V_{CC} = MAX$ ,	V <sub>I</sub> = 0.5 V				-2			-2	mA
I <sub>OS</sub> §	$V_{CC} = MAX$			-40		-100	-40		-100	mA
Іссн	$V_{CC} = MAX$ ,	V <sub>I</sub> = 0 V			15	24		15	24	mA
ICCL	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 4.5 V			30	54		30	54	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

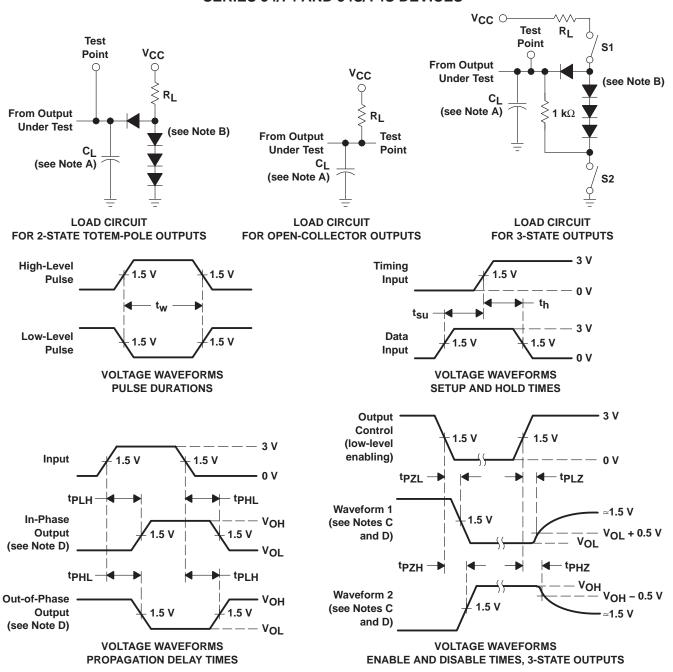
## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS			N54S04 N74S04		UNIT
	(INFOT)	(001-01)			MIN	TYP	MAX	
t <sub>PLH</sub>	^	V	B 200 O	C <sub>I</sub> = 15 pF		3	4.5	no
tPHL	A	T	$R_L = 280 \Omega$	CL = 15 pr		3	5	ns
t <sub>PLH</sub>	^	V	B 200 O	C <sub>I</sub> = 50 pF		4.5		no
<sup>t</sup> PHL	А	T	$R_L = 280 \Omega$ ,	CL = 50 pr		5		ns

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

#### PARAMETER MEASUREMENT INFORMATION SERIES 54/74 AND 54S/74S DEVICES



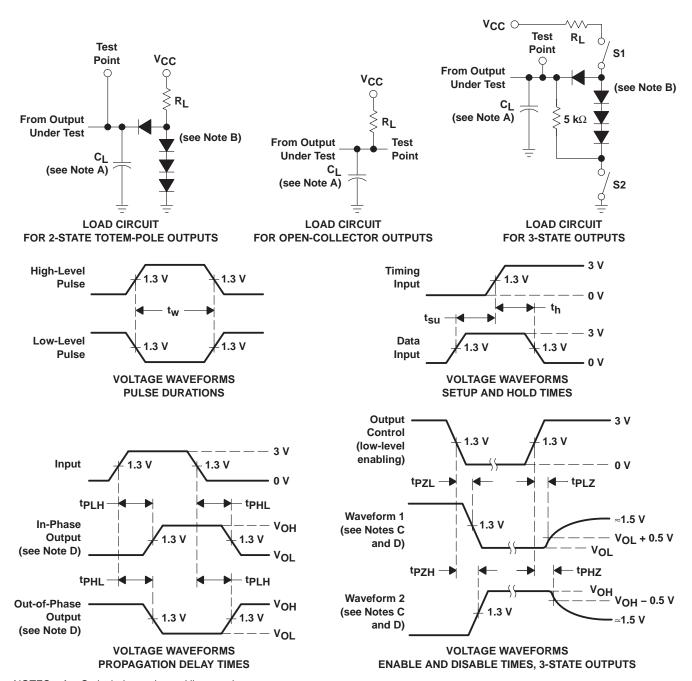
NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. All diodes are 1N3064 or equivalent.
- C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- D. S1 and S2 are closed for tpLH, tpHZ, and tpLZ; S1 is open and S2 is closed for tpZH; S1 is closed and S2 is open for tpZL.
- E. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O \approx 50 \Omega$ ;  $t_r$  and  $t_f \leq$  7 ns for Series 54/74 devices and  $t_r$  and  $t_f \le 2.5$  ns for Series 54S/74S devices.
- F. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



# PARAMETER MEASUREMENT INFORMATION SERIES 54LS/74LS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.
  - B. All diodes are 1N3064 or equivalent.
  - C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - D. S1 and S2 are closed for tpLH, tpHL, tpHZ, and tpLZ; S1 is open and S2 is closed for tpZH; S1 is closed and S2 is open for tpZL.
  - E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
  - F. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O \approx 50 \ \Omega$ ,  $t_f \leq$  1.5 ns,  $t_f \leq$  2.6 ns.
  - G. The outputs are measured one at a time, with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms







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#### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
JM38510/00105BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00105BCA	Samples
JM38510/00105BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00105BDA	Samples
JM38510/07003BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07003BCA	Samples
JM38510/07003BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07003BDA	Samples
JM38510/30003B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30003B2A	Samples
JM38510/30003BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30003BCA	Samples
JM38510/30003BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30003BDA	Samples
JM38510/30003SCA	ACTIVE	CDIP	J	14	25	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30003SCA	Samples
M38510/00105BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00105BCA	Samples
M38510/00105BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00105BDA	Samples
M38510/07003BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07003BCA	Samples
M38510/07003BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07003BDA	Samples
M38510/30003B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30003B2A	Samples
M38510/30003BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30003BCA	Samples
M38510/30003BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30003BDA	Samples
M38510/30003SCA	ACTIVE	CDIP	J	14	25	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30003SCA	Samples
SN5404J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN5404J	Samples





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Orderable Device	Status	Package Type		Pins		Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	<b>Device Marking</b>	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
SN54LS04J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS04J	Samples
SN54S04J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S04J	Samples
SN7404D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7404	Samples
SN7404DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7404	Samples
SN7404DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7404	Samples
SN7404DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7404	Samples
SN7404N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN7404N	Samples
SN7404NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN7404N	Samples
SN74LS04D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS04	Samples
SN74LS04DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		LS04	Samples
SN74LS04DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS04	Samples
SN74LS04DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS04	Samples
SN74LS04DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS04	Samples
SN74LS04DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS04	Samples
SN74LS04N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type 0 to 70		SN74LS04N	Samples
SN74LS04NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS04N	Samples
SN74LS04NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS04	Samples
SN74LS04NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS04	Samples





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Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	<b>Device Marking</b>	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
SN74S04D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S04	Samples
SN74S04DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S04	Samples
SN74S04DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S04	Samples
SN74S04N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S04N	Samples
SN74S04NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S04N	Samples
SN74S04NSR	ACTIVE	so	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74S04	Samples
SNJ5404J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5404J	Samples
SNJ5404W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5404W	Samples
SNJ54LS04FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 04FK	Samples
SNJ54LS04J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS04J	Samples
SNJ54LS04W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS04W	Samples
SNJ54S04FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 04FK	Samples
SNJ54S04J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S04J	Samples
SNJ54S04W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S04W	Samples

<sup>(1)</sup> The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

#### PACKAGE OPTION ADDENDUM



.com 17-Mar-2017

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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#### OTHER QUALIFIED VERSIONS OF SN5404, SN54LS04, SN54LS04-SP, SN54S04, SN7404, SN74LS04, SN74S04:

Catalog: SN7404, SN74LS04, SN54LS04, SN74S04

Military: SN5404, SN54LS04, SN54S04

Space: SN54LS04-SP

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications



### **PACKAGE OPTION ADDENDUM**

17-Mar-2017

• Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## **PACKAGE MATERIALS INFORMATION**

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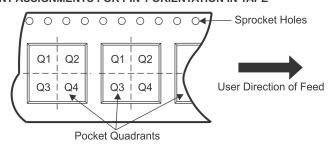
#### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

All diffiensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN7404DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS04DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LS04DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74S04DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74S04NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

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\*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN7404DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74LS04DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74LS04DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74S04DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74S04NSR	SO	NS	14	2000	367.0	367.0	38.0

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



#### **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

## 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## W (R-GDFP-F14)

## CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14



## D (R-PDSO-G14)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



# D (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



#### DB (R-PDSO-G\*\*)

#### PLASTIC SMALL-OUTLINE

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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