



PCA9517 Level-Translating I²C Bus Repeater

Not Recommended for New Designs

1 Features

- Two-Channel Bidirectional Buffer
- I²C Bus and SMBus Compatible
- Operating Supply Voltage Range of 0.9 V to 5.5 V on A Side
- Operating Supply Voltage Range of 2.7 V to 5.5 V on B Side
- Voltage-Level Translation From 0.9 V to 5.5 V and 2.7 V to 5.5 V
- Footprint and Function Replacement for PCA9515A
- Active-High Repeater-Enable Input
- Open-Drain I²C I/O
- 5.5-V Tolerant I²C and Enable Input Support Mixed-Mode Signal Operation
- Lockup-Free Operation
- Accommodates Standard Mode and Fast Mode I²C Devices and Multiple Masters
- Powered-Off High-Impedance I²C Pins
- 400-kHz Fast I²C Bus
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Description

This dual bidirectional I²C buffer is operational at 2.7 V to 5.5 V.

The PCA9517 is a BiCMOS integrated circuit intended for I²C bus and SMBus systems. It can also provide bidirectional voltage-level translation (up-translation/down-translation) between low voltages (down to 0.9 V) and higher voltages (2.7 V to 5.5 V) in mixed-mode applications. This device enables I²C and similar bus systems to be extended, without degradation of performance even during level shifting.

The PCA9517 buffers both the serial data (SDA) and the serial clock (SCL) signals on the I²C bus, thus allowing two buses of 400-pF bus capacitance to be connected in an I²C application. This device can also be used to isolate two halves of a bus for voltage and capacitance.

The PCA9517 has two types of drivers—A-side drivers and B-side drivers. All inputs and I/Os are overvoltage tolerant to 5.5 V, even when the device is unpowered (V_{CCB} and/or $V_{CCA} = 0$ V).

The PCA9517 does not support clock stretching and arbitration across the repeater.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCA9517	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

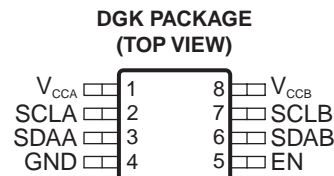
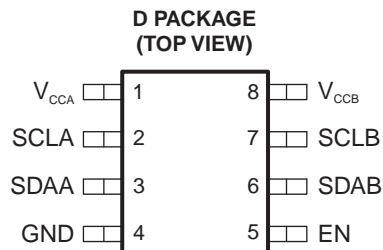


Table of Contents

1 Features	1	7 Parameter Measurement Information	8
2 Description	1	8 Detailed Description	9
3 Revision History	2	8.1 Functional Block Diagram	9
4 Description (Continued)	3	8.2 Feature Description.....	10
5 Pin Configuration and Functions	4	8.3 Device Functional Modes.....	12
6 Specifications	4	9 Application and Implementation	12
6.1 Absolute Maximum Ratings	4	9.1 Typical Application	12
6.2 Handling Ratings.....	4	10 Device and Documentation Support	15
6.3 Recommended Operating Conditions.....	5	10.1 Trademarks	15
6.4 Thermal Information	5	10.2 Electrostatic Discharge Caution.....	15
6.5 Electrical Characteristics.....	6	10.3 Glossary	15
6.6 Timing Requirements.....	6	11 Mechanical, Packaging, and Orderable	
6.7 I ² C Interface Timing Requirements.....	7	Information	15

3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2012) to Revision E	Page
• Added Clock Stretching Errata section.	10
• Added Load Dependent Undershoot Errata section.....	10
• Added Glitch/Noise Susceptibility Errata section.....	11
• Added Load Susceptibility Errata section.....	11

Changes from Revision B (May 2010) to Revision C	Page
• Deleted all references to arbitration and clock stretching support. This does not effect min/max specifications.	1

4 Description (Continued)

The B-side drivers operate from 2.7 V to 5.5 V and behave like the drivers in the PCA9515A. The output low level for this internal buffer is approximately 0.5 V, but the input voltage must be 70 mV or more below the output low level when the output internally is driven low. The higher-voltage low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released.

This type of design on the B side prevents it from being used in series with the PCA9515A and another PCA9517 (B side). This is because these devices do not recognize buffered low signals as a valid low and do not propagate it as a buffered low again.

The A-side drivers operate from 0.9 V to 5.5 V and drive more current. They do not require the buffered low feature (or the static offset voltage). This means that a low signal on the B side translates to a nearly 0-V low on the A side, which accommodates smaller voltage swings of lower-voltage logic. The output pulldown on the A side drives a hard low, and the input level is set at $0.3 V_{CCA}$ to accommodate the need for a lower low level in systems where the low-voltage-side supply voltage is as low as 0.9 V.

The A side of two or more PCA9517s can be connected together to allow a star topography, with the A side on the common bus. Also, the A side can be connected directly to any other buffer with static- or dynamic-offset voltage. Multiple PCA9517s can be connected in series, A side to B side, with no buildup in offset voltage and with only time-of-flight delays to consider.

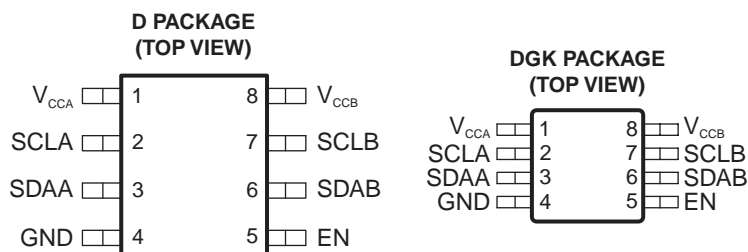
The PCA9517 drivers are enabled when V_{CCA} is above 0.8 V and V_{CCB} is above 2.5 V.

The PCA9517 has an active-high enable (EN) input with an internal pullup to V_{CCB} , which allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up reset. It should never change state during an I²C operation, because disabling during a bus operation hangs the bus, and enabling part way through a bus cycle could confuse the I²C parts being enabled. The EN input should change state only when the global bus and repeater port are in an idle state, to prevent system failures.

The PCA9517 includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2.5 V and the V_{CCA} is above 0.8 V. V_{CCB} and V_{CCA} can be applied in any sequence at power up. After power up and with the EN high, a low level on the A side (below $0.3 V_{CCA}$) turns the corresponding B-side driver (either SDA or SCL) on and drives the B side down to approximately 0.5 V. When the A side rises above $0.3 V_{CCA}$, the B-side pulldown driver is turned off and the external pullup resistor pulls the pin high. When the B side falls first and goes below $0.3 V_{CCB}$, the A-side driver is turned on and the A side pulls down to 0 V. The B-side pulldown is not enabled unless the B-side voltage goes below 0.4 V. If the B-side low voltage does not go below 0.5 V, the A-side driver turns off when the B-side voltage is above $0.7 V_{CCB}$. If the B-side low voltage goes below 0.4 V, the B-side pulldown driver is enabled, and the B side is able to rise to only 0.5 V until the A side rises above $0.3 V_{CCA}$. Then the B side continues to rise, being pulled up by the external pullup resistor. V_{CCA} is only used to provide the $0.3 V_{CCA}$ reference to the A-side input comparators and for the power-good-detect circuit. The PCA9517 logic and all I/Os are powered by the V_{CCB} pin.

As with the standard I²C system, pullup resistors are required to provide the logic-high levels on the buffered bus. The PCA9517 has standard open-collector configuration of the I²C bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with Standard mode and Fast mode I²C devices in addition to SMBus devices. Standard mode I²C devices only specify 3 mA in a generic I²C system, where Standard mode devices and multiple masters are possible. Under certain conditions, higher termination currents can be used.

5 Pin Configuration and Functions



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
V_{CCA}	1	A-side supply voltage (0.9 V to 5.5 V)
SCLA	2	Serial clock bus, A side. Connect to V_{CCA} through a pullup resistor.
SDAA	3	Serial data bus, A side. Connect to V_{CCA} through a pullup resistor.
GND	4	Supply ground
EN	5	Active-high repeater enable input
SDAB	6	Serial data bus, B side. Connect to V_{CCB} through a pullup resistor.
SCLB	7	Serial clock bus, B side. Connect to V_{CCB} through a pullup resistor.
V_{CCB}	8	B-side and device supply voltage (2.7 V to 5.5 V)

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CCB}	Supply voltage range	-0.5	7	V
V_{CCA}	Supply voltage range	-0.5	7	V
V_I	Enable input voltage range ⁽²⁾	-0.5	7	V
$V_{I/O}$	I ² C bus voltage range ⁽²⁾	-0.5	7	V
I_{IK}	Input clamp current		-50	mA
I_{OK}	Output clamp current		-50	
I_O	Continuous output current		±50	mA
	Continuous current through V_{CC} or GND		±100	

- Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 Handling Ratings

		MIN	MAX	UNIT	
T_{stg}	Storage temperature range	-65	150	°C	
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	1000	

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CCA}	Supply voltage, A-side bus	0.9 ⁽¹⁾	5.5	V
V _{CCB}	Supply voltage, B-side bus	2.7	5.5	V
V _{IH}	High-level input voltage	SDAA, SCLA	0.7 × V _{CCA}	5.5
		SDAB, SCLB	0.7 × V _{CCB}	5.5
		EN	0.7 × V _{CCB}	5.5
V _{IL}	Low-level input voltage	SDAA, SCLA	−0.5	0.28 × V _{CCA}
		SDAB, SCLB	−0.5 ⁽²⁾	0.3 × V _{CCB}
		EN	−0.5	0.3 × V _{CCB}
I _{OL}	Low-level output current	V _{CCB} = 2.7 V		6
		V _{CCB} = 3 V		6
T _A	Operating free-air temperature	−40	85	°C

(1) Low-level supply voltage

 (2) V_{IL} specification is for the first low level seen by the SDAB and SCLB lines. V_{ILc} is for the second and subsequent low levels seen by the SDAB and SCLB lines.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	PCA9517		UNIT	
	D	DGK		
	8 PINS	8 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	97	172	°C/W

 (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

PCA9517

SCPS157E –DECEMBER 2007–REVISED JUNE 2014

www.ti.com

6.5 Electrical Characteristics

V_{CCB} = 2.7 V to 5.5 V, GND = 0 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CCB}	MIN	TYP	MAX	UNIT
V _{IK}	Input clamp voltage	I _I = –18 mA	2.7 V to 5.5 V			–1.2	V
V _{OL}	Low-level output voltage	SDAB, SCLB I _{OL} = 100 μA or 6 mA, V _{ILA} = V _{ILB} = 0 V	2.7 V to 5.5 V	0.45	0.52	0.7	V
		SDAA, SCLA I _{OL} = 6 mA			0.1	0.2	
V _{OL} – V _{ILC}	Low-level input voltage below low-level output voltage	SDAB, SCLB	2.7 V to 5.5 V			70	mV
V _{ILC}	SDA and SCL low-level input voltage contention	SDAB, SCLB	2.7 V to 5.5 V	–0.5	0.4		V
I _{CC}	Quiescent supply current for V _{CCA}	Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open, or SDAA = SCLA = open and SDAB = SCLB = GND				1	mA
I _{CC}	Quiescent supply current	Both channels high, SDAA = SCLA = V _{CCA} and SDAB = SCLB = V _{CCB} and EN = V _{CCB}	5.5 V		1.5	4	mA
		Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open, or SDAA = SCLA = open and SDAB = SCLB = GND			1.5	5	
		In contention, SDAA = SCLA = GND and SDAB = SCLB = GND			1.5	5	
I _I	Input leakage current	SDAB, SCLB	2.7 V to 5.5 V	V _I = V _{CCB}		±1	μA
				V _I = 0.2 V		10	
		SDAA, SCLA		V _I = V _{CCB}		±1	
				V _I = 0.2 V		10	
		EN		V _I = V _{CCB}		±1	
				V _I = 0.2 V		–10 –30	
I _{OH}	High-level output leakage current	SDAB, SCLB	2.7 V to 5.5 V			10	μA
		SDAA, SCLA		V _O = 3.6 V			
C _I	Input capacitance	EN	V _I = 3 V or 0 V	3.3 V	6	7	pF
		SCLA, SCLB	V _I = 3 V or 0 V	3.3 V	6	9	
			0 V		6	8	
C _{IO}	Input/output capacitance	SDAA, SDAB	V _I = 3 V or 0 V	3.3 V	6	9	pF
			0 V		6	8	

6.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
t _{su} Setup time, EN high before Start condition ⁽¹⁾	100		ns
t _h Hold time, EN high after Stop condition ⁽¹⁾	100		ns

(1) EN should change state only when the global bus and the repeater port are in an idle state.

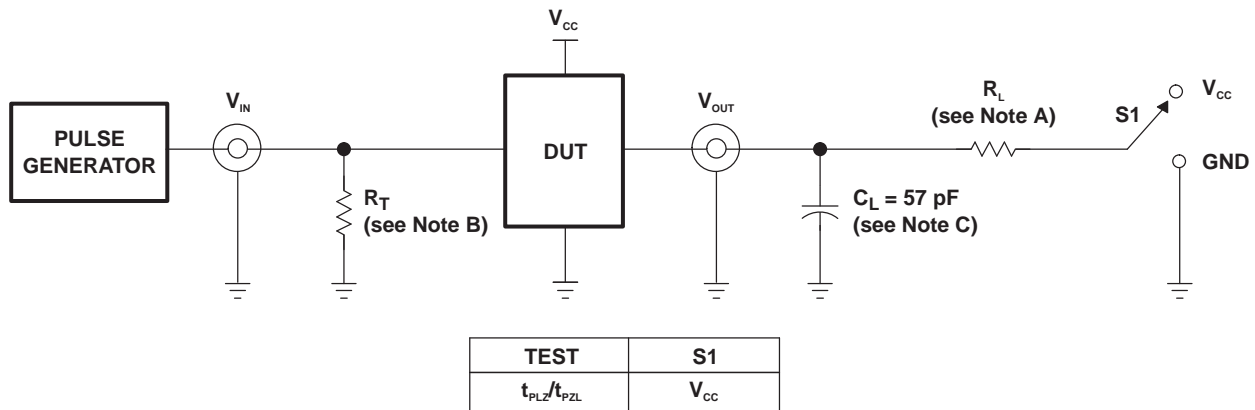
6.7 I²C Interface Timing Requirements

 $V_{CCB} = 2.7\text{ V to }5.5\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
t_{PLZ}	Propagation delay	SDAB, SCLB ⁽²⁾ (see Figure 4)	SDAA, SCLA ⁽²⁾ (see Figure 4)		100	169	255	ns	
		SDAA, SCLA ⁽³⁾ (see Figure 3)	SDAB, SCLB ⁽³⁾ (see Figure 3)		25	67	110		
t_{PZL}	Propagation delay	SDAB, SCLB	SDAA, SCLA	$V_{CCA} \leq 2.7\text{ V}$ (see Figure 2)	15	68 ⁽⁴⁾	110	ns	
				$2.7\text{ V} \leq V_{CCA} \leq 3\text{ V}$ (see Figure 2)	20	79	130		
				$V_{CCA} \geq 3\text{ V}$ (see Figure 2)	10	103 ⁽⁵⁾	300		
		SDAA, SCLA ⁽³⁾ (see Figure 3)	SDAB, SCLB ⁽³⁾ (see Figure 3)		45	118	230		
t_{TLH}	Transition time	B side to A side (see Figure 3)	20%	80%		1	6	30	ns
		A side to B side (see Figure 2)				20	31	170	
t_{THL}	Transition time	B side to A side	80%	20%	$V_{CCA} \leq 2.7\text{ V}$ (see Figure 3)	1	3 ⁽⁶⁾	105	ns
					$2.7\text{ V} \leq V_{CCA} \leq 3\text{ V}$ (see Figure 2)	1	6	120	
					$V_{CCA} \geq 3\text{ V}$ (see Figure 3)	1	25 ⁽⁷⁾	175	
		A side to B side (see Figure 2)		1	12	90			

- (1) Typical values were measured with $V_{CCA} = V_{CCB} = 2.7\text{ V}$ at $T_A = 25^\circ\text{C}$, unless otherwise noted.
- (2) The t_{PLH} delay data from B to A side is measured at 0.5 V on the B side to 0.5 V_{CCA} on the A side when V_{CCA} is less than 2 V, and 1.5 V on the A side if V_{CCA} is greater than 2 V.
- (3) The proportional delay data from A to B side is measured at 0.3 V_{CCA} on the A side to 1.5 V on the B side.
- (4) Typical value measured with $V_{CCA} = 0.9\text{ V}$ at $T_A = 25^\circ\text{C}$
- (5) Typical value measured with $V_{CCA} = 5.5\text{ V}$ at $T_A = 25^\circ\text{C}$
- (6) Typical value measured with $V_{CCA} = 0.9\text{ V}$ at $T_A = 25^\circ\text{C}$
- (7) Typical value measured with $V_{CCA} = 5.5\text{ V}$ at $T_A = 25^\circ\text{C}$

7 Parameter Measurement Information



TEST CIRCUIT FOR OPEN-DRAIN OUTPUT

- A. $R_L = 167 \Omega$ on the A side and $1.35 \text{ k}\Omega$ on the B side
- B. R_T termination resistance should be equal to Z_{OUT} of pulse generators.
- C. C_L includes probe and jig capacitance.
- D. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, slew rate $\geq 1 \text{ V/ns}$.
- E. The outputs are measured one at a time, with one transition per measurement.
- F. t_{PLH} and t_{PHL} are the same as t_{pd} .
- G. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- H. t_{PZL} and t_{PZH} are the same as t_{en} .

Figure 1. Test Circuit

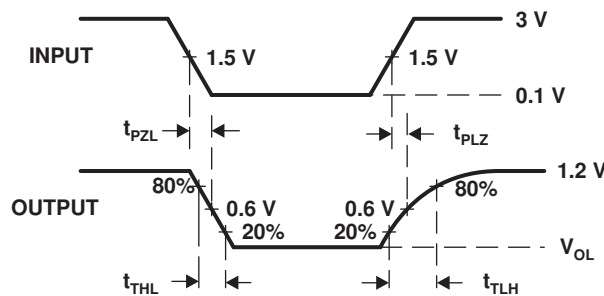


Figure 2. Waveform 1 – Propagation Delay and Transition Times for B Side to A Side

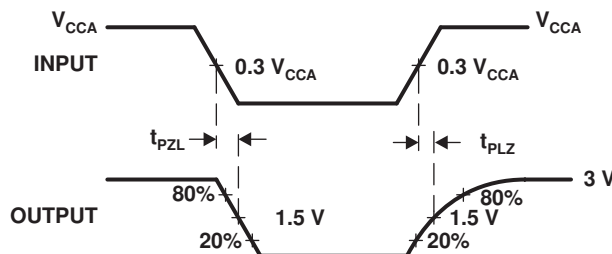


Figure 3. Waveform 2 – Propagation Delay and Transition Times for A Side to B Side

Parameter Measurement Information (continued)

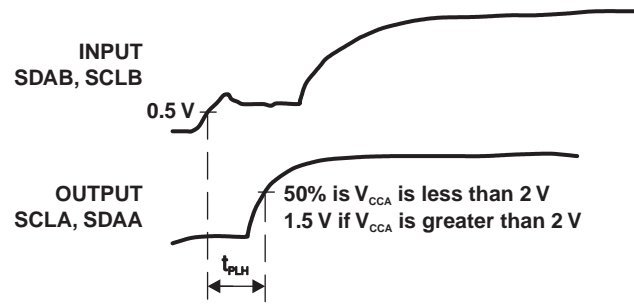
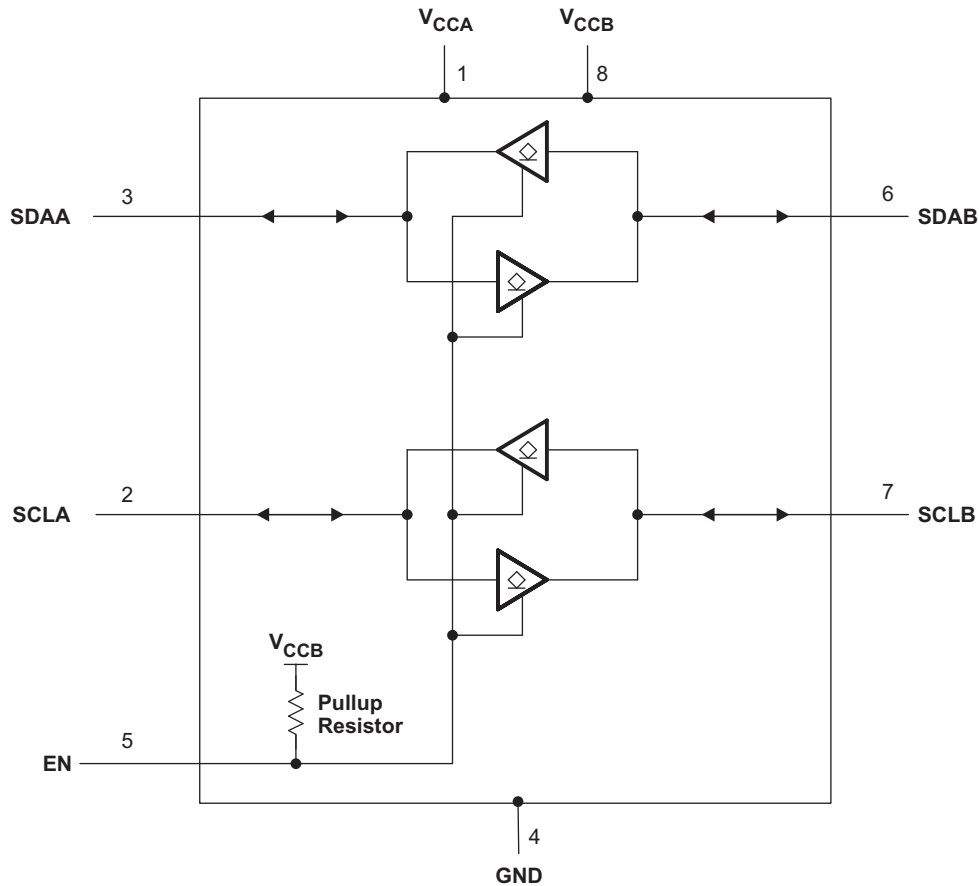


Figure 4. Waveform 3

8 Detailed Description

8.1 Functional Block Diagram



8.2 Feature Description

8.2.1 Clock Stretching Errata

Description

Due to the static offset on the B-side and the possibility of an overshoot above 500mV during events like clock stretching, the device should not be used with rise time accelerators on the B-side.

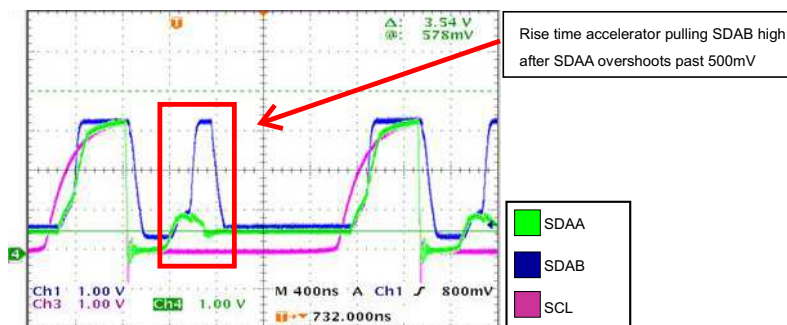


Figure 5. Waveform of Clock Stretching with Rise Time Accelerator on the Bus

System Impact

An incorrect logic state will be transferred to circuits, creating an I2C communication failure on the bus.

System Workaround

Usage of the TCA9517 is recommended.

There are two possible workarounds to avoid an I2C communication failure:

- Removing rise-time accelerators from the B-side bus
- Adding a larger capacitive load to the bus will limit the overshoot

8.2.2 Load Dependent Undershoot Errata

Description

There is a case in which a combination of weak pull-up resistance and light bus loading will cause communication failure through the bus due to undershoot. During a low-to-high transition, when the B-side releases from its 500mV V_{OL} , an undershoot below V_{ILC} can occur. In this event, the A-side will recognize this as a valid low coming from the B-side, causing the A-side to be pulled down by the buffer. The A-side being improperly pulled down by the buffer will trigger the B-side to be pulled low. Since the B-side will be pulled to 500mV, this will not force the A-side to stay low. As the A-side begins transitioning high again, the issue will repeat itself.

System Impact

An incorrect logic state will be transferred to circuits, creating an I2C communication failure on the bus.

System Workaround

Usage of the [TCA9517](#) is recommended.

There are two possible workarounds to avoid an I2C communication failure:

- Removing rise-time accelerators from the B-side bus
- Adding a larger capacitive load to the bus will limit the overshoot

Feature Description (continued)

8.2.3 Glitch/Noise Susceptibility Errata

Description

During the event of a glitch on the SDA/SCL line on one side of the buffer, this glitch can be propagated through and widened by the device during transfer to the other side of the buffer

System Impact

The widened glitch can be recognized as a valid transmission logic, causing a communication failure on the I2C bus

System Workaround

Usage of the TCA9517 is recommended.

Ensure glitch free SDA/SCL lines.

8.2.4 Load Susceptibility Errata

Description

There is a possibility of a race condition of the internal logic of the device that can arise due to bus loading. Within a narrow window, dependent on the following parameters, the internal latch controlling the direction of transfer is set in the wrong state after a falling edge on SCLA/SDAA

- Pull-up resistance
- Bus capacitance
- Temperature

This window location will shift based on the combination of these parameters, therefore cannot be bounded. The typical bus capacitance window is observed to be ~2pF wide for a given pull-up resistance and at a given temperature. The typical temperature window for a given pull-up resistance and bus capacitance is observed to be ~0.8°C wide. This phenomenon can be exacerbated by noise/glitching on the bus.

System Impact

An incorrect logic state will be transferred through the device creating an I2C communication failure on the bus (Figure 6). The bus has the potential to lock under certain external conditions.

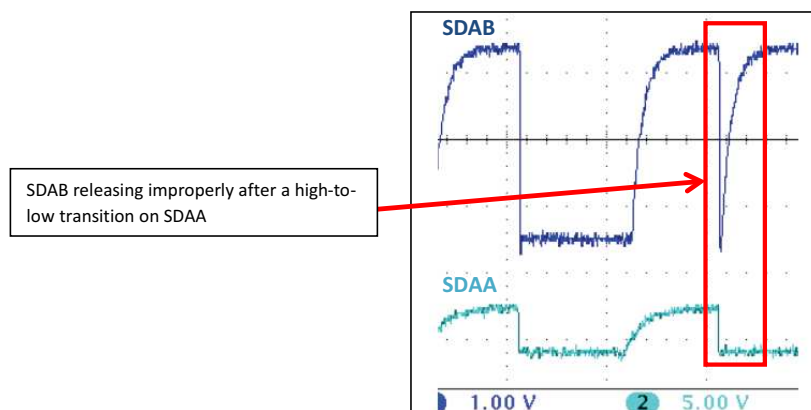


Figure 6. Load Susceptibility Failure Signature

System Workaround

Usage of the [TCA9517](#) is recommended.

8.3 Device Functional Modes

Table 1. Function Table

INPUT EN	FUNCTION
L	Outputs disabled
H	SDAA = SDAB SCLA = SCLB

9 Application and Implementation

9.1 Typical Application

A typical application is shown in Figure 7. In this example, the system master is running on a 3.3-V I²C bus, and the slave is connected to a 1.2-V bus. Both buses run at 400 kHz. Master devices can be placed on either bus.

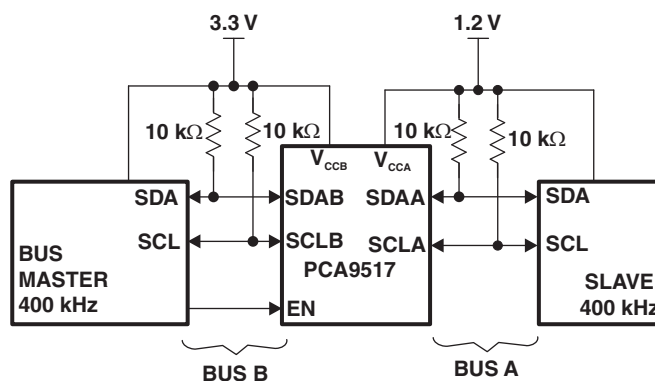


Figure 7. Typical Application

Typical Application (continued)

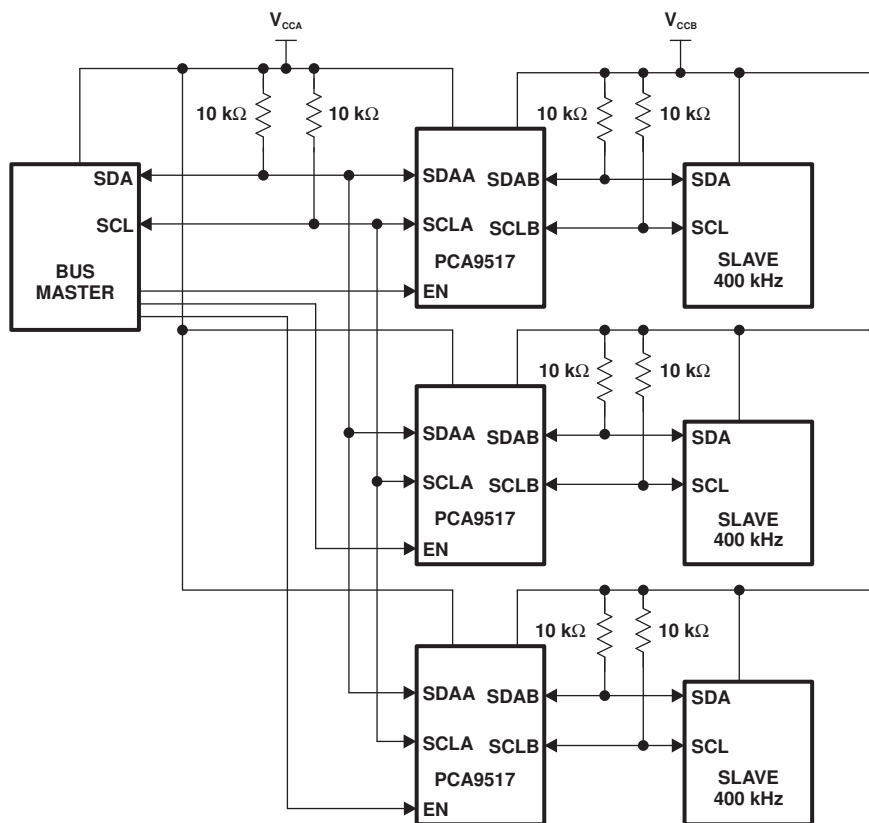


Figure 8. Typical Star Application

9.1.1 Design Requirements

The PCA9517 is 5-V tolerant, so it does not require any additional circuitry to translate between 0.9-V to 5.5-V bus voltages and 2.7-V to 5.5-V bus voltages.

When the A side of the PCA9517 is pulled low by a driver on the I²C bus, a comparator detects the falling edge when it goes below 0.3 V_{CCA} and causes the internal driver on the B side to turn on, causing the B side to pull down to about 0.5 V. When the B side of the PCA9517 falls, first a CMOS hysteresis-type input detects the falling edge and causes the internal driver on the A side to turn on and pull the A-side pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 9 and Figure 10. If the bus master in Figure 7 were to write to the slave through the PCA9517, waveforms shown in Figure 9 would be observed on the A bus. This looks like a normal I²C transmission, except that the high level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the B-side bus of the PCA9517, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the PCA9517. After the eighth clock pulse, the data line is pulled to the V_{OL} of the slave device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver in the PCA9517 for a short delay, while the A-bus side rises above 0.3 V_{CCA} and then continues high.

PCA9517

SCPS157E –DECEMBER 2007–REVISED JUNE 2014

www.ti.com

Typical Application (continued)

9.1.2 Detailed Design Procedure

Multiple PCA9517 A sides can be connected in a star configuration, allowing all nodes to communicate with each other.

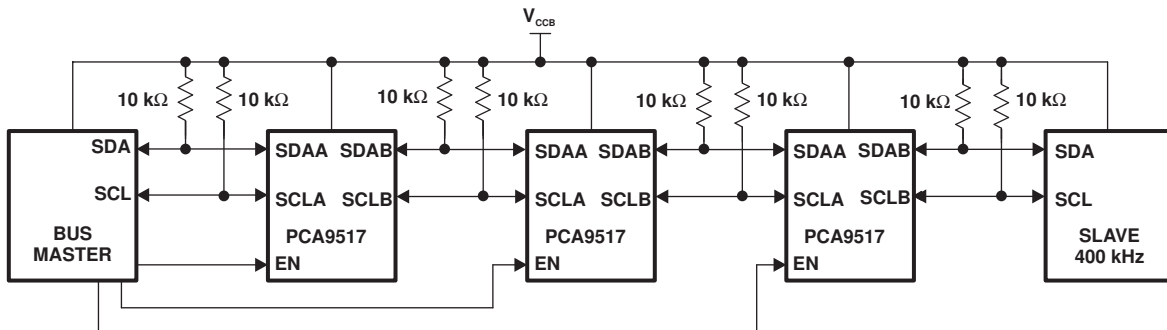


Figure 9. Typical Series Application

Multiple PCA9517s can be connected in series as long as the A side is connected to the B side. I²C bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

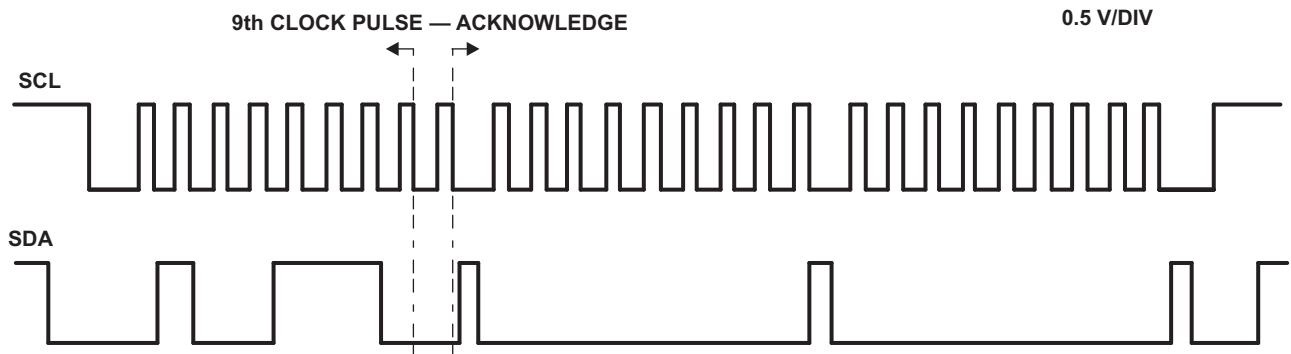


Figure 10. Bus A (0.9-V to 5.5-V Bus) Waveform

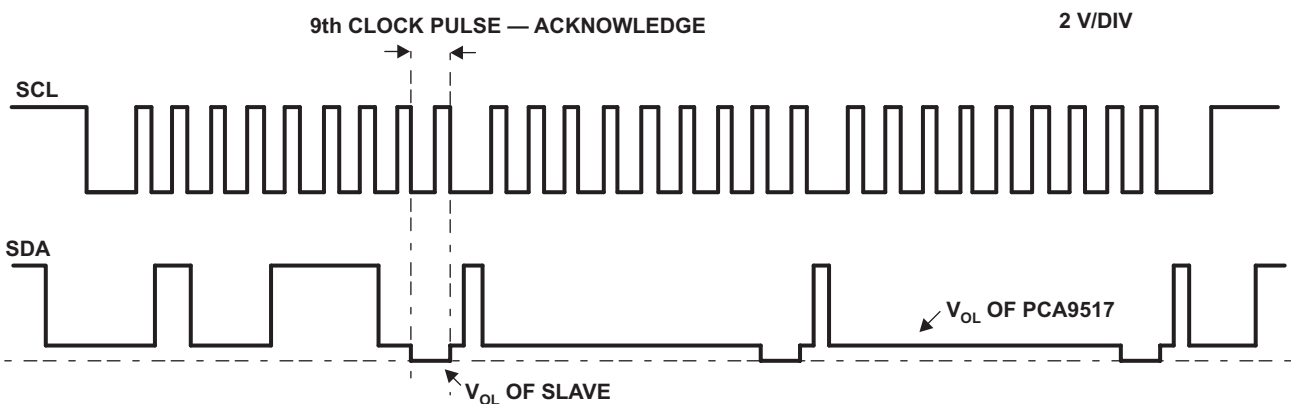


Figure 11. Bus B (2.7-V to 5.5-V Bus) Waveform

10 Device and Documentation Support

10.1 Trademarks

All trademarks are the property of their respective owners.

10.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9517D	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD517	
PCA9517DG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD517	
PCA9517DGKR	NRND	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(7EA ~ 7EE ~ 7EF)	
PCA9517DGKRG4	NRND	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(7EA ~ 7EE ~ 7EF)	
PCA9517DR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD517	
PCA9517DRG4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD517	
PCA9517P	NRND	PDIP	P	8		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9517DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
PCA9517DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
PCA9517DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9517DGKR	VSSOP	DGK	8	2500	346.0	346.0	35.0
PCA9517DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
PCA9517DR	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.