TPD5S116 HDMI Companion Chip with ESD Protection, Level Shifting Buffers, 5V Load Switch with Current Limit

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  – ±15-kV Contact Discharge on External Lines
  – ±15-kV Air-gap Discharge on External Lines
- Conforms to HDMI Control and 5VOUT Compliance Tests without External Components
- Supports HDMI1.3, HDMI1.4, and HDMI2.0 Standards
- Auto-direction Sensing I2C Level Shifter with One-Shot Circuit to Drive Long HDMI Cable (750-pF Load)
- Back Drive Protection
- 55-mA Load Switch with Current Limit for Short Circuit Protection
- Hot Plug Detect Module with Pull Down Resistor
- Integrated Pull-up and Pull-down Resistors per HDMI Specification
- Utility Pin ESD Protection for Ethernet and Audio Return

2 Applications

- End Equipment
  – Cell Phones
  – eBook
  – Portable Media Players
  – Tablet
  – Set Top Box
- Interfaces
  – HDMI

3 Description

TPD5S116 is a single-chip HDMI interface Electrostatic Discharge (ESD) protection device with auto-direction sensing I2C voltage level shifting buffers and a 5-V HDMI compliant current limited load switch. Other key features are hot-plug-detect and Transient Voltage Suppression (TVS) with ESD protection diodes. Each connector-side pin has a TVS diode for circuit protection from ESD. An internal 3.3-V node powers the CEC pin, eliminating the need for a 3.3-V supply on board.

TPD5S116 integrates all external termination resistors needed for the HPD, CEC, SCL, and SDA lines. There are three non-inverting bi-directional translation circuits for the SDA, SCL, and CEC lines. Each has a common power rail (VCCA) on system side from 1.1 V to 3.6 V. A 55-mA current limiting switch regulates current sent from 5V_SYS to 5V_CON. The SCL and SDA pins meet the I2C specification and can drive capacitive loads greater than 750 pF, which exceeds HDMI2.0 specifications. The HPD_CON port has a glitch filter to avoid false detection due to plug bouncing during the HDMI connector insertion.

The TPD5S116 offers reverse current blocking at the 5V_CON pin. In fault conditions, such as when two HDMI transmitters are connected to the same HDMI cable, TPD5S116 ensures that the system is safe from powering up through an external HDMI transmitter. The SCL_CON, SDA_CON, CEC_CON, and HPD_CON pins also feature reverse-current blocking, which ensures that the system sees no leakage if an HDMI receiver is connected while the system is powered off.

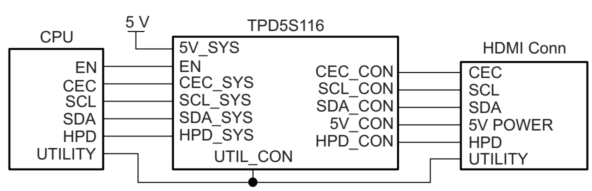
The EN pin enables the hot-plug detect and load switch. The level shifters are enabled after a valid HPD signal is detected.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD5S116	DSBGA (15)	2.13 mm x 1.33 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



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5 Revision History

Changes from Revision B (April 2015) to Revision C **Page**

- Updated non-technical formatting. 1

Changes from Revision A (March 2012) to Revision B **Page**

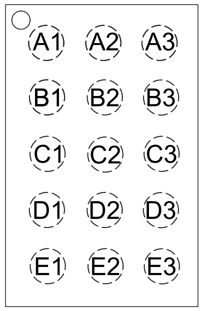
- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. 1
- Updated datasheet to reflect HDMI2.0 compliance. 1

Changes from Original (December 2012) to Revision A **Page**

- Changed the YFF package dimensions 1

6 Pin Configuration and Functions

YFF Package
15-Pin DSBGA
Top View



Pin Assignments

	1	2	3
A	CEC_SYS	V_{CCA}	CEC_CON
B	SCL_SYS	GND	SCL_CON
C	SDA_SYS	EN	SDA_CON
D	5V_SYS	GND	5V_CON
E	HPD_SYS	UTI_CON	HPD_CON

Pin Functions

PIN		I/O	DESCRIPTION
NAME	DSBGA		
5V_CON	D3	Output Power	HDMI connector-side external 5V Supply; output of load switch
5V_SYS	D1	Input Power	System-side PCB 5V supply; input of load switch
CEC_SYS	A1	IO Port	HDMI system-side CEC signal pin referenced to V_{CCA}. Connect to HDMI controller.
CEC_CON	A3	IO Port	HDMI connector-side CEC signal pin referenced to internal 3.3V supply. Connect to HDMI connector CEC pin.
EN	C2	Control Input	Disables the load switch and HPD when EN =L. The EN pin is referenced to V_{CCA}
GND	B2, D2	Ground	Connect to System Ground Plane
HPD_SYS	E1	Output	HDMI system-side: Hot plug detect Output referenced to V_{CCA}. Connect to HDMI controller Hot plug detect input pin
HPD_CON	E3	Input	HDMI connector-side: Hot plug detect Input. Connect directly to HDMI Connector Hot Plug Detect pin
SCL_CON	B3	IO Port	HDMI connector-side SCL signal pin referenced to 5V_CON supply. Connect to HDMI connector SCL pin.
SDA_CON	C3	IO Port	HDMI connector-side SDA signal pin referenced to 5V_CON supply. Connect to HDMI connector SDA pin.
SCL_SYS	B1	IO Port	HDMI system-side SCL signal pin referenced to V_{CCA}. Connect to HDMI controller.
SDA_SYS	C1	IO Port	HDMI system-side SDA signal pin referenced to V_{CCA}. Connect to HDMI controller.
UTI_CON	E2	IO Port	Protects the HDMI connector's utility pin
V_{CCA}	A2	Input Supply	Internal PCB Low Voltage Supply (Same as the HDMI Controller Chip Supply)

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.3	6	V
5V_SYS	Supply voltage range		–0.3	6	V
V_I	Input voltage range(2)	SCL_SYS, SDA_SYS, CEC_SYS, EN	–0.3	6	V
		SCL_CON, SDA_CON, CEC_CON, HPD_CON	–0.3	6	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)(3)	SCL_SYS, SDA_SYS, CEC_SYS, HPD_SYS	–0.3	6	V
		SCL_CON, SDA_CON, CEC_CON, HPD_CON	–0.3	6	
V_O	Voltage range applied to any output in the high or low state(2)(3)	SCL_SYS, SDA_SYS, CEC_SYS,HPD_SYS	–0.3	V_{CCA} + 0.5	V
		SCL_CON, SDA_CON, CEC_CON	–0.3	5V_SYS + 0.5	
I_{IK}	Input clamp current	VI < 0		–50	mA
I_{OK}	Output clamp current	VO < 0		–50	mA
	Continuous current through 5V_SYS, or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)			
		IEC 61000-4-2 Contact Discharge	Pins SCL_CON, SDA_CON, CEC_CON, HPD_CON, 5V_CON, UTI_CON	±15000	
		IEC 61000-4-2 Air-gap ESD			

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as 2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as 2000 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CCA}	Supply Voltage			1.1		5.5	V
5V_SYS	Supply Voltage			4.5		5.5	V
V_{IH}	High-level input voltage	SCL_SYS, SDA_SYS,	V_{CCA} = 1.1 V to 5.5 V	0.7 × V_{CCA}		V_{CCA}	V
		CEC_SYS,	V_{CCA} = 1.1 V to 5.5 V	0.7 × V_{CCA}		V_{CCA}	V
		EN	V_{CCA} = 1.1 V to 5.5 V	1		V_{CCA}	V
		SCL_CON, SDA_CON,	5V_ SYS = 5.5 V	0.7 × 5V_SYS		5V_SYS	V
		CEC_CON	5V_ SYS = 5.5 V	0.7 ×V_{3P3}		V_{3P3}	
		HPD_CON	5V_ SYS = 5.5 V	2		5V_SYS	
V_{IL}	Low-level input voltage	SCL_SYS, SDA_SYS,	V_{CCA} = 1.1 V to 5.5 V	–0.5		0.082 × V_{CCA}	V
		CEC_SYS,	V_{CCA} = 1.1 V to 5.5 V	–0.5		0.082 × V_{CCA}	V
		EN	V_{CCA} = 1.1 V to 5.5 V	–0.5		0.4	V
		SCL_CON, SDA_CON,	5V_ SYS = 5.5 V	–0.5		0.3 × 5V_SYS	V
		CEC_CON	5V_ SYS = 5.5 V	–0.5		0.3 × V_{3P3}	V
		HPD_CON	5V_ SYS = 5.5 V	0		0.8	V
V_{ILC}	(contention) Low-level input voltage	SCL_SYS, SDA_SYS, CEC_SYS	V_{CCA} = 1.1 V to 5.5 V	–0.5		0.0524 × V_{CCA}	V
$V_{OL} – V_{ILC}$	Delta between VOL and VILC	SCL_SYS, SDA_SYS, CEC_SYS	V_{CCA} = 1.8 V		0.1 × V_{CCA}		mV
T_A	Operating free-air temperature			–40		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPDSS116 YFF (DSBGA) 12 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	79.6	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	0.6	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	13	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	2.4	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	13	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) and V_{CCA} = 1.1 V to 5.5 V and 5V_SYS = 5.5 V. Typical values measured at V_{CCA} = 1.8 V and 5V_SYS = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current						
I_{CC5V}	Disabled	5V_SYS =5V, 5V_CON =Open EN = GND, HPD_CON = GND		2	10	µA
	Load Switch active	5V_SYS =5V, 5V_CON =Open EN = V_{CCA}, HPD_CON = GND		30	50	µA
	Active	5V_SYS =5V, 5V_CON =Open EN = V_{CCA}, HPD_CON = 5V		125	200	µA
Load Switch						
V_{REV}	Reverse voltage comparator trip point	5V_SYS=4V, 5V_CON > 5V_SYS		100		mV
I_{OFF}	Leakage Current	5V_CON = 0V, 5V_SYS = 5 V , EN = GND, HPD_CON = GND Measured at 5V_SYS pin.		1	5	µA
		5V_CON = 0V, 5V_SYS= 5 V , EN = GND, HPD_CON = 5 V Measured at 5V_SYS pin		1	5	µA
		5V_CON = 5V, 5V_SYS = 0 V , EN = GND, HPD_CON = GND Measured at 5V_CON pin.		1	5	µA
		5V_CON = 5V, 5V_SYS = 0 V EN = GND, HPD_CON = 5 V Measured at 5V_CON pin.		1	5	µA
		5V_CON = 5V, 5V_SYS = 0 V, EN=V_{CCA}, HPD_CON = GND Measured at 5V_CON pin.		1	5	µA
		5V_CON = 5 V, 5V_SYS = 0 V, EN = V_{CCA}, HPD_CON = 5 V Measured at 5V_CON pin.		1	5	µA
I_{SC}	Short circuit current at 5V_CON	5V_SYS = 5 V, 5V_CON = GND	110	140	170	mA
$T_{DEGLITCH}$	Deglitch time against false short	5V_SYS = 5 V , EN = V_{CCA}, Short 5V_CON		3		µs
UVLO	Under voltage lockout rising	5V_SYS = 0 V to 5 V, RL = 100 Ω, CL = 1 µF		2.85		V
UVLO_HYS	Under voltage lockout falling hysteresis	5V_SYS = 5 V to 0 V, RL = 100 Ω, CL = 1 µF		200		mV
V_{DROP}	5V_OUT output voltage drop	5V_SYS = 5 V, I5V_OUT = 55 mA		38.5	55	mV
I_{RUSH}	Inrush Current	5V_SYS = 5 V, RL = 100 Ω, Cin=10uF, C = 1 µF		140		mA
T_{ON}	Turn on Time, EN to 5V_CON	5V_SYS = 5 V, RL = 100 Ω, Cin=10uF, C = 1 µF		92.3		µs
T_{OFF}	Turn off Time, EN to 5V_CON	5V_SYS = 5 V, RL = 100 Ω, Cin=10uF, C = 1 µF		5		µs
T_{SHUT}	Thermal Shutdown	Shutdown threshold, TRIP(1)		166		°C
		HYST(2)		23		°C

(1) The TPD5S116 turns off after the device temperature reaches the TRIP temperature.
(2) Once the thermal shut-down circuit turns off the load switch, the switch turns on again after the device junction temperature cools down to a temperature equals to or less than TRIP-HYST.

7.6 Voltage Level Shifter, SCL, SDA Lines

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	MIN	TYP	MAX	UNIT
V_{OH_SYS}		I_{OH} = –10 μA	$V_I = V_{IH}$		0.8 × V_{CCA}		V_{CCA} + 0.02	V
V_{OL_SYS}		I_{OL} = 10 μA	$V_I = V_{IL}$				0.17 × V_{CCA}	V
V_{OH_CON}		I_{OH} = –10 μA	$V_I = V_{IH}$		0.8 x 5V_SYS		5V_SYS+ 0.02	V
V_{OL_CON}		I_{OH} = 3 mA	$V_I = V_{IL}$			0.3	0.4	V
ΔVT Hysteresis at the SDx_IN (VT+ - VT-)						40		mV
ΔVT Hysteresis at the SDx_OUT (VT+ - VT-)						400		mV
R_{PU} (Internal pull-up)		SCL_SYS, SDA_SYS	Pull-up connected to V_{CCA} rail			5		kΩ
R_{PU} (Internal pull-up)		SCL_CON, SDA_CON	Pull-up connected to 5V rail			1.75		kΩ
$I_{PULLUPAC}$ Transient Boosted Pull-up Current (rise-time accelerator)		SCL_CON, SDA_CON	Pull-up connected to 5V rail			13		mA
I_{off}	SYS Port	V_{CCA} = 0V, V_I or V_O = 0 to 3.6 V		0 V			±5	μA
I_{off}	CON Port	5V_CON=0V, V_I or V_O = 0 to 5.5 V		0 V			±5	μA
I_{OZ}	SYS Port	$V_I = V_{CCI}$ or GND					±5	μA

7.7 Voltage Level Shifter, CEC Line

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	MIN	TYP	MAX	UNIT
V_{OH_SYS}		I_{OH} = –10 μA	$V_I = V_{IH}$		0.8 × V_{CCA}		V_{CCA} + 0.02	V
V_{OL_SYS}		I_{OL} = 10 μA	$V_I = V_{IL}$				0.17 × V_{CCA}	V
V_{OH_CON}		I_{OH} = –10 μA	$V_I = V_{IH}$		0.8 x V_{3P3}			V
V_{OL_CON}		I_{OH} = 3 mA	$V_I = V_{IL}$			0.3	0.4	V
ΔVT Hysteresis at the CEC_SYS (VT+ - VT-)						30		mV
ΔVT Hysteresis at the CEC_CON (VT+ - VT-)						283		mV
R_{PU} (Internal pull-up)		CEC_SYS	Pull-up connected to V_{CCA} rail			5		kΩ
R_{PU} (Internal pull-up)		CEC_CON	Pull-up connected to 3.3V rail		22	26	30	kΩ
R_{PD} (Internal pull-down)		CEC_CON	Pull-down connected connector-side			10		MΩ
I_{off}	SYS Port	V_{CCA} = 0V, V_I or V_O = 0 to 3.6 V		0 V			±5	μA
I_{off}	CON Port	5V_CON=0V, V_I or V_O = 0 to 5.5 V		0 V			±1.8	μA
I_{OZ}	SYS Port	$V_I = V_{CCI}$ or GND					±5	μA

7.8 Voltage Level Shifter, HPD Line

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	MIN	TYP	MAX	UNIT
V_{OH_SYS}		I_{OH} = 1 mA	$V_I = V_{IH}$	1.2 V to 5.0 V	V_{CCA} × 0.7			V
$V_{OH\_SYS\_1P1}$		I_{OH} = 100 µA	$V_I = V_{IH}$	1.1 V	V_{CCA} × 0.7			V
V_{OL_SYS}		I_{OL} = 3 µA	$V_I = V_{IL}$	1.2 V to 5.0 V			0.4	V
$V_{OL\_SYS\_1P1}$		I_{OL} = 3 mA	$V_I = V_{IL}$	1.1 V			0.68	V
ΔVT Hysteresis at the CEC_CON (VT+ - VT-)				1.2 V to 5.0 V		500		mV
R_{PD_IN} (Input internal pull-down resistor)			Pull-down connected to GND		60	100	140	kΩ
R_{PD_OUT} (Output internal pull-down resistor)			Pull-down connected to GND		60	100	140	kΩ
TFILT	Glitch Filter Duration	HPD_CON = 5 V, EN = V_{CCA}, Short HPD_SYS				10		µs

7.9 EN

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CCA}	MIN	TYP	MAX	UNIT
$R_{PD\ EN}$ (Internal pull-down resistor)	Pull-down connected to GND	1.8 V		470		kΩ

7.10 Utility Pin

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage				6	V
V_{CLAMP}	Clamp voltage with ESD strike	IPP = 1 A, tp = 8/20 µSec, from I/O to GND(1)		8		V
		IPP = 5 A, tp = 8/20 µSec, , from I/O to GND(1)		10		
R_{DYN}	Dynamic resistance	UTI pin to GND Pin(2)		0.33		Ω
C_{UTI}	Line capacitance	V_{IO}=0V, f=1GHz, I/O to GND		5.5		pF
V_{BR}	Break-down voltage	I_{IO} = 1mA	7			V
I_{LEAK}	Leakage current	V_{IO} = 3V		1	10	nA

(1) Non-repetitive current pulse 8/20us exponentially decaying waveform according to IEC 61000-4-5
(2) Extraction of RDYN using least squares fit of TLP characteristics between I=10A and I=20A

7.11 I/O Capacitances

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITONS	SUPPLY & EN SIGNAL	MIN	TYP	MAX	UNIT
C_I	EN	$V_{BIAS} = V_{CCA}/2$, f = 1 MHz, 30 mV p-p AC signal			8	9	pF
C_I	HPD_CON	V_{BIAS} = 0 V – 5 V , f = 1 MHz, 30 mV p-p AC signal			7	7.5	pF

I/O Capacitances (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITONS	SUPPLY & EN SIGNAL	MIN	TYP	MAX	UNIT
C_{IO}	SYS port	V_{BIAS} = 1.8 V, f = 1 MHz, 30 mV p-p AC signal			6.5	9.5	pF
	CON port	V_{BIAS} = 2.5 V, f = 1 MHz, 30 mV p-p AC signal			15	20	pF
	SCL_CON, SDA_CON	V_{BIAS} = 2.5V, f = 100 kHz, 3.5 V p-p AC signal	V_{CCA}= 3.6 V, 5V_SYS = 5 V, EN = HPD_CON = 0 V		17		pF
	CEC_CON	V_{BIAS} = 1.65 V, f = 100 kHz, 2.5 V p-p AC signal	V_{CCA}= 3.6 V, 5V_SYS = 5 V, EN=HPD_CON = 0 V		13		pF
	CEC_CON	V_{BIAS} = 1.65 V, f = 100 kHz, 2.5 V p-p AC signal	V_{CCA}= 0 V 5V_SYS = 0 V EN = HPD_CON = 0 V		12		pF

7.12 Dynamic Load Characteristics

Propagation delays measured from 50% threshold to 50% threshold, Rise time measured from 30% to 70% threshold, Fall time measured from 70% to 30% threshold

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
C_L	Bus Load Capacitance (connector-side)				750	pF
	Bus Load Capacitance (System Side)				30	

7.13 SCL, SDA Lines, V_{CCA} = 1.2 V

over operating free-air temperature range (unless otherwise noted) and 5V_CON = 5 V; V_{CCA} = 1.2 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	SYS to CON	DDC Channels Enabled		316		ns
		CON to SYS	DDC Channels Enabled		286		ns
T_{PLH}	Propagation Delay	SYS to CON	DDC Channels Enabled		489		ns
		CON to SYS	DDC Channels Enabled		199		ns
T_{FALL}	SYS Port Fall Time	SYS Port	DDC Channels Enabled		110		ns
T_{FALL}	CON Port Fall Time	CON Port	DDC Channels Enabled		82		ns
T_{RISE}	SYS Port Rise Time	SYS Port	DDC Channels Enabled		229		ns
T_{RISE}	CON Port Rise Time	CON Port	DDC Channels Enabled		86		ns
F_{MAX}	Maximum Switching Frequency		DDC Channels Enabled	400			kHz

7.14 CEC Line, V_{CCA} = 1.2 V

over operating free-air temperature range (unless otherwise noted) and 5V_CON = 5 V; V_{CCA} = 1.2 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	SYS to CON	CEC Channels Enabled		436		ns
		CON to SYS	CEC Channels Enabled		97		ns
T_{PLH}	Propagation Delay	SYS to CON	CEC Channels Enabled		13.8		µs
		CON to SYS	CEC Channels Enabled		319		ns
T_{FALL}	SYS Port Fall Time	SYS Port	CEC Channels Enabled		37		ns
T_{FALL}	CON Port Fall Time	CON Port	CEC Channels Enabled		114		ns
T_{RISE}	SYS Port Rise Time	SYS Port	CEC Channels Enabled		234		ns
T_{RISE}	CON Port Rise Time	CON Port	CEC Channels Enabled		16.6		µs

7.15 HPD Line, V_{CCA} = 1.2 V

over operating free-air temperature range (unless otherwise noted) and 5V_CON = 5 V; V_{CCA} = 1.2 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	CON to SYS	CEC Channels Enabled		10.1		µs
T_{PLH}	Propagation Delay	CON to SYS	CEC Channels Enabled		9.7		µs
T_{FALL}	SYS Port Fall Time	SYS Port	CEC Channels Enabled		14		ns
T_{RISE}	SYS Port Rise Time	SYS Port	CEC Channels Enabled		18		ns

7.16 SCL, SDA Lines, V_{CCA} = 1.5 V

over operating free-air temperature range (unless otherwise noted) and 5V_CON = 5 V; V_{CCA} = 1.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	SYS to CON	DDC Channels Enabled		297		ns
		CON to SYS	DDC Channels Enabled		224		ns
T_{PLH}	Propagation Delay	SYS to CON	DDC Channels Enabled		473		ns
		CON to SYS	DDC Channels Enabled		193		ns
T_{FALL}	SYS Port Fall Time	SYS Port	DDC Channels Enabled		87		ns
T_{FALL}	CON Port Fall Time	CON Port	DDC Channels Enabled		82		ns
T_{RISE}	SYS Port Rise Time	SYS Port	DDC Channels Enabled		226		ns
T_{RISE}	CON Port Rise Time	CON Port	DDC Channels Enabled		86		ns
F_{MAX}	Maximum Switching Frequency		DDC Channels Enabled	400			kHz

7.17 CEC Line, V_{CCA} = 1.5 V

over operating free-air temperature range (unless otherwise noted) and 5V_CON = 5 V; V_{CCA} = 1.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	SYS to CON	CEC Channels Enabled		419		ns
		CON to SYS	CEC Channels Enabled		102		ns
T_{PLH}	Propagation Delay	SYS to CON	CEC Channels Enabled		13.7		µs
		CON to SYS	CEC Channels Enabled		314		ns
T_{FALL}	SYS Port Fall Time	SYS Port	CEC Channels Enabled		39		ns
T_{FALL}	CON Port Fall Time	CON Port	CEC Channels Enabled		115		ns
T_{RISE}	SYS Port Rise Time	SYS Port	CEC Channels Enabled		230		ns
T_{RISE}	CON Port Rise Time	CON Port	CEC Channels Enabled		16.6		µs

7.18 HPD Line, V_{CCA} = 1.5 V

over operating free-air temperature range (unless otherwise noted) and 5V_CON = 5 V; V_{CCA} = 1.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	CON to SYS	CEC Channels Enabled		10.1		µs
T_{PLH}	Propagation Delay	CON to SYS	CEC Channels Enabled		9.7		µs
T_{FALL}	SYS Port Fall Time	SYS Port	CEC Channels Enabled		8		ns
T_{RISE}	SYS Port Rise Time	SYS Port	CEC Channels Enabled		9.5		ns

7.19 SCL, SDA Lines, V_{CCA} = 1.8 V

over operating free-air temperature range (unless otherwise noted) and 5V_CON = 5 V; V_{CCA} = 1.8 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	SYS to CON	DDC Channels Enabled		292		ns
		CON to SYS	DDC Channels Enabled		192		ns
T_{PLH}	Propagation Delay	SYS to CON	DDC Channels Enabled		466		ns
		CON to SYS	DDC Channels Enabled		190		ns
T_{FALL}	SYS Port Fall Time	SYS Port	DDC Channels Enabled		75		ns
T_{FALL}	CON Port Fall Time	CON Port	DDC Channels Enabled		82		ns
T_{RISE}	SYS Port Rise Time	SYS Port	DDC Channels Enabled		224		ns
T_{RISE}	CON Port Rise Time	CON Port	DDC Channels Enabled		86		ns
F_{MAX}	Maximum Switching Frequency		DDC Channels Enabled	400			kHz

7.20 CEC Line, V_{CCA} = 1.8 V

over operating free-air temperature range (unless otherwise noted) and 5V_CON = 5 V; V_{CCA} = 1.8 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	SYS to CON	CEC Channels Enabled		417		ns
		CON to SYS	CEC Channels Enabled		108		ns
T_{PLH}	Propagation Delay	SYS to CON	CEC Channels Enabled		13.7		µs
		CON to SYS	CEC Channels Enabled		312		ns
T_{FALL}	SYS Port Fall Time	SYS Port	CEC Channels Enabled		41		ns
T_{FALL}	CON Port Fall Time	CON Port	CEC Channels Enabled		114		ns
T_{RISE}	SYS Port Rise Time	SYS Port	CEC Channels Enabled		228		ns
T_{RISE}	CON Port Rise Time	CON Port	CEC Channels Enabled		16.6		µs

7.21 HPD Line, V_{CCA} = 1.8 V

over operating free-air temperature range (unless otherwise noted) and 5V_CON = 5V; V_{CCA} = 1.8 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	CON to SYS	CEC Channels Enabled		10.1		µs
T_{PLH}	Propagation Delay	CON to SYS	CEC Channels Enabled		9.7		µs
T_{FALL}	SYS Port Fall Time	SYS Port	CEC Channels Enabled		5.5		ns
T_{RISE}	SYS Port Rise Time	SYS Port	CEC Channels Enabled		7		ns

7.22 SCL, SDA Lines, V_{CCA} = 2.5 V

over operating free-air temperature range (unless otherwise noted) and 5V_CON = 5 V; V_{CCA} = 2.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	SYS to CON	DDC Channels Enabled		291		ns
		CON to SYS	DDC Channels Enabled		154		ns
T_{PLH}	Propagation Delay	SYS to CON	DDC Channels Enabled		455		ns
		CON to SYS	DDC Channels Enabled		186		ns
T_{FALL}	SYS Port Fall Time	SYS Port	DDC Channels Enabled		64		ns
T_{FALL}	CON Port Fall Time	CON Port	DDC Channels Enabled		82		ns
T_{RISE}	SYS Port Rise Time	SYS Port	DDC Channels Enabled		221		ns
T_{RISE}	CON Port Rise Time	CON Port	DDC Channels Enabled		86		ns
F_{MAX}	Maximum Switching Frequency		DDC Channels Enabled	400			kHz

7.23 CEC Line, V_{CCA} = 2.5 V

over operating free-air temperature range (unless otherwise noted) and 5V_CON = 5 V; V_{CCA} = 2.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	SYS to CON	CEC Channels Enabled		421		ns
		CON to SYS	CEC Channels Enabled		122		ns
T_{PLH}	Propagation Delay	SYS to CON	CEC Channels Enabled		13.7		µs
		CON to SYS	CEC Channels Enabled		311		ns
T_{FALL}	SYS Port Fall Time	SYS Port	CEC Channels Enabled		49		ns
T_{FALL}	CON Port Fall Time	CON Port	CEC Channels Enabled		114		ns
T_{RISE}	SYS Port Rise Time	SYS Port	CEC Channels Enabled		225		ns
T_{RISE}	CON Port Rise Time	CON Port	CEC Channels Enabled		16.6		µs

7.24 HPD Line, V_{CCA} = 2.5 V

over operating free-air temperature range (unless otherwise noted) and 5V_CON = 5 V; V_{CCA} = 2.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	CON to SYS	CEC Channels Enabled		10.1		µs
T_{PLH}	Propagation Delay	CON to SYS	CEC Channels Enabled		9.7		µs
T_{FALL}	SYS Port Fall Time	SYS Port	CEC Channels Enabled		4		ns
T_{RISE}	SYS Port Rise Time	SYS Port	CEC Channels Enabled		5		ns

7.25 SCL, SDA Lines, V_{CCA} = 3.3 V

over operating free-air temperature range (unless otherwise noted) and 5V_CON = 5 V; V_{CCA} = 3.3 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	SYS to CON	DDC Channels Enabled		292		ns
		CON to SYS	DDC Channels Enabled		133		ns
T_{PLH}	Propagation Delay	SYS to CON	DDC Channels Enabled		449		ns
		CON to SYS	DDC Channels Enabled		184		ns
T_{FALL}	SYS Port Fall Time	SYS Port	DDC Channels Enabled		57		ns
T_{FALL}	CON Port Fall Time	CON Port	DDC Channels Enabled		82		ns
T_{RISE}	SYS Port Rise Time	SYS Port	DDC Channels Enabled		218		ns
T_{RISE}	CON Port Rise Time	CON Port	DDC Channels Enabled		86		ns
F_{MAX}	Maximum Switching Frequency		DDC Channels Enabled	400			kHz

7.26 CEC Line, V_{CCA} = 3.3 V

over operating free-air temperature range (unless otherwise noted) and 5V_CON = 5 V; V_{CCA} = 3.3 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	SYS to CON	CEC Channels Enabled		428		ns
		CON to SYS	CEC Channels Enabled		138		ns
T_{PLH}	Propagation Delay	SYS to CON	CEC Channels Enabled		13.7		µs
		CON to SYS	CEC Channels Enabled		309		ns
T_{FALL}	SYS Port Fall Time	SYS Port	CEC Channels Enabled		59		ns
T_{FALL}	CON Port Fall Time	CON Port	CEC Channels Enabled		114		ns
T_{RISE}	SYS Port Rise Time	SYS Port	CEC Channels Enabled		223		ns
T_{RISE}	CON Port Rise Time	CON Port	CEC Channels Enabled		16.6		µs

7.27 HPD Line, V_{CCA} = 3.3 V

over operating free-air temperature range (unless otherwise noted) and 5V_CON = 5 V; V_{CCA} = 3.3 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	CON to SYS	CEC Channels Enabled		10.1		µs
T_{PLH}	Propagation Delay	CON to SYS	CEC Channels Enabled		9.7		µs
T_{FALL}	SYS Port Fall Time	SYS Port	CEC Channels Enabled		3		ns
T_{RISE}	SYS Port Rise Time	SYS Port	CEC Channels Enabled		3.5		ns

7.28 SCL, SDA Lines, V_{CCA} = 5 V

over operating free-air temperature range (unless otherwise noted) and 5V_CON = 5 V; V_{CCA} = 5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	SYS to CON	DDC Channels Enabled		298		ns
		CON to SYS	DDC Channels Enabled		113		ns
T_{PLH}	Propagation Delay	SYS to CON	DDC Channels Enabled		442		ns
		CON to SYS	DDC Channels Enabled		182		ns
T_{FALL}	SYS Port Fall Time	SYS Port	DDC Channels Enabled		52		ns
T_{FALL}	CON Port Fall Time	CON Port	DDC Channels Enabled		82		ns
T_{RISE}	SYS Port Rise Time	SYS Port	DDC Channels Enabled		217		ns
T_{RISE}	CON Port Rise Time	CON Port	DDC Channels Enabled		86		ns
F_{MAX}	Maximum Switching Frequency		DDC Channels Enabled	400			kHz

7.29 CEC Line, V_{CCA} = 5 V

over operating free-air temperature range (unless otherwise noted) and 5V_CON = 5 V; V_{CCA} = 5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	SYS to CON	CEC Channels Enabled		446		ns
		CON to SYS	CEC Channels Enabled		169		ns
T_{PLH}	Propagation Delay	SYS to CON	CEC Channels Enabled		13.7		µs
		CON to SYS	CEC Channels Enabled		306		ns
T_{FALL}	SYS Port Fall Time	SYS Port	CEC Channels Enabled		82		ns
T_{FALL}	CON Port Fall Time	CON Port	CEC Channels Enabled		114		ns
T_{RISE}	SYS Port Rise Time	SYS Port	CEC Channels Enabled		221		ns
T_{RISE}	CON Port Rise Time	CON Port	CEC Channels Enabled		16.6		µs

7.30 HPD Line, V_{CCA} = 5 V

over operating free-air temperature range (unless otherwise noted) and 5V_CON = 5 V; V_{CCA} = 5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PHL}	Propagation Delay	CON to SYS	CEC Channels Enabled		10.1		µs
T_{PLH}	Propagation Delay	CON to SYS	CEC Channels Enabled		9.7		µs
T_{FALL}	SYS Port Fall Time	SYS Port	CEC Channels Enabled		2.5		ns
T_{RISE}	SYS Port Rise Time	SYS Port	CEC Channels Enabled		2.5		ns

7.31 Typical Characteristics

At T_A = 25°C, unless otherwise noted.

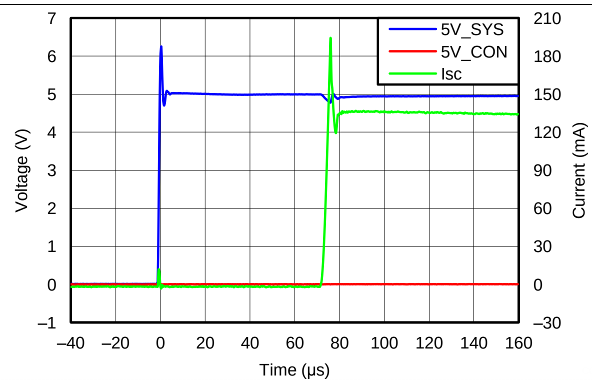


Figure 1. Power up to Short Circuit

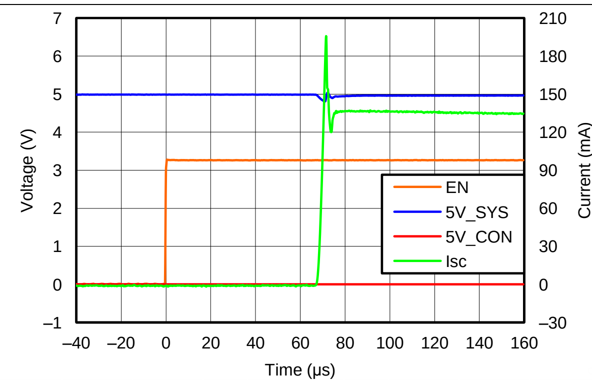


Figure 2. Enable to Short Circuit

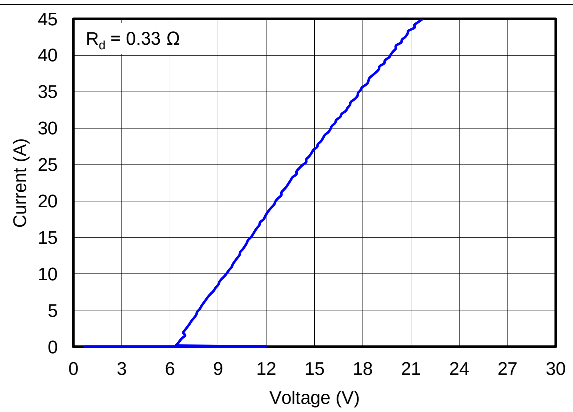


Figure 3. Utility Pin TLP Curve

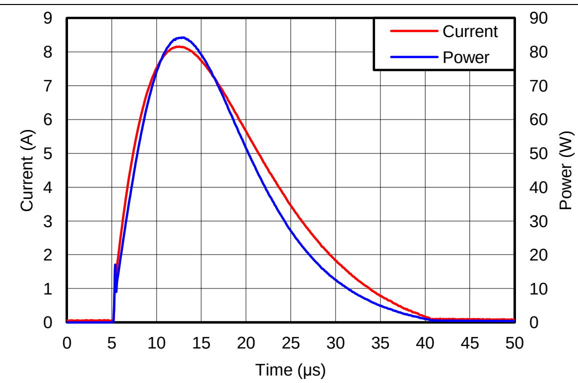


Figure 4. Utility Pin Surge Curves

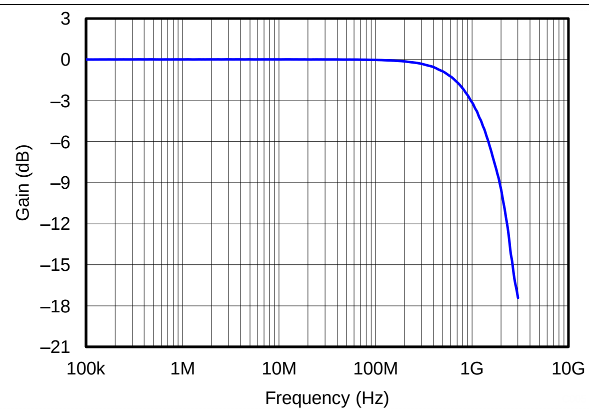


Figure 5. Utility Pin Insertion Loss

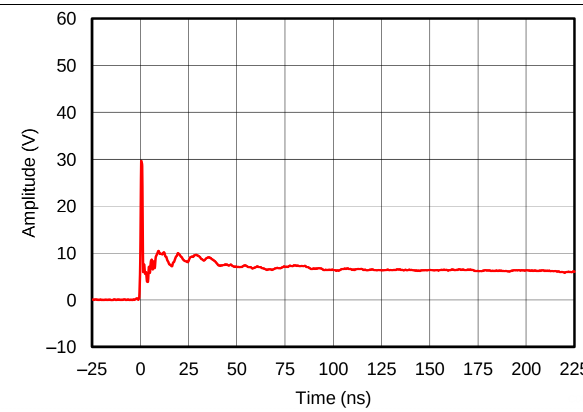


Figure 6. Utility Pin, +8kv IEC Voltage Clamp Waveform

Typical Characteristics (continued)

At T_A = 25°C, unless otherwise noted.

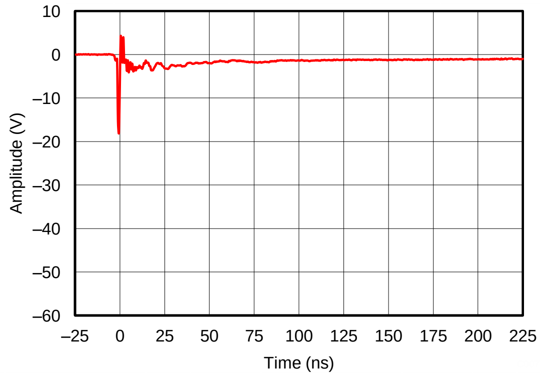


Figure 7. Utility Pin, -8kv IEC Voltage Clamp Waveform

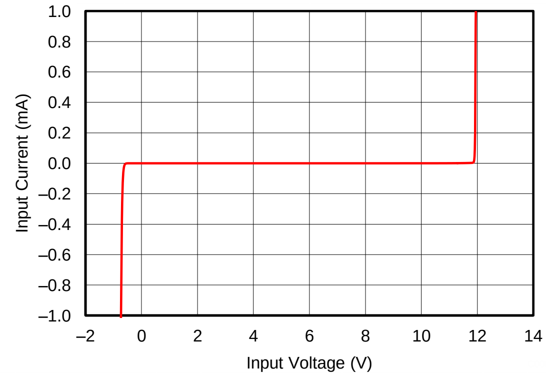


Figure 8. Utility Pin IV Curve

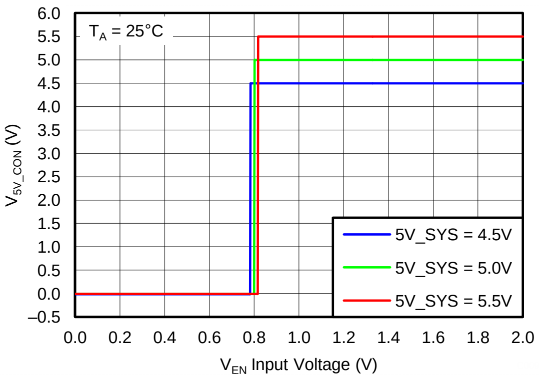


Figure 9. EN V_{TH}

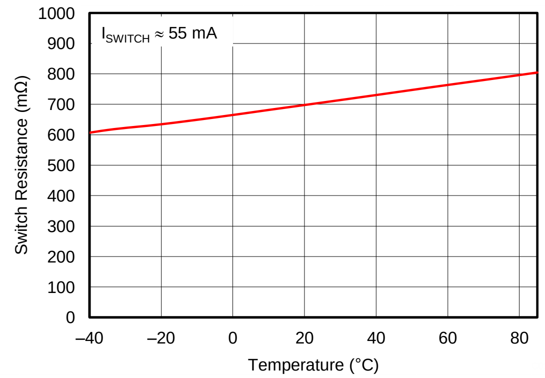


Figure 10. R_{DS} for I_{SWITCH}

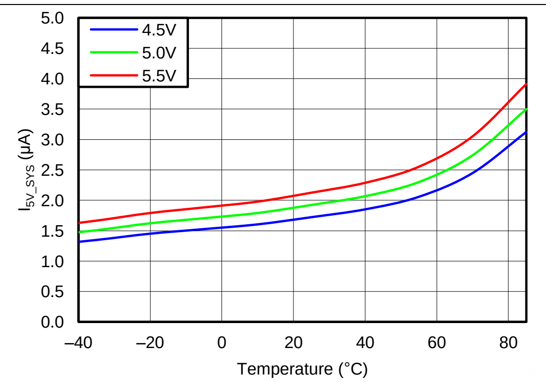


Figure 11. I_{5V_SYS} vs. Temperature

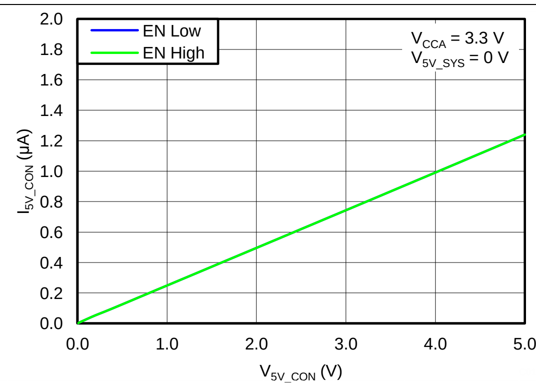


Figure 12. Reverse Switch Current

Typical Characteristics (continued)

At T_A = 25°C, unless otherwise noted.

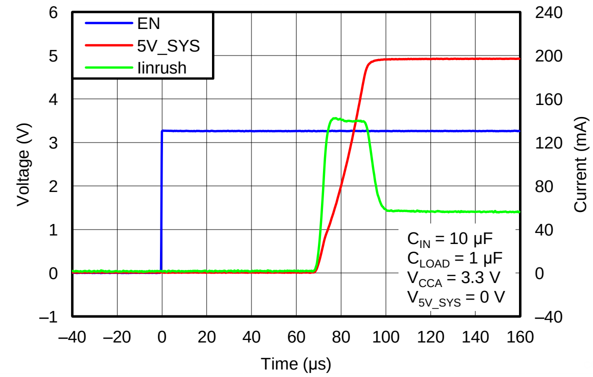


Figure 13. I_{INRUSH} Waveform

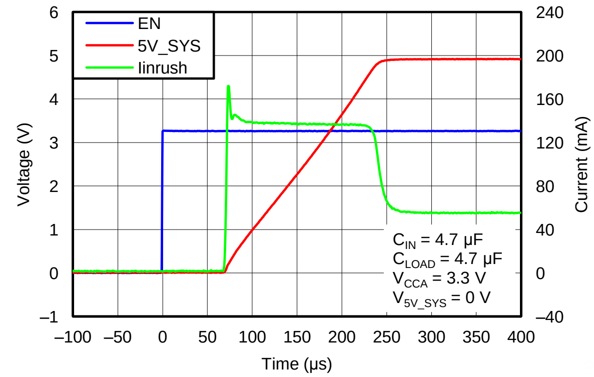


Figure 14. I_{INRUSH} Waveform

8 Detailed Description

8.1 Overview

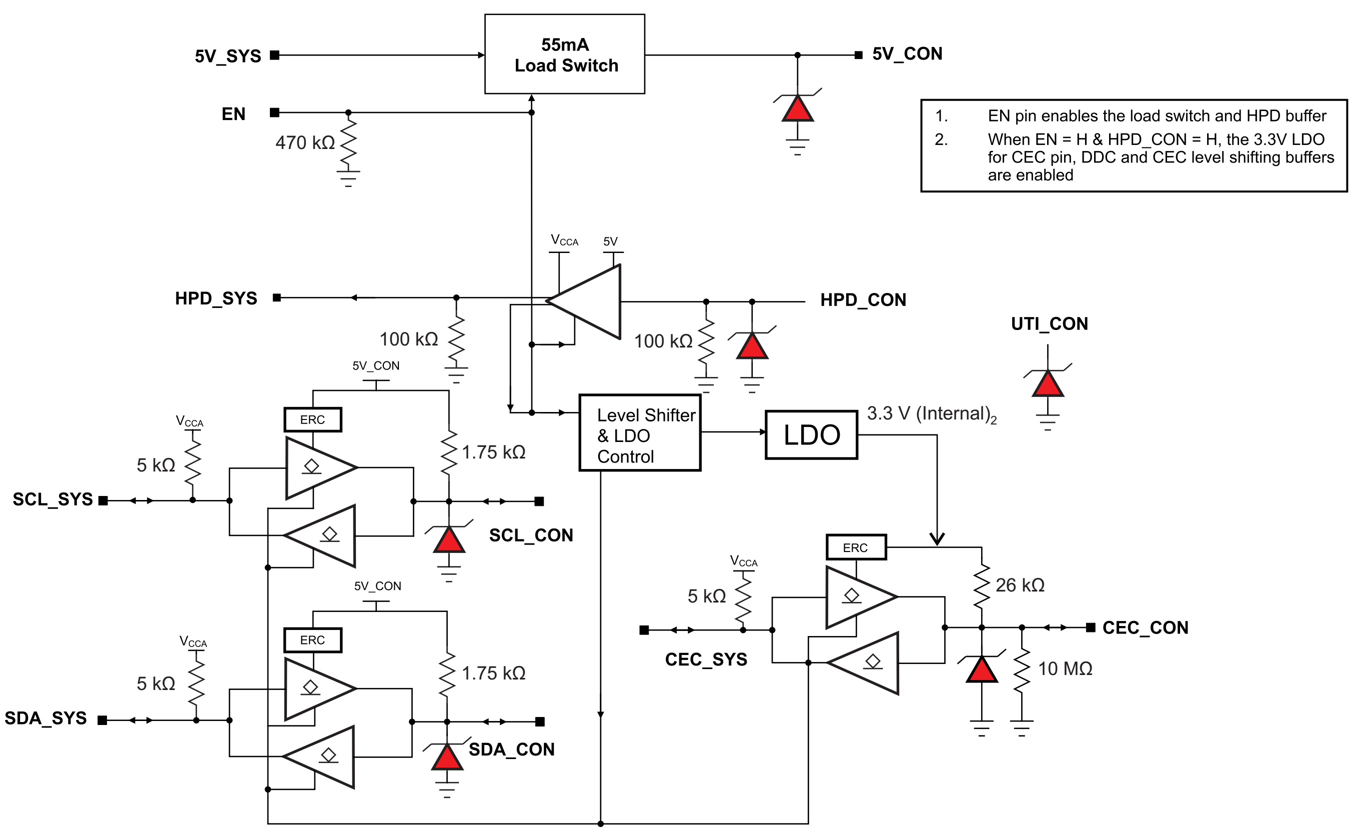
TPD5S116 is a single-chip HDMI interface electrostatic discharge (ESD) protection product with auto-direction sensing I2C voltage level shift buffers, a 5-V HDMI compliant current limited load switch, hot-plug-detect, and transient voltage suppression (TVS) with ESD protection diodes. Each connector-side pin has a TVS diode for circuit protection from ESD. The device pin mapping can be routed to either an HDMI Type D or Type C connector. An internal 3.3-V node powers the CEC pin, eliminating the need for a 3.3-V supply on board.

TPD5S116 integrates all of the external termination resistors at the HPD, CEC, SCL, and SDA lines. There are three non-inverting bidirectional translation circuits for the SDA, SCL, and CEC lines. Each has a common power rail (V_{CCA}) on system-side from 1.1 V to 3.6V. A 55-mA current limiting switch regulates current sent from 5V_SYS to 5V_CON. The SCL and SDA pins meet the I2C specification and can drive capacitive loads greater than 750 pF, which exceeds HDMI2.0 specifications. The HPD_CON port has a glitch filter to avoid false detection due to plug bouncing during the HDMI connector insertion.

The TPD5S116 offers reverse current blocking at the 5V_CON pin. In fault conditions, such as when two HDMI transmitters are connected to the same HDMI cable, TPD5S116 ensures that the system is safe from powering up through external HDMI transmitter. The SCL_CON, SDA_CON, CEC_CON, and HPD_CON pins also feature reverse-current blocking, which ensures that the system sees no leakage if an HDMI receiver is connected while the system is powered off.

The EN pin enables the hot-plug detect and load switch. The level shifters are enabled after a valid HPD signal is detected.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 IEC 61000-4-2 Level 4 ESD Protection

In many cases, the core ICs, such as the scalar chipset, may not have robust ESD cells to sustain system-level ESD strikes. In these cases, the TPD5S116 provides the desired system-level ESD protection, such as the IEC 61000-4-2 Level 4 ESD protection of ±15-kV Contact and Air-gap ratings by absorbing the energy associated with the ESD strike.

8.3.2 Conforms to HDMI Control and 5VOUT Compliance Tests Without External Components

The TPD5S116 is designed to be fully compliant to the HDMI 7-13 Compliance Test. See *HDMI Compliance* for a detailed procedure.

8.3.3 Auto-direction Sensing I2C Level Shifter with One-Shot Circuit to Drive Long HDMI Cable (750-pF Load)

The TPD5S116 contains three bidirectional open-drain buffers specifically designed to support up-translation/ down-translation between the low voltage, V_{CCA} side DDC-bus and the 5-V DDC-bus or 3.3-V CEC line. The HDMI cable side of the DDC lines incorporates rise-time accelerators to support a high capacitive load on the HDMI cable side. The rise time accelerators boost the cable side DDC signal independent of which side of the bus is releasing the signal.

8.3.4 Back Drive Protection

The TPD5S116 offers reverse current blocking at the 5V_CON pin. In fault conditions, such as when two HDMI transmitters are connected to the same HDMI cable, TPD5S116 ensures that the system is safe from powering up through an external HDMI transmitter. The SCL_CON, SDA_CON, CEC_CON, and HPD_CON pins also feature reverse-current blocking, which ensures that the system sees no leakage if an HDMI receiver is connected while the system is powered off.

8.3.5 55-mA Load Switch with Short Circuit Protection

A 55-mA current limiting switch regulates current sent from 5V_SYS to 5V_CON. This provides protection from a short-circuit or excessive load when there is a fault condition, such as a defective HDMI cable.

8.3.6 Hot Plug Detect Module with Pull Down Resistor

Once TPD5S116 is enabled and the system's 5-V source is on, TPD5S116 is ready for continual HDMI receiver detection. When an HDMI cable connects a receiving and transmitting device together, the 5 V on the load switch (5V_CON) flows through the receiving device's internal resistor and into HPD's input (HPD_CON). The HPD buffer's output (HPD_SYS) then goes high, indicating to the transmitter that a receiving device is connected. To save power, periodic detection can be done by turning on and off the TPD5S116 before a receiving device is connected. HPD_CON port has a glitch filter to avoid false detection due to plug bouncing during the HDMI connector insertion. An integrated pull-down resistor for HPD_CON eliminates the need for an additional external component.

8.3.7 Integrated Pull-up and Pull-down Resistors per HDMI Specification

The system is designed to work properly according to the HDMI 2.0 specification with no external pull-up resistors on the DDC, CEC, and HPD lines.

8.3.8 Utility Pin ESD Protection for Ethernet and Audio Return

A TVS is provided for the Utility Pin in the HDMI connector. This pin should be routed to the TPD5S116 for proper ESD protection regardless of whether Utility is used in the application.

8.3.9 DDC/CEC LEVEL SHIFT Circuit Operation

The TPD5S116 enables DDC translation from V_{CCA} (system-side - Port A in Figure 15) voltage levels to 5-V (HDMI connector-side - Port B in Figure 15) voltage levels without degradation of system performance. The TPD5S116 contains two bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage, V_{CCA} side DDC-bus and the 5-V DDC-bus. The connector port I/Os are over-voltage tolerant to 5.5 V, even when the device is un-powered. After power-up and with enable pin and

Feature Description (continued)

HPD_CON pin HIGH, a LOW level on the system port (below approximately V_{ILC} = 0.08 × V_{CCA} V) turns the connector port driver (either SDA or SCL) on and drives port B down to V_{OL_CON} V. When the system port rises above approximately 0.10 × V_{CCA} V, the connector port pull-down driver is turned off and the internal pull-up resistor pulls the pin HIGH. When the connector port falls first and goes below 0.3 × 5 V_CON V, a CMOS hysteresis input buffer detects the falling edge, turns on the system port driver, and pulls port A down to approximately V_{OLA}. The connector port pull-down is not enabled unless the system port voltage goes below V_{ILC}, in which case the connector port pull-down driver is enabled until system port rises above (V_{ILC} + $\Delta V_{T\text{-}HYSTA}$). If the connector port is not externally driven LOW, its voltage will continue to rise due to the internal pull-up resistor.

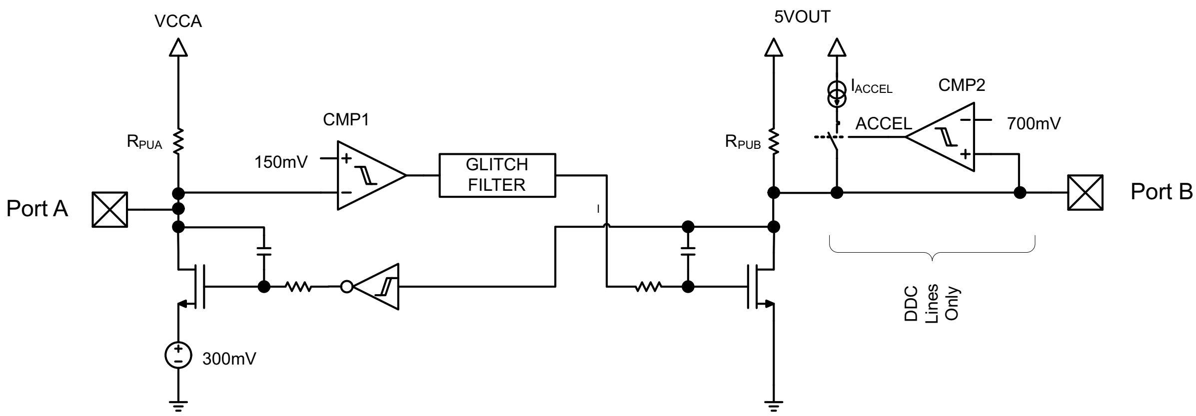


Figure 15. DDC/CEC Level Shifter Block Diagram

8.3.10 DDC/CEC Level Shifter Operational Notes For V_{CCA} = 1.8V

- The threshold of CMP1 is ~150 mV +/- the 40mV of total hysteresis.
- The comparator will trip for a falling waveform at ~130mV
- The comparator will trip for a rising waveform at ~170mV
- To be recognized as a zero, the level at system port must first go below 130mV (V_{ILC} in spec) and then stay below 170mV (V_{IL_SYS} in spec)
- To be recognized as a one, the level at system port must first go above 170mV and then stay above 130mV
- V_{ILC} is set to 110mV in Electrical Characteristics Table to give some margin to the 130mV
- V_{IL_SYS} is set to 140mV in the Electrical Characteristics Table to give some margin to the 170mV
- V_{IH_SYS} is set to 70% of V_{CCA} to be consistent with standard CMOS levels

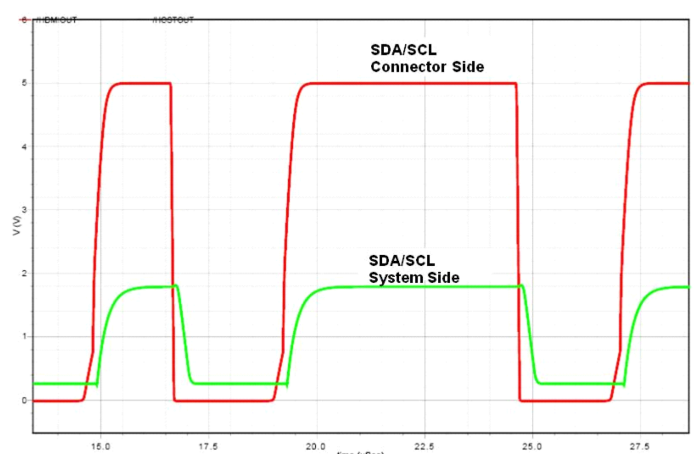


Figure 16. DDC Level Shifter Operation (Connector To System Direction)

Feature Description (continued)

8.3.11 Rise-Time Accelerators

The HDMI cable side of the DDC lines incorporates rise-time accelerators to support the high capacitive load on the HDMI cable side. The rise time accelerator boosts the cable side DDC signal independent of which side of the bus is releasing the signal.

8.3.12 Noise Considerations

Ground offset between the TPD5S116 ground and the ground of devices on the system port of the TPD5S116 must be avoided. The reason for this cautionary remark is that a CMOS/NMOS open-drain capable of sinking 3 mA of current at 0.4 V will have an output resistance of 133Ω or less (R = E / I). Such a driver will share enough current with the system port output pull-down of the TPD5S116 to be seen as a LOW as long as the ground offset is zero. If the ground offset is greater than 0 V, then the driver resistance must be less. Since V_{ILC} can be as low as 90 mV at cold temperatures and the low end of the current distribution, the maximum ground offset should not exceed 50 mV. Bus repeaters that use an output offset are not interoperable with the system port of the TPD5S116 as their output LOW levels will not be recognized by the TPD5S116 as a LOW. If the TPD5S116 is placed in an application where the V_{IL_SYS} does not go below V_{ILC}, it will pull connector port LOW initially when system port input transitions LOW but the connector port will return HIGH, so it will not reproduce the system port input on connector port. Such applications should be avoided. The connector port is interoperable with all I2C-bus slaves, masters and repeaters.

8.3.13 HDMI Compliance

The TPD5S116 is designed to be fully compliant to the HDMI 7-13 capacitance specification. Both power on and power off capacitance measurements are done on the CEC, SDA, and SCL connector-side pins using a Hioki 3522-50 meter. In the power on setup, connect TPD5S116's EN and HPD_CON pins low and 5V_SYS and V_{CCA} pins high. Use the Hioki meter to measure the test fixture with and without the TPD5S116 and subtract to obtain the capacitance. In the power off setup, connect TPD5S116's EN, HPD_CON, 5V_SYS, and V_{CCA} pins low and conduct the same test with the Hioki meter. Read the C_p result from the Hioki meter.

- SCL_CON, SDA_CON Test:
  - Measure the large signal capacitance at SCL_CON & SDA_CON pins at either power-up or power down conditions:
    - VBIAS = 2.5 V
    - f = 100 kHz
    - 3.5 V p-p ac signal
- CEC Test:
  - Measure the large signal capacitance of the CEC_CON pin at both power-up and power down conditions:
    - VBIAS = 1.65 V,
    - f = 100 kHz
    - 2.5V p-p ac signal

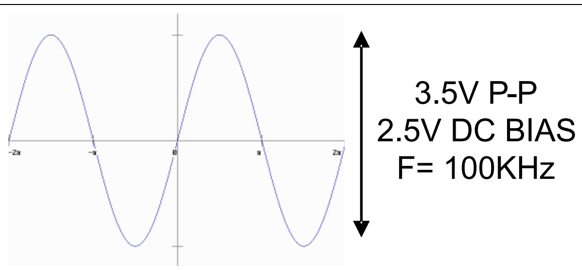


Figure 17. Hioki Meter Signal Set-Up For Scl, Sda Cap Measurement

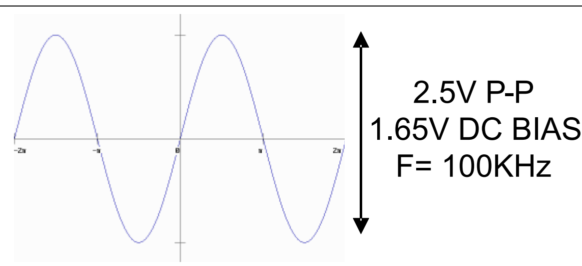


Figure 18. Hioki Meter Signal Set-Up For Cec Cap Measurement

8.4 Device Functional Modes

HDMI Driver Chip is controlling the TPD5S116 via only one control line (EN). The DDC and CEC level shifting buffers become active after HPD_CON receives a valid high signal and EN is high. EN and HPD_CON control the TPD5S116 power saving options according to the following table:

Table 1. Function Table – Power Saving Options

HPD_CON	EN	V_{CCA}	5V_SYS	5V_CON	Dxx_SYS CEC_SYS Pull-ups	DCC_CON Pull-ups	CEC_CON Pull-ups	CEC LDO	LOAD SW & HPD	DCC/CEC VLTs	ICCA Typ	ICC5V Typ	Comments
L	L	1.2V – 5.0V	5.0V	High-Z	Off	Off	Off	Off	Off	Off	1µA	2µA	Fully Disabled
L	H	1.2V – 5.0V	5.0V	5.0V	On	On	Off	Off	On	Off	1µA	30µA	Load Switch on
H	L	1.2V – 5.0V	5.0V	High-Z	Off	Off	Off	Off	Off	Off	1µA	2µA	Not Valid State
H	H	1.2V – 5.0V	5.0V	5.0V	On	On	On	On	On	On	24µA	125µA	Fully On
X	X	0V	0V	High-Z	High-Z	High-Z	High-Z	Off	Off	Off	0	0	Power Down
X	X	1.2V – 5.0V	0V	High-Z	High-Z	High-Z	High-Z	Off	Off	Off	1	0	Power Down
X	X	0V	5.0V	High-Z	High-Z	High-Z	High-Z	Off	Off	Off	0	1	Power Down

9 Applications and Implementations

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

TPD5S116 provides IEC 61000-4-2 Level 4 Contact ESD rating to the HDMI 2.0 transmitter port, with backwards compatibility. Buffered voltage level translators (VLT) translate DDC and CEC channels bidirectionally. The system is designed to work properly with no external pull-up resistors on the DDC, CEC, and HPD lines. The CEC line has an integrated 3.3-V rail, eliminating the need for a 3.3-V supply on board.

9.2 Typical Application

The TPD5S116 is placed as close as possible to the HDMI connector to provide voltage level translation, 5V_OUT current limiting and overall ESD protection for the HDMI Controller.

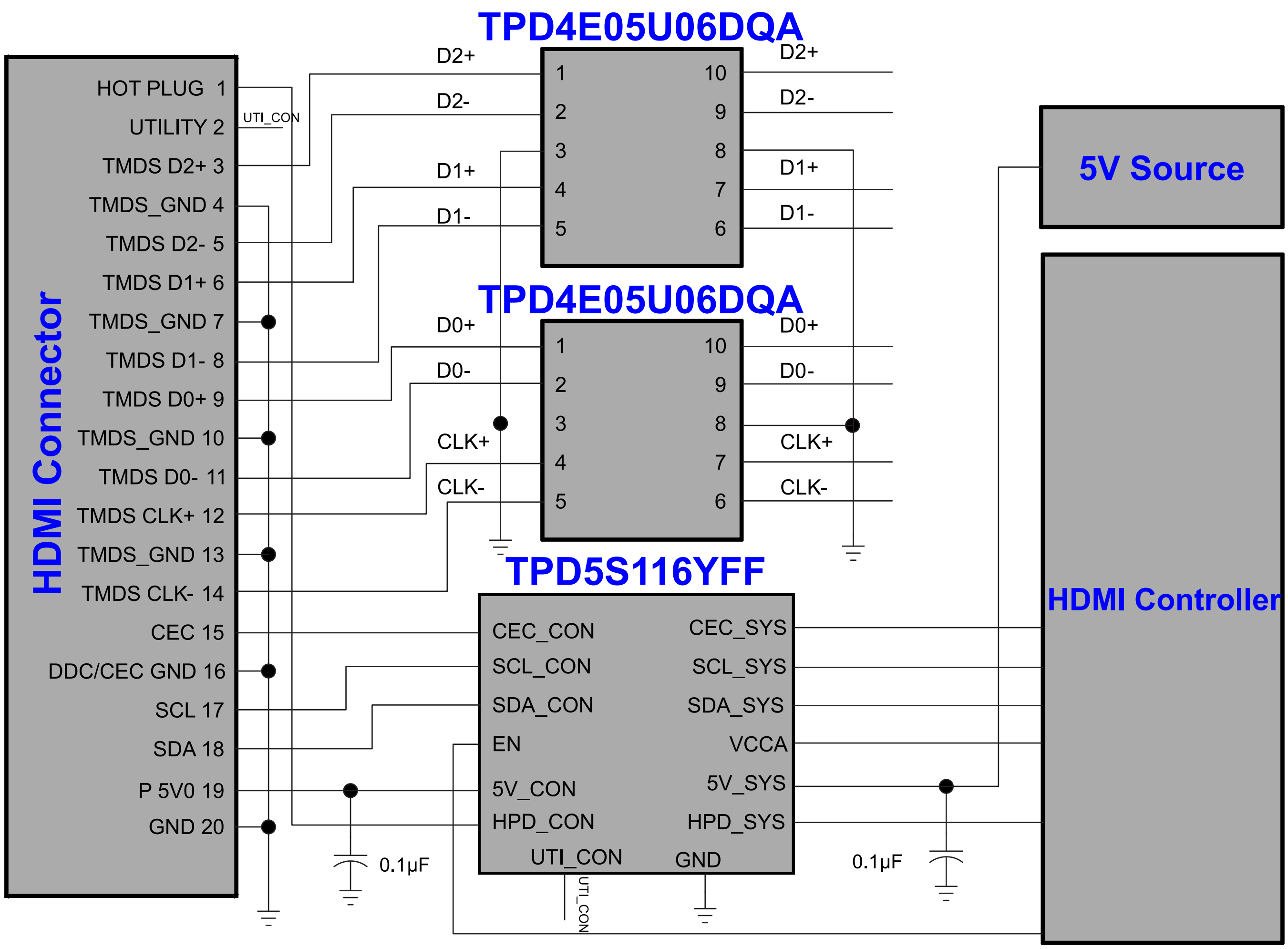


Figure 19. Application Schematics For HDMI Controllers With One GPIO For HDMI Interface Control

Typical Application (continued)

9.2.1 Design Requirements

For this example, use Table 2 as the input parameters:

Table 2. HDMI Controller Using One Control Line Design Parameters

<table>
<tr><th colspan="3">DESIGN PARAMETERS</th><th>EXAMPLE VALUE</th></tr>
<tr><td colspan="3">Voltage on V_{CCA}</td><td>1.8 V</td></tr>
<tr><td colspan="3">Voltage on 5V_SYS</td><td>5.0 V</td></tr>
<tr><td colspan="3">Drive EN low (disabled)</td><td>-0.5 – 0.4 V</td></tr>
<tr><td colspan="3">Drive EN low (enabled)</td><td>1.0 V to 1.8 V</td></tr>
<tr><td colspan="3">Drive HPD_CON low (disabled)</td><td>0 V – 0.8 V</td></tr>
<tr><td colspan="3">Drive HPD_CON high (enabled)</td><td>2.0 V – 5.0 V</td></tr>
<tr><td rowspan="4">Drive a logical "1"</td><td rowspan="2">SYS to CON</td><td>SCL and SDA</td><td rowspan="2">1.26 V – 1.8 V</td></tr>
<tr><td>CEC</td></tr>
<tr><td rowspan="2">CON to SYS</td><td>SCL and SDA</td><td>3.5 V – 5.0 V</td></tr>
<tr><td>CEC</td><td>2.31 V – 3.3 V</td></tr>
<tr><td rowspan="4">Drive a logical "0"</td><td rowspan="2">SYS to CON</td><td>SCL and SDA</td><td rowspan="2">-0.5 V – 0.11 V</td></tr>
<tr><td>CEC</td></tr>
<tr><td rowspan="2">CON to SYS</td><td>SCL and SDA</td><td>-0.5 V – 1.5 V</td></tr>
<tr><td>CEC</td><td>-0.5 V – 0.99 V</td></tr>
</table>

9.2.2 Detailed Design Procedure

To begin the design process the designer needs to know the 5V_SYS voltage range and the logic level, V_{CCA}, voltage range.

9.2.2.1 Resistor Pull-Up Value Selection

The system is designed to work properly with no external pull-up resistors on the DDC, CEC, and HPD lines.

9.2.2.2 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between 5V_SYS and GND. A 10-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

9.2.2.3 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_{LOAD} is highly recommended. A C_{LOAD} greater than C_{IN} can cause 5V_CON to exceed 5V_SYS when the system supply is removed. A C_{IN} to C_{LOAD} ratio of 10 to 1 is recommended for minimizing 5V_SYS dip caused by inrush currents during startup.

9.2.3 Application Curve

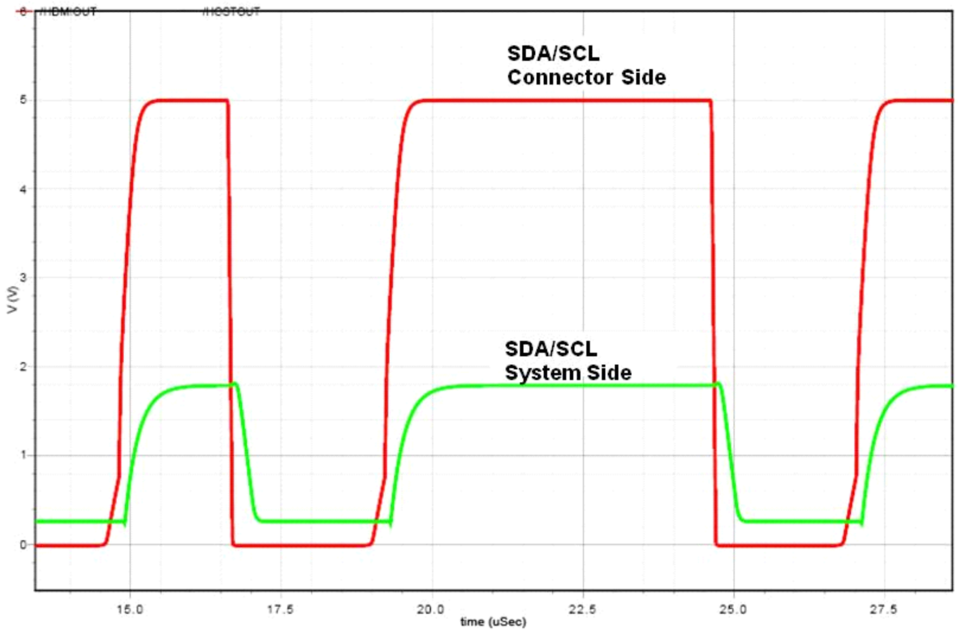


Figure 20. DDC Level Shifter Operation (Connector To System Direction)

10 Power Supply Requirements

TPD5S116 has two power input pins: 5V_SYS and V_{CCA}. It can operate normally with 5V_SYS between 4.5 V and 5.5 V; and V_{CCA} between 1.1 V and 5.5 V. Thus, the power supply (with a ripple of V_{RIPPLE}) requirement for TPD5S116 for 5V_SYS is between 4.5 V + ½V_{RIPPLE} and 5.5 V – ½V_{RIPPLE}; and for V_{CCA} it is between 1.1 V + ½V_{RIPPLE} and 5.5 V – ½V_{RIPPLE}.

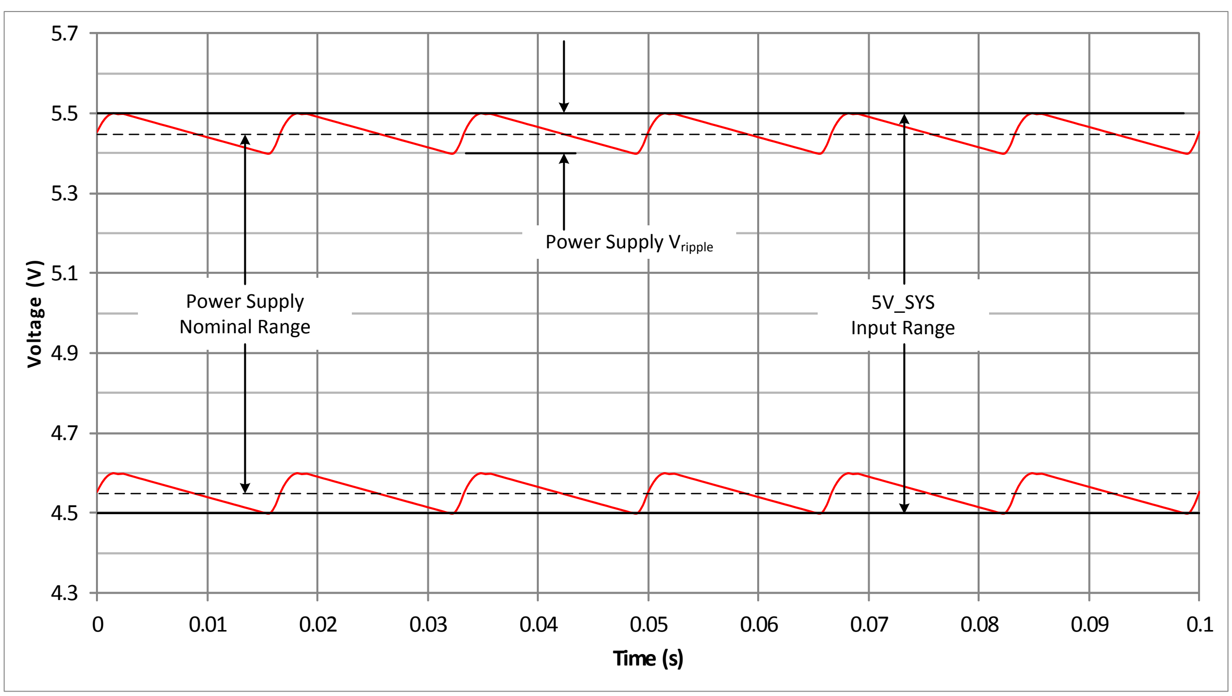


Figure 21. Power Supply Ripple and TPD5S116 5V_SYS Voltage Requirements

11 Layout

11.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. Therefore, the PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Avoid using VIAs between the connecter and an I/O protection pin on TPD5S116.
- Avoid 90º turns in traces.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- Minimize impedance on the path to GND for maximum ESD dissipation.
- The capacitors on 5V_CON and 5V_SYS should be placed close to their respective pins on TPD5S116.

11.2 Layout Example

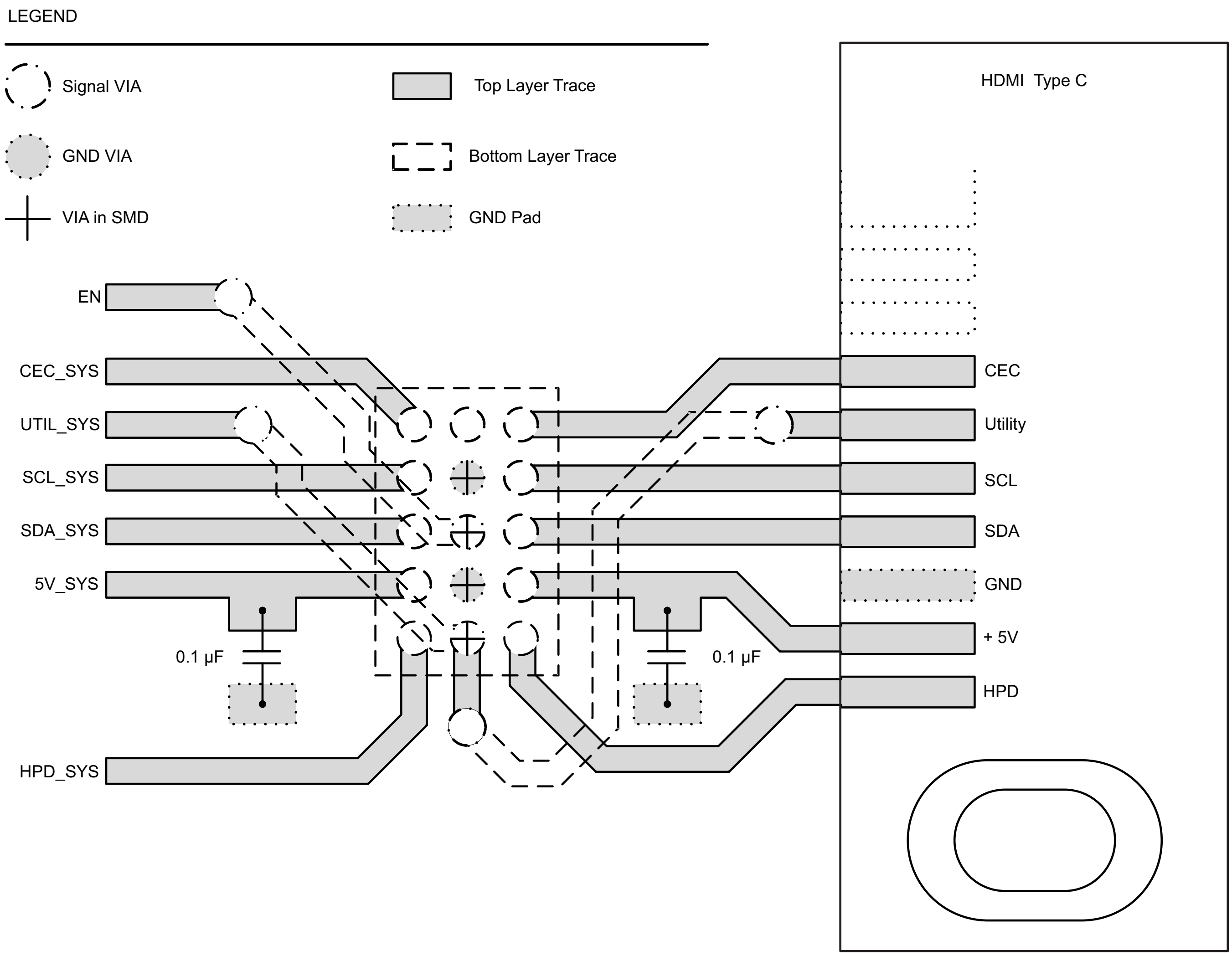


Figure 22. TPD5S116 HDMI Layout Example

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD5S116YFFR	ACTIVE	DSBGA	YFF	15	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RE116	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

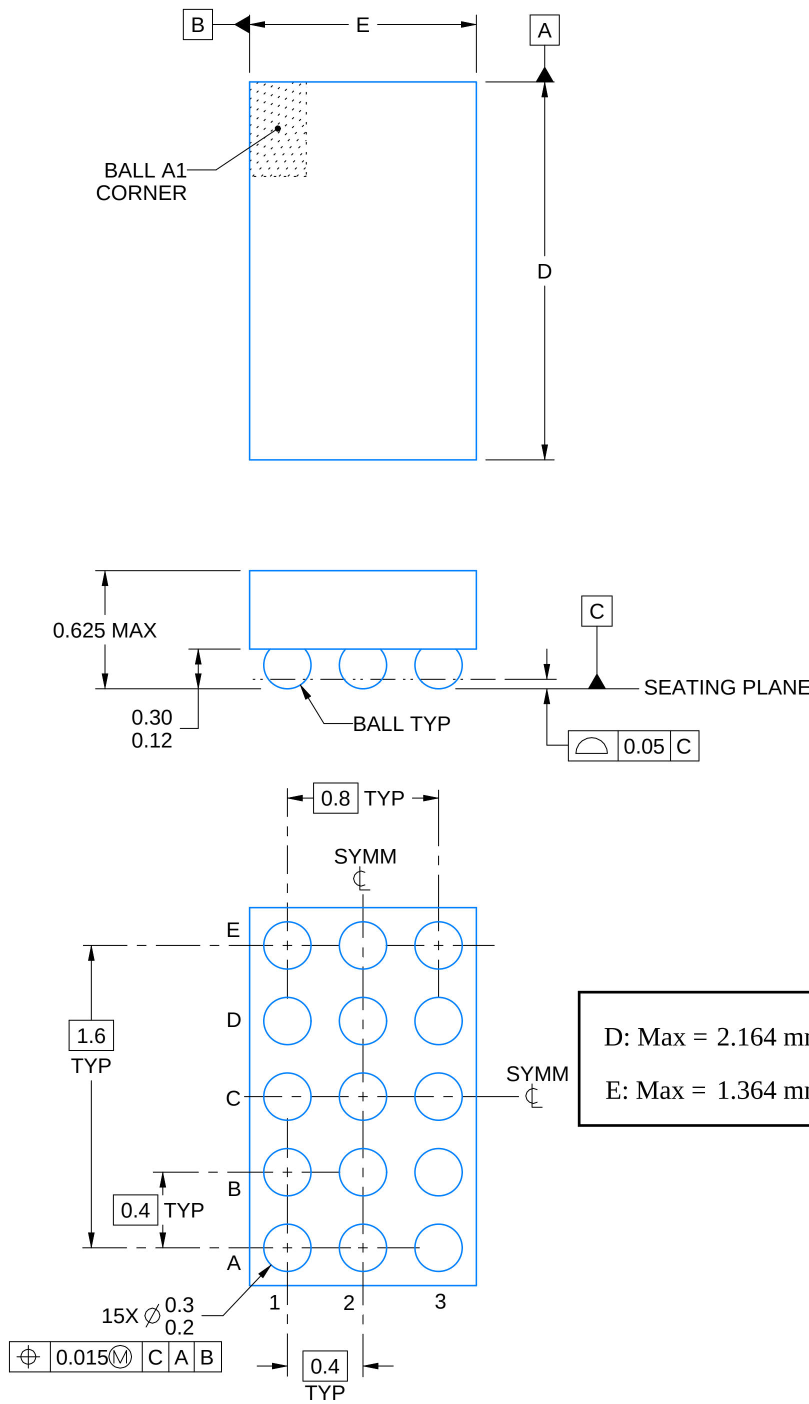
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



D: Max = 2.164 mm, Min =2.104 mm	
E: Max = 1.364 mm, Min =1.304 mm	

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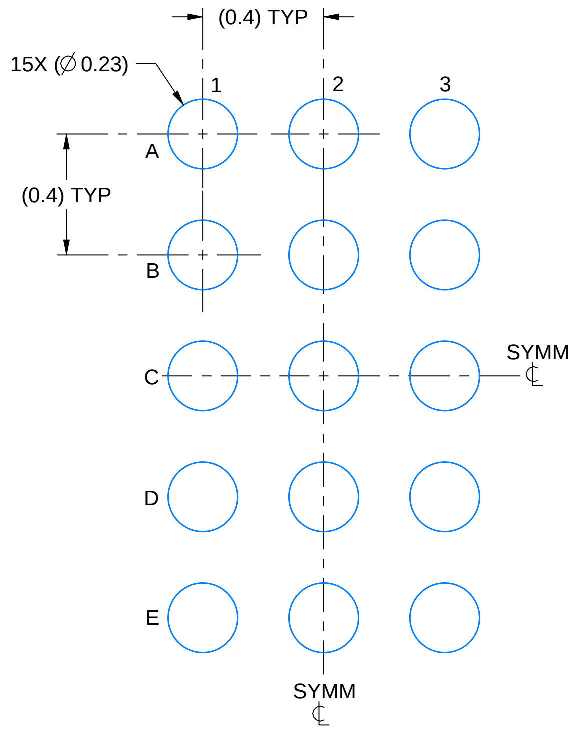
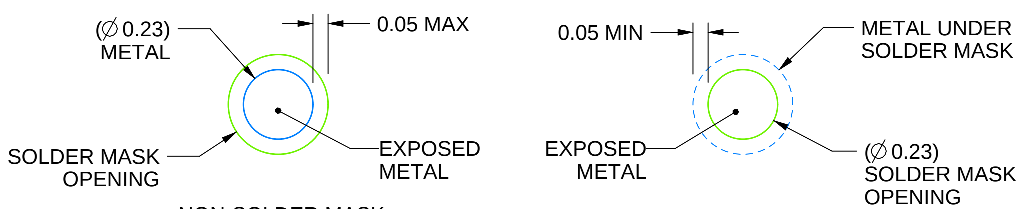
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



NON-SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

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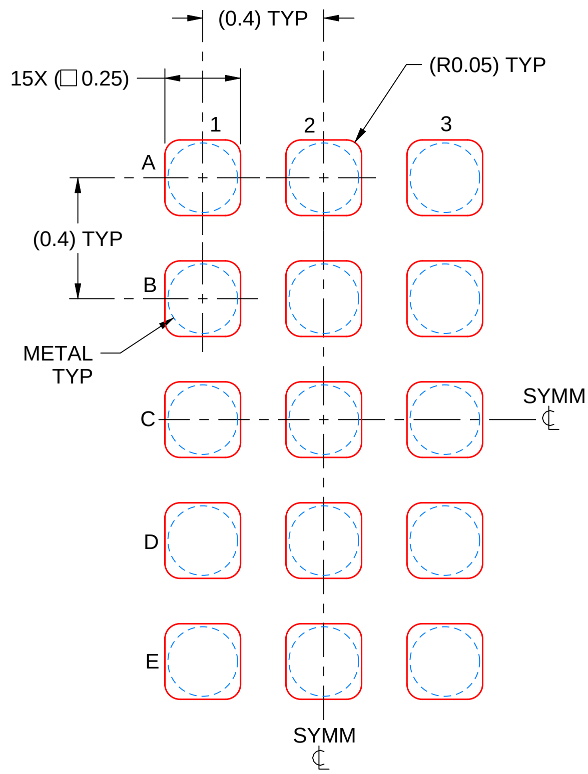
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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