



SBOS141C – JANUARY 1984 – REVISED SEPTEMBER 2009

# PRECISION VOLTAGE-TO-CURRENT CONVERTER/TRANSMITTER

## FEATURES

- 4mA TO 20mA TRANSMITTER
- SELECTABLE INPUT/OUTPUT RANGES:  
0V to +5V, 0V to +10V Inputs  
0mA to 20mA, 5mA to 25mA Outputs  
Other Ranges
- 0.005% MAX NONLINEARITY, 14 BIT
- PRECISION +10V REFERENCE OUTPUT
- SINGLE-SUPPLY OPERATION
- WIDE SUPPLY RANGE: 13.5V to 40V

## DESCRIPTION

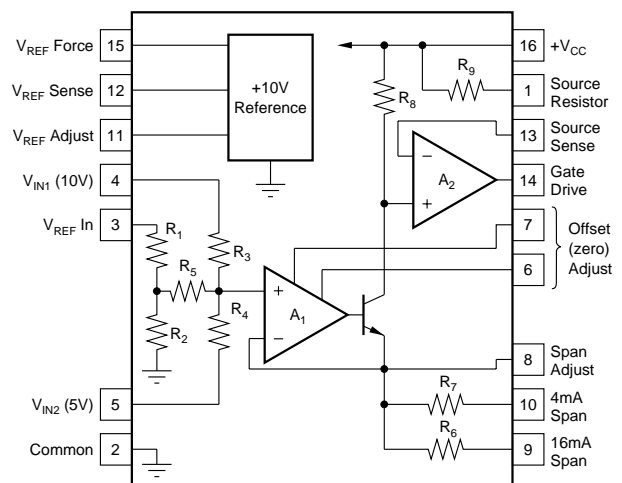
The XTR110 is a precision voltage-to-current converter designed for analog signal transmission. It accepts inputs of 0 to 5V or 0 to 10V and can be connected for outputs of 4mA to 20mA, 0mA to 20mA, 5mA to 25mA, and many other commonly used ranges.

A precision on-chip metal film resistor network provides input scaling and current offsetting. An internal 10V voltage reference can be used to drive external circuitry.

The XTR110 is available in 16-pin plastic DIP, ceramic DIP and SOL-16 surface-mount packages. Commercial and industrial temperature range models are available.

## APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- PRESSURE/TEMPERATURE TRANSMITTERS
- CURRENT-MODE BRIDGE EXCITATION
- GROUNDING TRANSDUCER CIRCUITS
- CURRENT SOURCE REFERENCE FOR DATA ACQUISITION
- PROGRAMMABLE CURRENT SOURCE FOR TEST EQUIPMENT
- POWER PLANT/ENERGY SYSTEM MONITORING



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Power Supply, $+V_{CC}$ .....	40V
Input Voltage, $V_{IN1}$ , $V_{IN2}$ , $V_{REF IN}$ .....	$+V_{CC}$
See text regarding safe negative input voltage range.	
Storage Temperature Range: A, B .....	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
K, U .....	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
Output Short-Circuit Duration, Gate Drive and $V_{REF}$ Force .....	Continuous to common and $+V_{CC}$
Output Current Using Internal $50\Omega$ Resistor .....	40mA

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

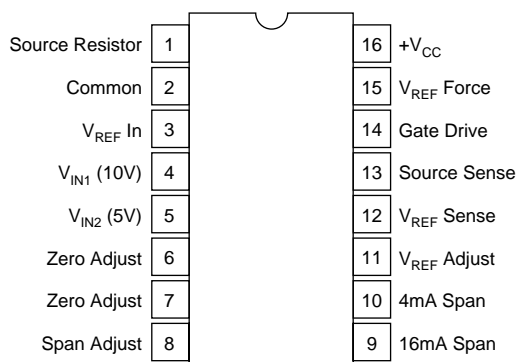
## PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	TEMPERATURE RANGE
XTR110AG	DIP-16 Ceramic	JD	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
XTR110BG	DIP-16 Ceramic	JD	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
XTR110KP	DIP-16 Plastic	N	$0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$
XTR110KU	SOL-16 Surface-Mount	DW	$0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

## PIN CONFIGURATION

### TOP VIEW



# ELECTRICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$  and  $V_{CC} = +24\text{V}$  and  $R_L = 250\Omega^{**}$ , unless otherwise specified.

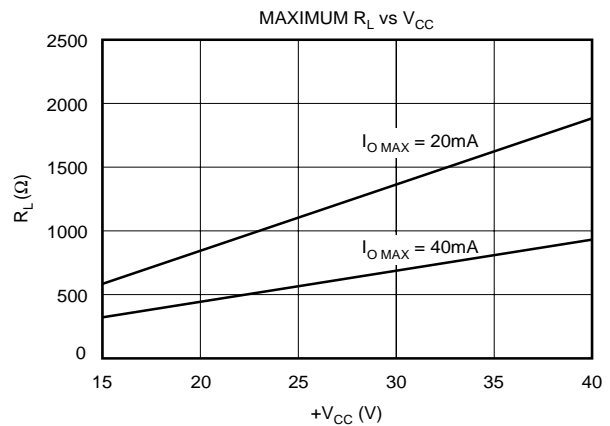
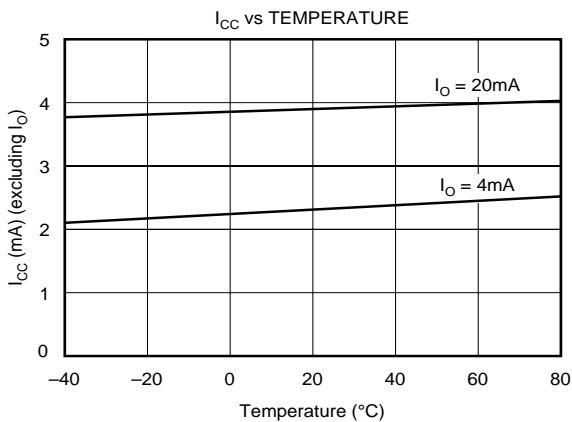
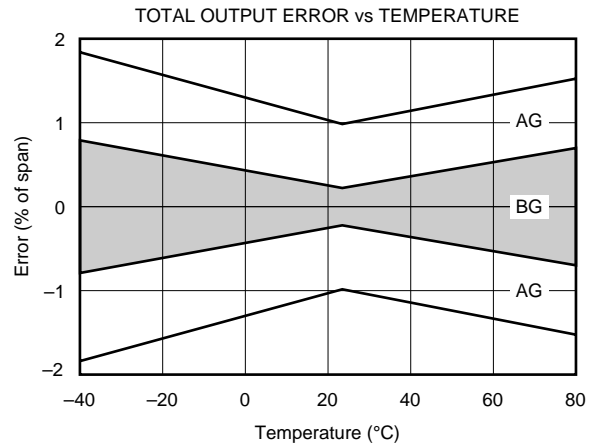
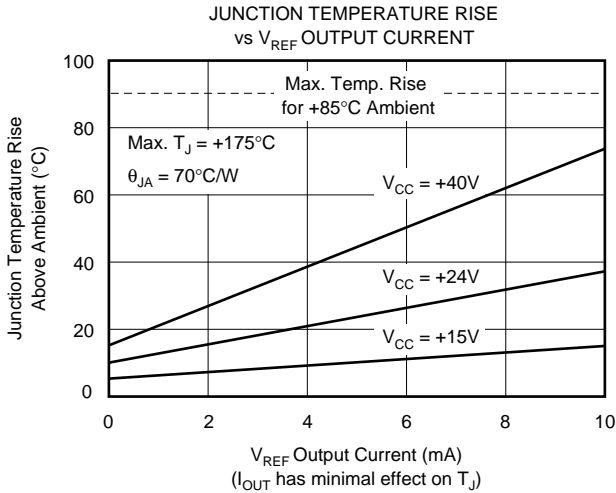
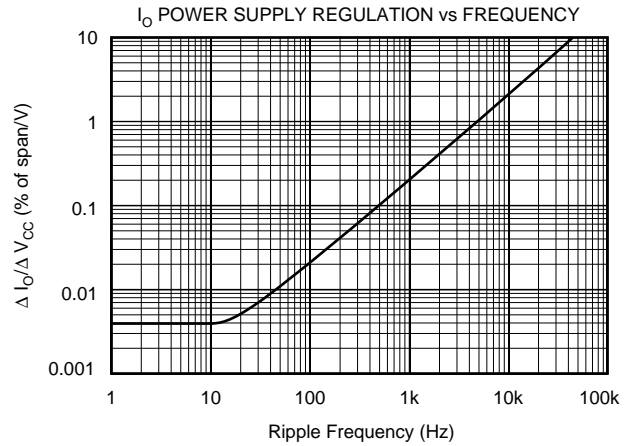
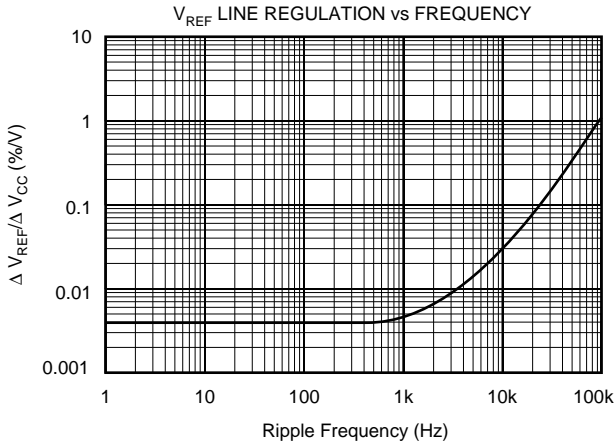
PARAMETER	CONDITIONS	XTR110AG, KP, KU			XTR110BG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>TRANSMITTER</b>								
Transfer Function			$I_O = 10 [(V_{REF}/16) + (V_{IN1}/4) + (V_{IN2}/2)] / R_{SPAN}$					
Input Range: $V_{IN1}^{(5)}$ $V_{IN2}$	Specified Performance	0		+10	*		*	V
	Specified Performance	0		+5	*		*	V
Current, $I_O$	Specified Performance <sup>(1)</sup>	4		20	*		*	mA
	Derated Performance <sup>(1)</sup>	0		40	*		*	mA
Nonlinearity	16mA/20mA Span <sup>(2)</sup>		0.01	0.025		0.002	0.005	% of Span
Offset Current, $I_{OS}$	$I_O = 4\text{mA}^{(1)}$							
Initial	(1)		0.2	0.4		0.02	0.1	% of Span
vs Temperature	(1)		0.0003	0.005		*	0.003	% of Span/ $^\circ\text{C}$
vs Supply, $V_{CC}$	(1)		0.0005	0.005		*	*	% of Span/V
Span Error	$I_O = 20\text{mA}$							
Initial	(1)		0.3	0.6		0.05	0.2	% of Span
vs Temperature	(1)		0.0025	0.005		0.0009	0.003	% of Span/ $^\circ\text{C}$
vs Supply, $V_{CC}$	(1)		0.003	0.005		*	*	% of Span/V
Output Resistance	From Drain of FET ( $Q_{EXT}$ ) <sup>(3)</sup>		$10 \times 10^9$			*	*	$\Omega$
Input Resistance	$V_{IN1}$		27			*	*	k $\Omega$
	$V_{IN2}$		22			*	*	k $\Omega$
	$V_{REF}$ In		19			*	*	k $\Omega$
Dynamic Response								
Settling Time	To 0.1% of Span		15			*	*	$\mu\text{s}$
	To 0.01% of Span		20			*	*	$\mu\text{s}$
Slew Rate			1.3			*	*	mA/ $\mu\text{s}$
<b>VOLTAGE REFERENCE</b>								
Output Voltage		+9.95	+10	+10.05	+9.98	*	+10.02	V
vs Temperature			35	50		15	30	ppm/ $^\circ\text{C}$
vs Supply, $V_{CC}$	Line Regulation		0.0002	0.005		*	*	%/V
vs Output Current	Load Regulation		0.0005	0.01		*	*	%/mA
vs Time			100			*	*	ppm/1k hrs
Trim Range		-0.100		+0.25	*		*	V
Output Current	Specified Performance	10			*		*	mA
<b>POWER SUPPLY</b>								
Input Voltage, $V_{CC}$		+13.5		+40	*		*	V
Quiescent Current	Excluding $I_O$		3	4.5		*	*	mA
<b>TEMPERATURE RANGE</b>								
Specification: AG, BG		-40		+85	*		*	$^\circ\text{C}$
	KP, KU	0		+70				$^\circ\text{C}$
Operating: AG, BG		-55		+125	*		*	$^\circ\text{C}$
	KP, KU	-25		+85				$^\circ\text{C}$

\* Specifications same as AG/KP grades. \*\* Specifications apply to the range of  $R_L$  shown in Typical Performance Curves.

NOTES: (1) Including internal reference. (2) Span is the change in output current resulting from a full-scale change in input voltage. (3) Within compliance range limited by  $(+V_{CC} - 2V) + V_{DS}$  required for linear operation of the FET. (4) For  $V_{REF}$  adjustment circuit see Figure 3. (5) For extended  $I_{REF}$  drive circuit see Figure 4. (5) Unit may be damaged. See *Input Voltage Range* section.

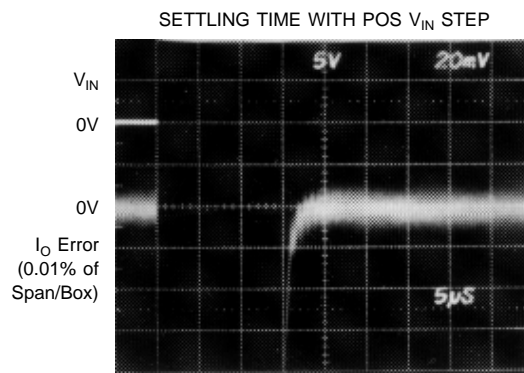
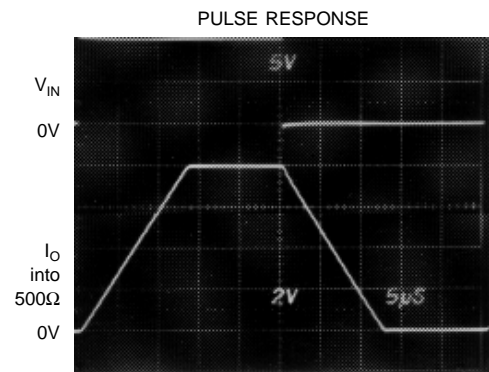
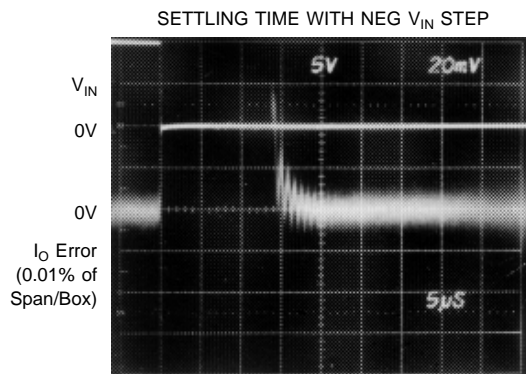
# TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$ ,  $V_{CC} = 24\text{VDC}$ ,  $R_L = 250\Omega$ , unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (Continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = 24\text{VDC}$ ,  $R_L = 250\Omega$ , unless otherwise noted.



# APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for 0V to 10V input and 4mA to 20mA output. Other input voltage and output current ranges require changes in connections of pins 3, 4, 5, 9 and 10 as shown in the table of Figure 1.

The complete transfer function of the XTR110 is:

$$I_O = \frac{10 \left[ \frac{(V_{REF IN})}{16} + \frac{(V_{IN1})}{4} + \frac{(V_{IN2})}{2} \right]}{R_{SPAN}} \quad (1)$$

$R_{SPAN}$  is the total impedance seen at the emitter of the internal NPN transistor. This impedance varies depending on how pins 8, 9 and 10 are configured. Typical operating region configurations are shown in Figure 1. An external  $R_{SPAN}$  can be connected for different output current ranges as described later.

## EXTERNAL TRANSISTOR

An external pass transistor,  $Q_{EXT}$ , is required as shown in Figure 1. This transistor conducts the output signal current. A P-channel MOSFET transistor is recommended. It must

have a voltage rating equal or greater than the maximum power supply voltage. Various recommended types are shown in Table I.

MANUFACTURER	PART NO.	BV <sub>DSS</sub> <sup>(1)</sup>	BV <sub>GS</sub> <sup>(1)</sup>	PACKAGE
Ferranti	ZVP1304A	40V	20V	TO-92
	ZVP1304B	40V	20V	TO-39
	ZVP1306A	60V	20V	TO-92
	ZVP1306B	60V	20V	TO-39
International Rectifier	IRF9513	60V	20V	TO-220
Motorola	MTP8P08	80V	20V	TO-220
RCA	RFL1P08	80V	20V	TO-39
	RFT2P08	80V	20V	TO-220
Siliconix (preferred)	VP0300B	30V	40V	TO-39
	VP0300L	30V	40V	TO-92
	VP0300M	30V	40V	TO-237
	VP0808B	80V	40V	TO-39
	VP0808L	80V	40V	TO-92
	VP0808M	80V	40V	TO-237
Supertex	VP1304N2	40V	20V	TO-220
	VP1304N3	40V	20V	TO-92
	VP1306N2	60V	20V	TO-220
	VP1306N3	60V	20V	TO-92

NOTE: (1) BV<sub>DSS</sub>—Drain-source breakdown voltage. BV<sub>GS</sub>—Gate-source breakdown voltage.

TABLE I. Available P-Channel MOSFETs.

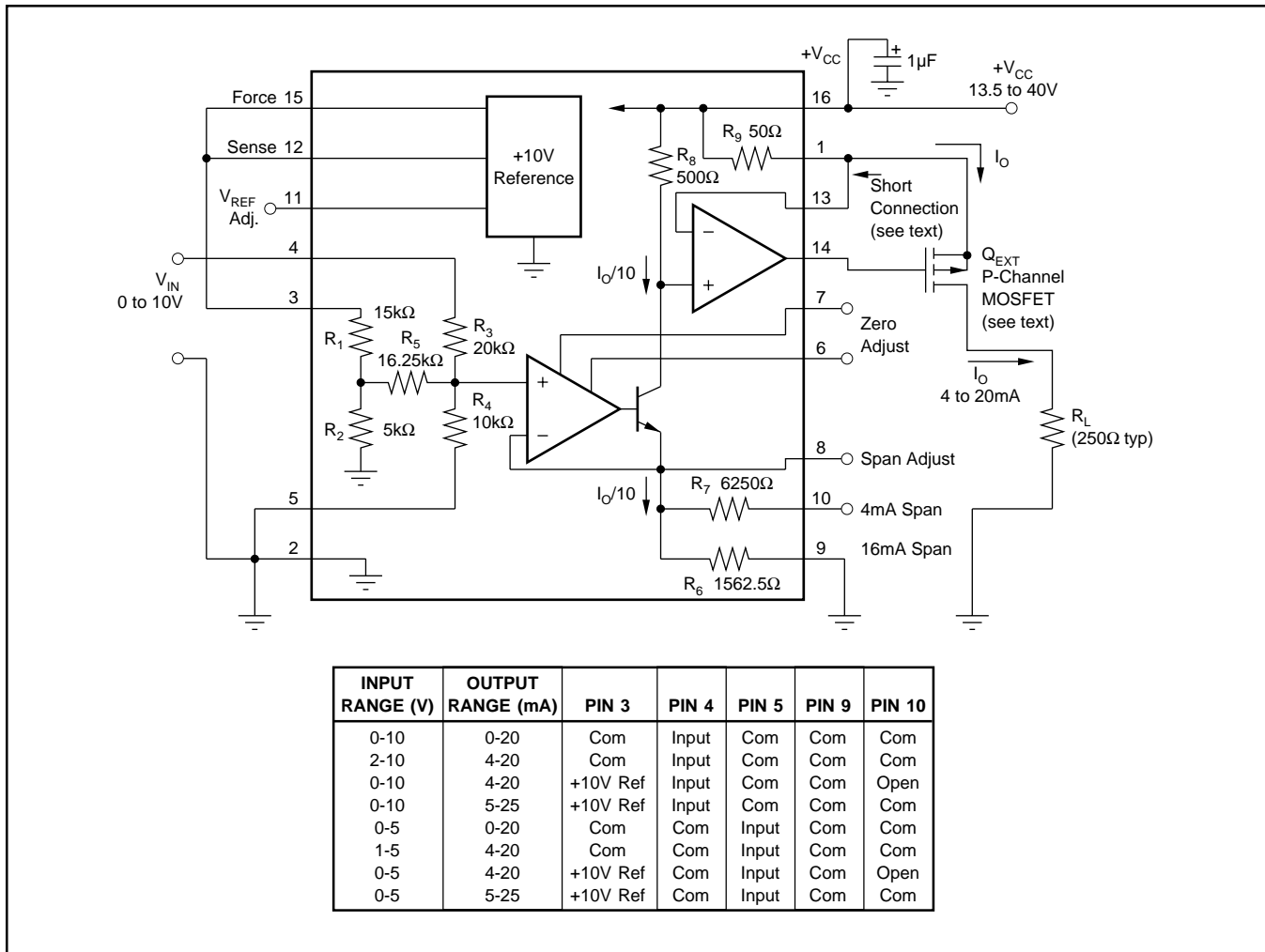


FIGURE 1. Basic Circuit Connection.

If the supply voltage,  $+V_{CC}$ , exceeds the gate-to-source breakdown voltage of  $Q_{EXT}$ , and the output connection (drain of  $Q_{EXT}$ ) is broken,  $Q_{EXT}$  could fail. If the gate-to-source breakdown voltage is lower than  $+V_{CC}$ ,  $Q_{EXT}$  can be protected with a 12V zener diode connected from gate to source.

Two PNP discrete transistors (Darlington-connected) can be used for  $Q_{EXT}$ —see Figure 2. Note that an additional capacitor is required for stability. Integrated Darlington transistors are not recommended because their internal base-emitter resistors cause excessive error.

## TRANSISTOR DISSIPATION

Maximum power dissipation of  $Q_{EXT}$  depends on the power supply voltage and full-scale output current. Assuming that the load resistance is low, the power dissipated by  $Q_{EXT}$  is:

$$P_{MAX} = (+V_{CC}) I_{FS} \quad (2)$$

The transistor type and heat sinking must be chosen according to the maximum power dissipation to prevent overheating. See Table II for general recommendations.

PACKAGE TYPE	ALLOWABLE POWER DISSIPATION
TO-92	Lowest: Use minimum supply and at +25°C.
TO-237	Acceptable: Trade-off supply and temperature.
TO-39	Good: Adequate for majority of designs.
TO-220	Excellent: For prolonged maximum stress.
TO-3	Use if hermetic package is required.

TABLE II. External Transistor Package Type and Dissipation.

## INPUT VOLTAGE RANGE

The internal op amp  $A_1$  can be damaged if its non-inverting input (an internal node) is pulled more than 0.5V below common (0V). This could occur if input pins 3, 4 or 5 were driven with an op amp whose output could swing negative under abnormal conditions. The voltage at the input of  $A_1$  is:

$$V_{A1} = \frac{(V_{REF IN})}{16} + \frac{(V_{IN1})}{4} + \frac{(V_{IN2})}{2} \quad (3)$$

This voltage should not be allowed to go more negative than  $-0.5V$ . If necessary, a clamp diode can be connected from the negative-going input to common to clamp the input voltage.

## COMMON (Ground)

Careful attention should be directed toward proper connection of the common (grounds). All commons should be joined at one point as close to pin 2 of the XTR110 as possible. The exception is the  $I_{OUT}$  return. It can be returned to any point where it will not modulate the common at pin 2.

## VOLTAGE REFERENCE

The reference voltage is accurately regulated at pin 12 ( $V_{REF SENSE}$ ). To preserve accuracy, any load including pin

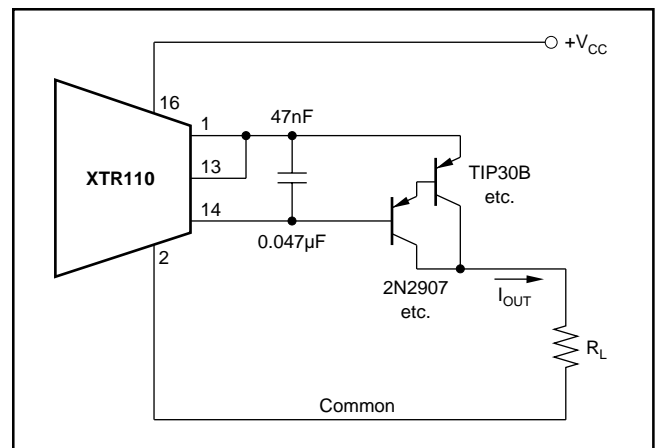


FIGURE 2.  $Q_{EXT}$  Using PNP Transistors.

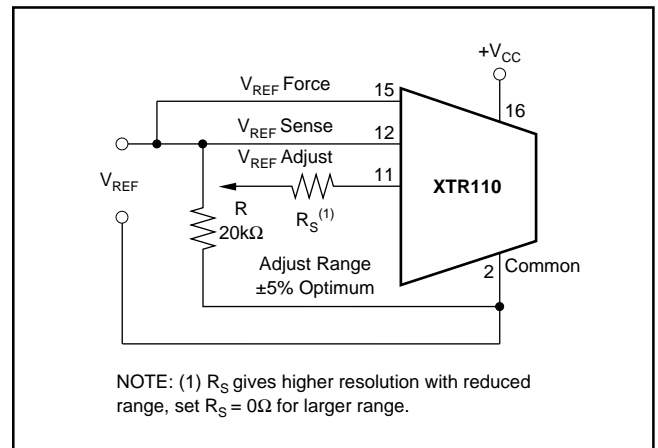


FIGURE 3. Optional Adjustment of Reference Voltage.

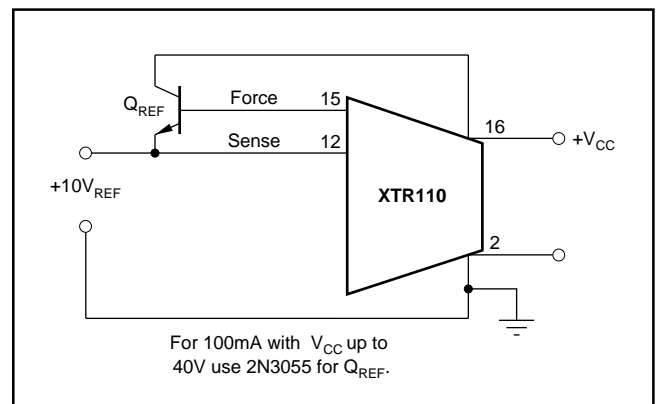


FIGURE 4. Increasing Reference Current Drive.

3 should be connected to this point. The circuit in Figure 3 shows adjustment of the voltage reference.

The current drive capability of the XTR110's internal reference is 10mA. This can be extended if desired by adding an external NPN transistor shown in Figure 4.

## OFFSET (ZERO) ADJUSTMENT

The offset current can be adjusted by using the potentiometer,  $R_1$ , shown in Figure 5. Set the input voltage to zero and then adjust  $R_1$  to give 4mA at the output. For spans starting

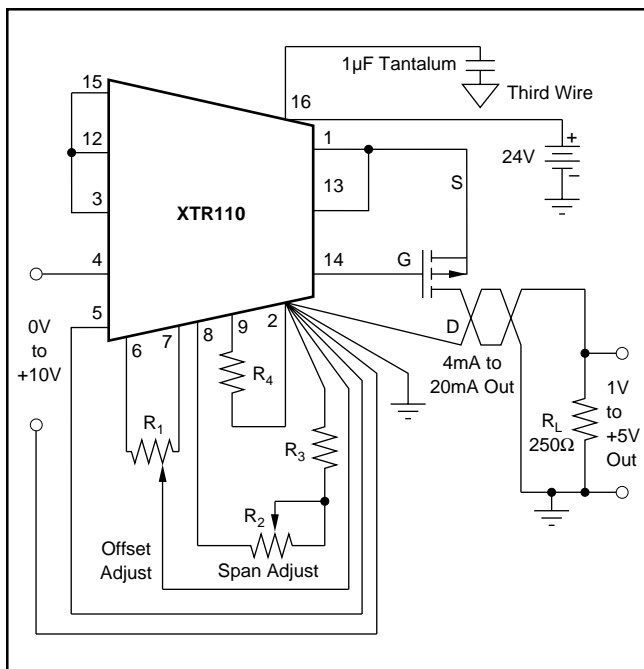


FIGURE 5. Offset and Span Adjustment Circuit for 0V to +10V Input, 4mA to 20mA Output.

at 0mA, the following special procedure is recommended: set the input to a small nonzero value and then adjust  $R_1$  to the proper output current. When the input is zero the output will be zero. Figures 6 and 7 show graphically how offset is adjusted.

### SPAN ADJUSTMENT

The span is adjusted at the full-scale output current using the potentiometer,  $R_2$ , shown in Figure 5. This adjustment is interactive with the offset adjustment, and a few iterations may be necessary. For the circuit shown, set the input voltage to +10V full scale and adjust  $R_2$  to give 20mA full-scale output. Figures 6 and 7 show graphically how span is adjusted.

The values of  $R_2$ ,  $R_3$ , and  $R_4$  for adjusting the span are determined as follows: choose  $R_4$  in series to slightly decrease the span; then choose  $R_2$  and  $R_3$  to increase the span to be adjustable about the center value.

### LOW TEMPERATURE COEFFICIENT OPERATION

Although the precision resistors in the XTR110 track within 1ppm/°C, the output current depends upon the absolute temperature coefficient (TC) of any one of the resistors,  $R_6$ ,  $R_7$ ,  $R_8$ , and  $R_9$ . Since the absolute TC of the output current can have 20ppm/°C, maximum, the TC of the output current can have 20ppm/°C drift. For low TC operation, zero TC resistors can be substituted for either the span resistors ( $R_6$  or  $R_7$ ) or for the source resistor ( $R_9$ ) but not both.

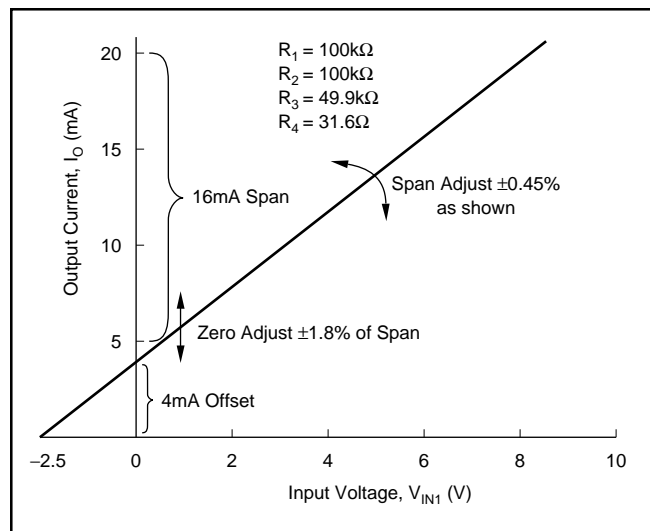


FIGURE 6. Zero and Span of 0V to +10V Input, 4mA to 20mA Output Configuration (see Figure 5).

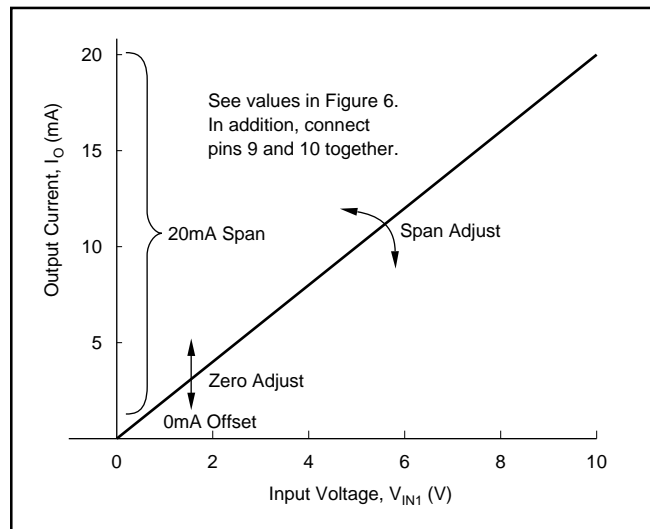


FIGURE 7. Zero and Span of 0V to +10V<sub>IN</sub>, 0mA to 20mA Output Configuration (see Figure 5).

### EXTENDED SPAN

For spans beyond 40mA, the internal 50Ω resistor ( $R_9$ ) may be replaced by an external resistor connected between pins 13 and 16.

Its value can be calculated as follows:

$$R_{EXT} = R_9 (\text{Span}_{OLD} / \text{Span}_{NEW})$$

Since the internal thin-film resistors have a 20% absolute value tolerance, measure  $R_9$  before determining the final value of  $R_{EXT}$ . Self-heating of  $R_{EXT}$  can cause nonlinearity. Therefore, choose one with a low TC and adequate power rating. See Figure 10 for application.



# TYPICAL APPLICATIONS

The XTR110 is ideal for a variety of applications requiring high noise immunity current-mode signal transmission. The precision +10V reference can be used to excite bridges and transducers. Selectable ranges make it very useful as a precision programmable current source. The compact design

and low price of the XTR110 allow versatility with a minimum of external components and design engineering expense.

Figures 8 through 10 show typical applications of the XTR110.

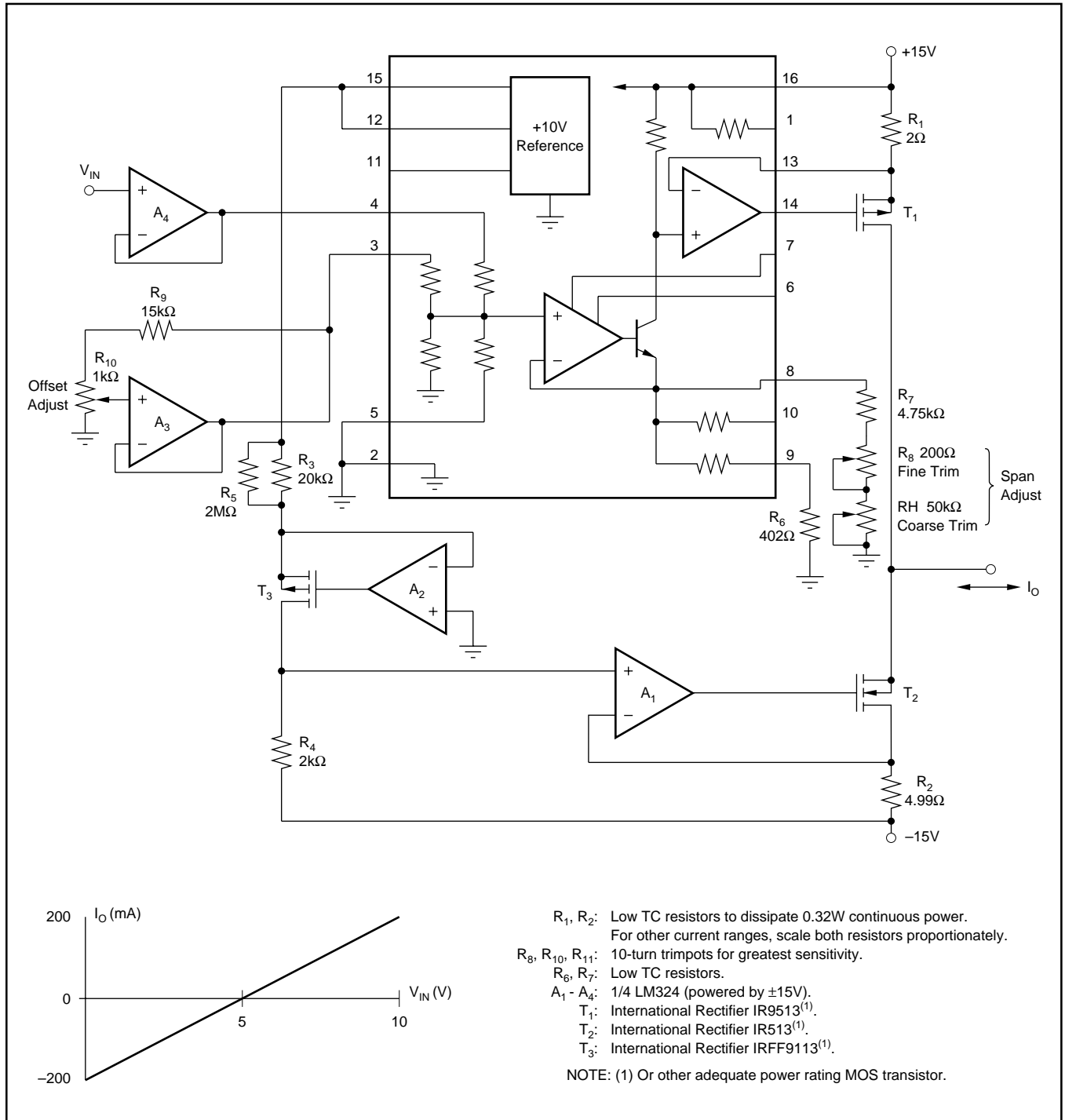


FIGURE 8.  $\pm 200mA$  Current Pump.

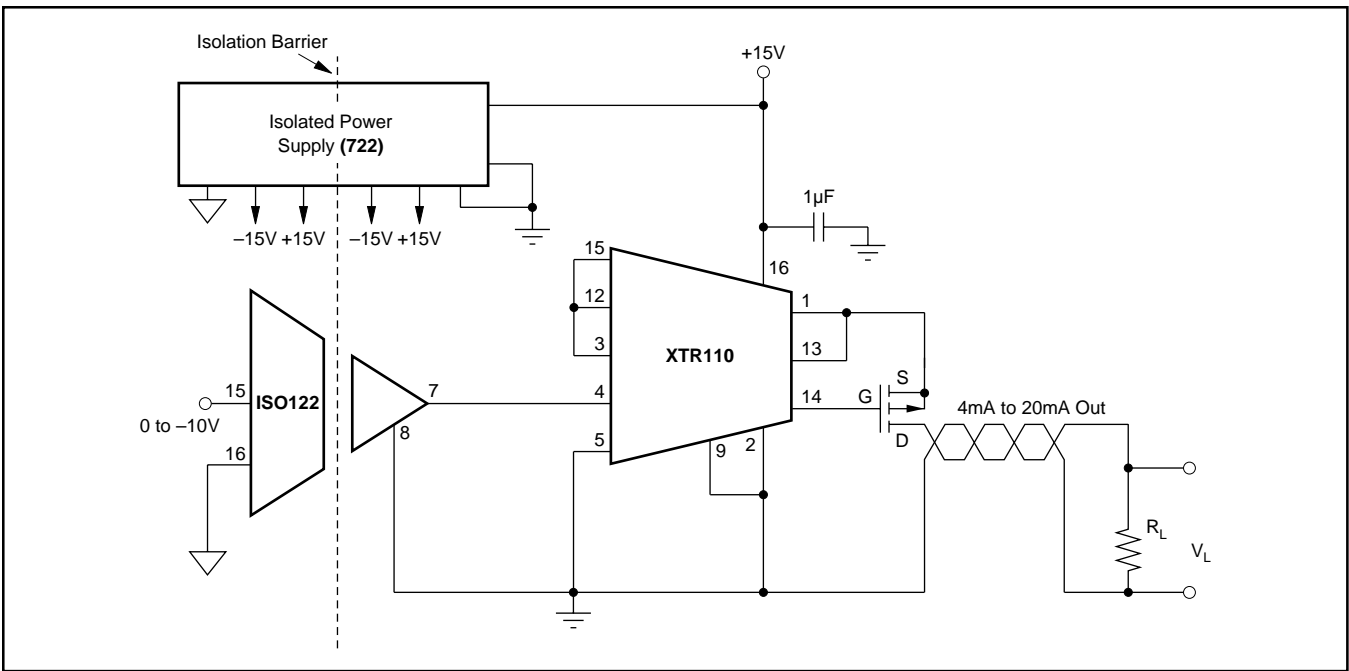


FIGURE 9. Isolated 4mA to 20mA Channel.

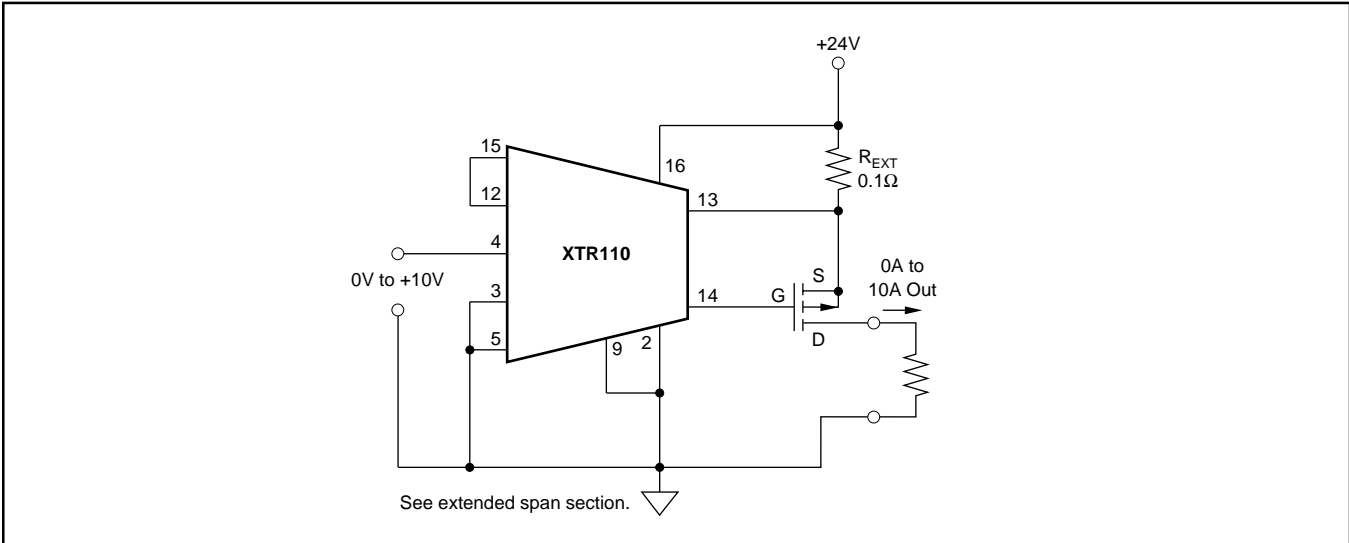


FIGURE 10. 0A to 10A Output Voltage-to-Current Converter.

## Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
9/09	C	6	Front Page	Changed front page to standard format.
			Applications Information	Changed text in third paragraph.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XTR110AG	NRND	CDIP SB	JD	16	1	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		XTR110AG	
XTR110BG	NRND	CDIP SB	JD	16	1	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		XTR110BG	
XTR110KP	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		XTR110KP	Samples
XTR110KPG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		XTR110KP	Samples
XTR110KU	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR110KU	Samples
XTR110KU/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR110KU	Samples
XTR110KU/1KG4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR110KU	Samples
XTR110KUG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		XTR110KU	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTR110KU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTR110KU/1K	SOIC	DW	16	1000	367.0	367.0	38.0

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

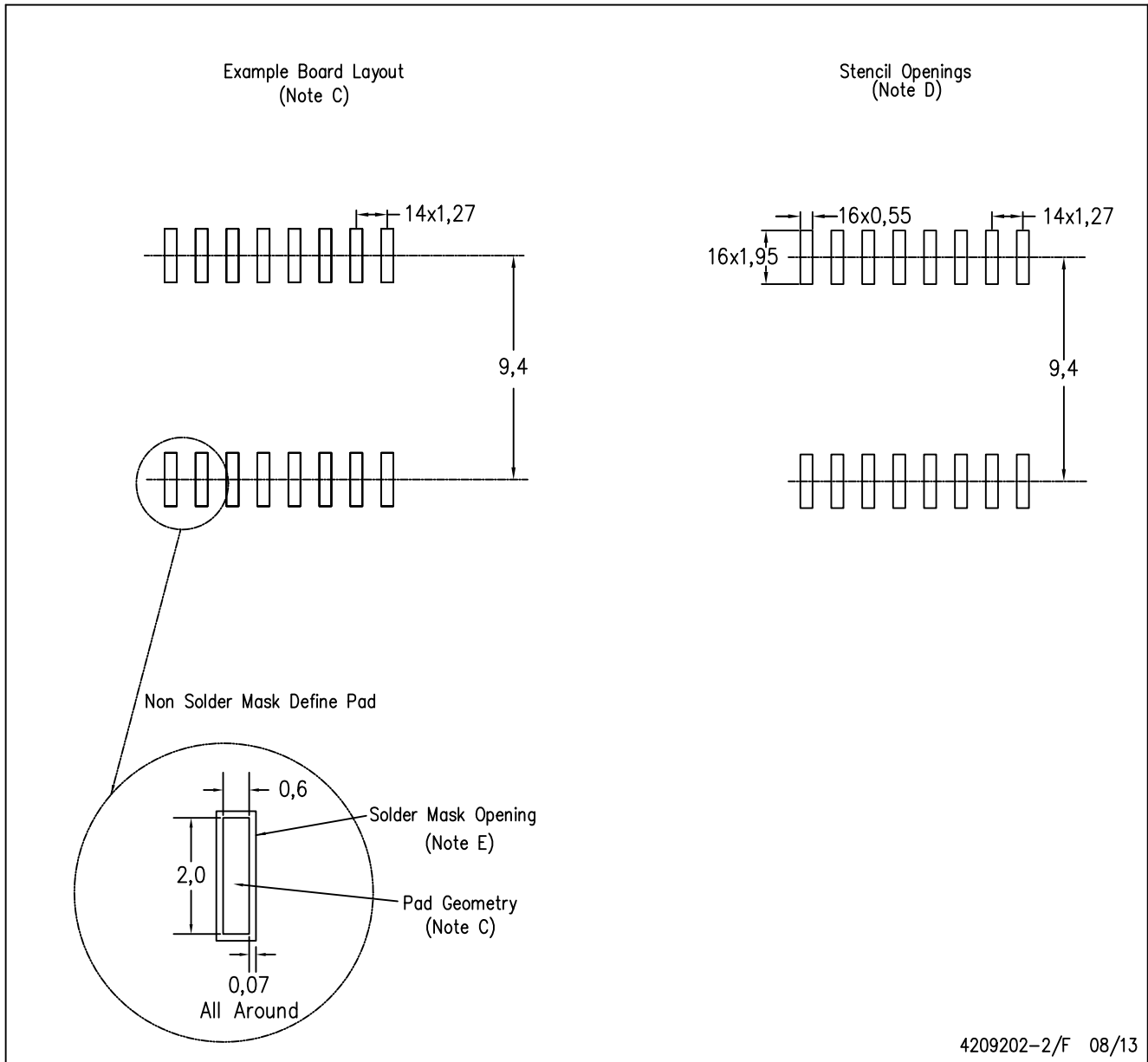


- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AA.



DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



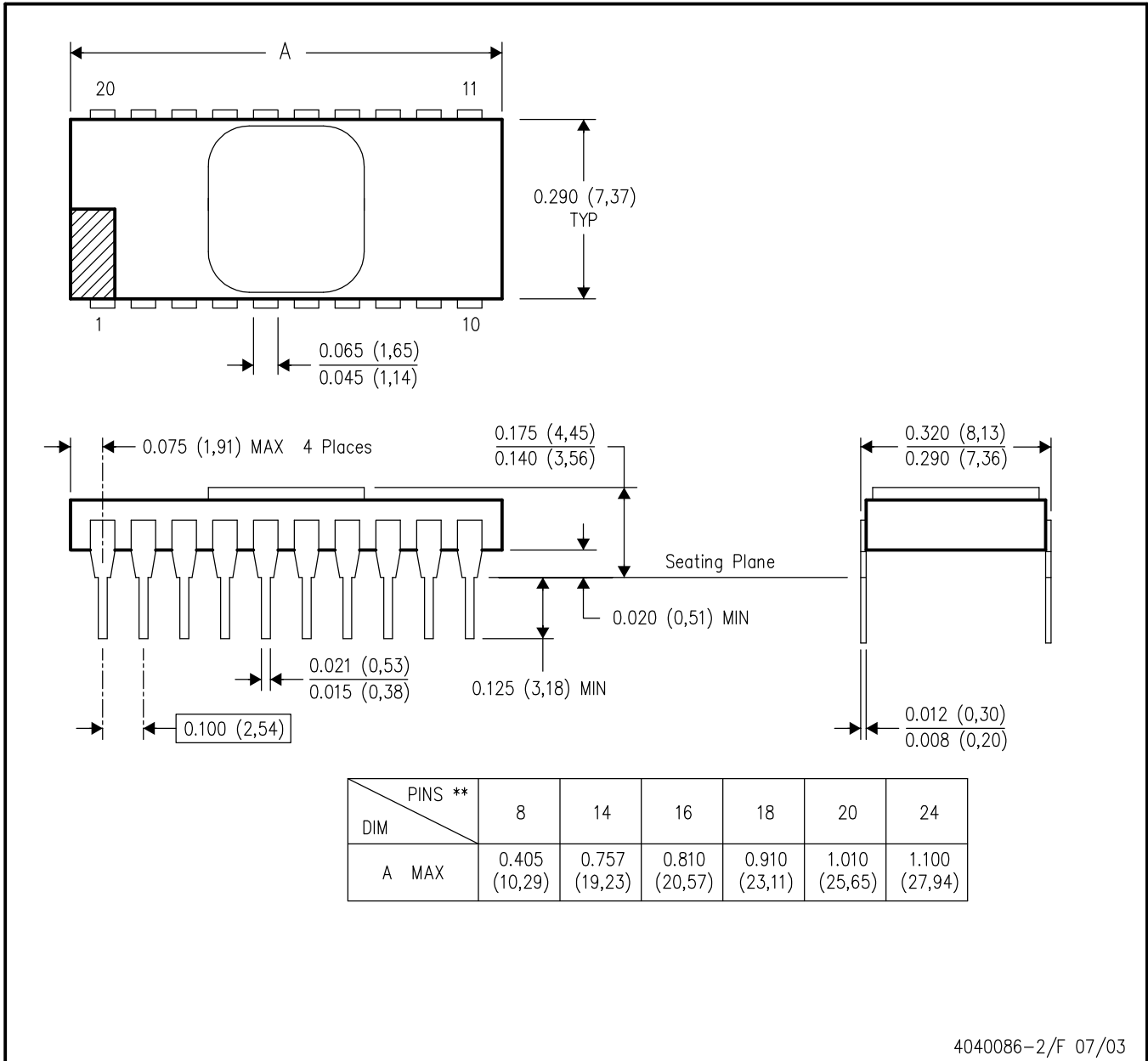
4209202-2/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

JD (R-CDIP-T\*\*)

CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE

20 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within MIL STD 1835 CDIP2 - T8, T14, T16, T18, T20 and T24 respectively.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.