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Dual 2-Input NAND Gate With Schmitt-Trigger Inputs

Check for Samples: SN74LVC2G132

FEATURES

- Available in Texas Instruments NanoFree™ **Package**
- **Supports 5-V V_{CC} Operation**
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 5.3 ns at 3.3 V
- Low Power Consumption, 10-µA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- I_{off} Supports Live Insertion, Partial Power Down Mode, and Back Drive Protection
- Support Translation Down (5V to 3.3V and 3.3V to 1.8V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION

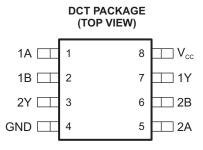
This dual 2-input NAND gate with Schmitt-trigger inputs is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC2G132 contains two inverters and performs the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The device functions as two independent inverters, but because of Schmitt action, it has different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

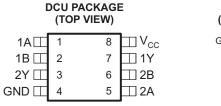
package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.







YZP PACKAGE (BOTTOM VIEW) 0450 0360 2B 1B 0270 1Y 0180

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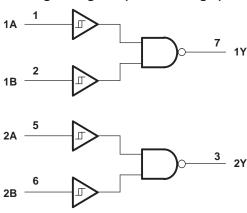


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Function Table (Each Gate)

INP	UTS	OUTPUT
Α	В	Y
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L

Logic Diagram (Positive Logic)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_{I}	Input voltage range ⁽²⁾		-0.5	6.5	V
V_{O}	Voltage range applied to any output in the high	gh-impedance or power-off state (2)	-0.5	6.5	V
Vo	Voltage range applied to any output in the high	gh or low state (2) (3)	-0.5	$V_{CC} + 0.5$	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
		DCT package		220	
θ_{JA}	Package thermal impedance (4)	DCU package		227	°C/W
		YZP package		102	
T _{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- 4) The package thermal impedance is calculated in accordance with JESD 51-7

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Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT	
\ /	Committee	Operating	1.65	5.5	V	
V_{CC}	Supply voltage	Data retention only	1.5		V	
VI	Input voltage		0	5.5	V	
Vo	Output voltage		0	V_{CC}	V	
	$V_{CC} = 1.65 \text{ V}$ $V_{CC} = 2.3 \text{ V}$			-4		
				-8		
I_{OH}	High-level output current	V 0 V		-16	mA	
I _{OH}		V _{CC} = 3 V		-24		
		V _{CC} = 4.5 V		-32		
		V _{CC} = 1.65 V		4		
	riigii-level output current	V _{CC} = 2.3 V		8		
I_{OL}	Low-level output current	V 2V		16	mA	
		V _{CC} = 3 V		24		
		V _{CC} = 4.5 V		32		
T _A	Operating free-air temperature		-40	125	°C	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

BARAMETER	TEGT COMPITIONS	.,	-40°	C to 85°C	-40°C	to 125°C	UNI
PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾ MAX	MIN	TYP ⁽¹⁾ MA	Х
		1.65 V	0.79	1.16	0.79	1.1	6
V_{T+}		2.3 V	1.11	1.56	1.11	1.5	6
Positive-going		3 V	1.5	1.87	1.5	1.8	7 V
input threshold voltage		4.5 V	2.16	2.74	2.16	2.7	4
		5.5 V	2.61	3.33	2.61	3.3	3
		1.65 V	0.39	0.62	0.39	0.6	2
V _T		2.3 V	0.58	0.87	0.58	0.8	7
Negative-going		3 V	0.84	1.14	0.84	1.1	4 V
input threshold voltage		4.5 V	1.41	1.79	1.41	1.7	9
		5.5 V	1.87	2.29	1.87	2.2	9
		1.65 V	0.37	0.62	0.37	0.6	2
ΔV_{T}		2.3 V	0.48	0.77	0.48	0.7	7
Hysteresis		3 V	0.56	0.87	0.56	0.0	7 V
$(V_{T+} - V_{T-})$		4.5 V	0.71	1.04	0.71	1.0	4
		5.5 V	0.71	1.11	0.71	1.1	1
	I _{OH} = -100 μA	1.65 V to 5.5 V	V _{CC} - 0.1		V _{CC} - 0.1		
	I _{OH} = -4 mA	1.65 V 1.2 1.2					
V	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9		1.9		V
V _{OH}	I _{OH} = -16 mA	2.1/	2.4		2.4		v
	I _{OH} = -24 mA	3 V	2.3		2.3		
	$I_{OH} = -32 \text{ mA}$	4.5 V	3.8		3.8		
	$I_{OL} = 100 \mu A$	1.65 V to 5.5 V		0.1		0	1
	I _{OL} = 4 mA	1.65 V		0.45		0.4	5
V	I _{OL} = 8 mA	2.3 V		0.3		0	3 _V
V _{OL}	I _{OL} = 16 mA	3 V		0.4		0	
	I _{OL} = 24 mA	3 V		0.55		0.6	5
	I _{OL} = 32 mA	4.5 V		0.55		0.6	5
I _I A or B inputs	V _I = 5.5 V or GND	1.65 V to 5.5 V		±1		±	1 µA
I _{off}	V _I or V _O = 5.5 V	0		±10		±1	0 µA
I _{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	1.65 V to 5.5 V		10		1	0 μΑ
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V		500		50	0 μΑ
Cı	V _I = V _{CC} or GND	3.3 V		3.5			pF

⁽¹⁾ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

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Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

			SN74LVC2G132 -40°C to 85°C								
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V				V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Υ	4	16	2.5	7	2	5.3	1.5	4.4	ns

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see Figure 2)

							C2G132 to 85°C				
PARAMETER	FROM (INPUT)	TO (OUTPUT)			V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Υ	4	16	3	7.5	2	6	2	5	ns

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see Figure 2)

							C2G132 o 125°C				
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	4	17	3	8.5	2	7	2	6	ns

Operating Characteristics

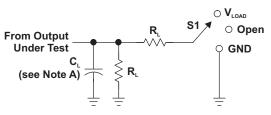
 $T_A = 25$ °C

	PARAMETER	TEST	V _{CC} = 1.8 V	$V_{CC} = 2.5 \text{ V}$	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT	
	FARAMETER	CONDITIONS	TYP	TYP	TYP	TYP	UNII	
C_{pd}	Power dissipation capacitance	f = 10 MHz	17	18	18	20	pF	

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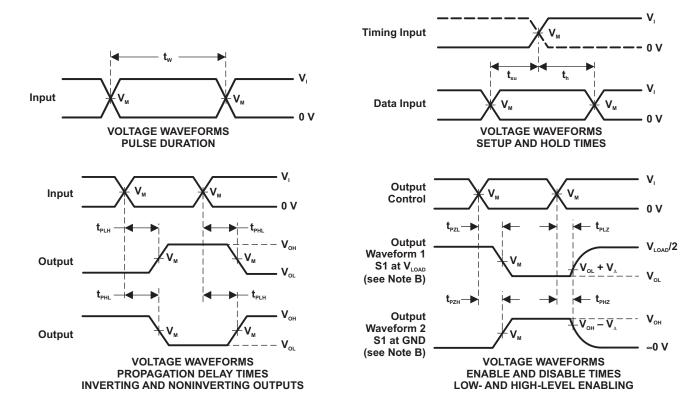
Parameter Measurement Information



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

	.,	INPUTS		.,	.,			.,
	V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C _L	R _⊾	V _A
ſ	$1.8~V~\pm~0.15~V$	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 M Ω	0.15 V
	$2.5~V~\pm~0.2~V$	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 M Ω	0.15 V
	3.3 V \pm 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 M Ω	0.3 V
	5 V \pm 0.5 V	V _{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 M Ω	0.3 V



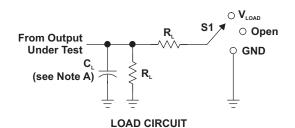
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_o = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{\mbox{\tiny PLZ}}$ and $\dot{t}_{\mbox{\tiny PHZ}}$ are the same as $t_{\mbox{\tiny dis}}.$
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. $t_{\mbox{\tiny PLH}}$ and $t_{\mbox{\tiny PHL}}$ are the same as $t_{\mbox{\tiny pd}}.$
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

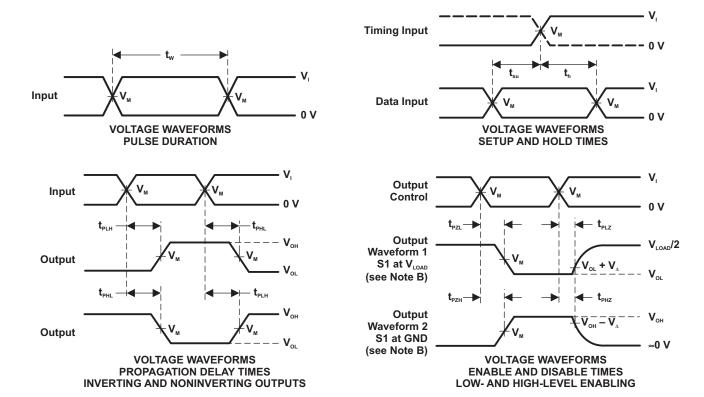


Parameter Measurement Information



TEST	S1
t _{PLH} /t _{PHL}	Open
$t_{_{\mathrm{PLZ}}}/t_{_{\mathrm{PZL}}}$	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

.,	INI	PUTS	.,	v		-	.,
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C _L	$R_{\scriptscriptstyle L}$	V _A
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	1 k Ω	0.15 V
2.5 V ± 0.2 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V _{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z₀ = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and \dot{t}_{PHZ} are the same as t_{dis} .
- F. $t_{\mbox{\tiny PZL}}$ and $t_{\mbox{\tiny PZH}}$ are the same as $t_{\mbox{\tiny en}}.$
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms



REVISION HISTORY

Changes from Revision C (January 2007) to Revision D					
•	Updated document to new TI data sheet format.	1			
•	Removed Ordering Information table.	1			
•	Added ESD warning.	2			
•	Updated operating temperature range.	3			





15-Apr-2017

PACKAGING INFORMATION

	,										,
Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
74LVC2G132DCTRG4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C3B Z	Samples
74LVC2G132DCURG4	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C3BR	Samples
SN74LVC2G132DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C3B Z	Samples
SN74LVC2G132DCUR	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 125	(3B ~ C3BR) CZ	Samples
SN74LVC2G132DCUT	ACTIVE	VSSOP	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C3BR	Samples
SN74LVC2G132YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(D57 ~ D5N)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



PACKAGE OPTION ADDENDUM

15-Apr-2017

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC2G132DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G132DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G132DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.05	3.3	1.0	4.0	8.0	Q3
SN74LVC2G132DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G132YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

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*All dimensions are nominal

All difficions die nomina										
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)			
74LVC2G132DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0			
SN74LVC2G132DCTR	SM8	DCT	8	3000	182.0	182.0	20.0			
SN74LVC2G132DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0			
SN74LVC2G132DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0			
SN74LVC2G132YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0			

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



NOTES:

- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-187 variation CA.



DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DCT (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. Falls within JEDEC MO-187 variation DA.

DCT (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.





DIE SIZE BALL GRID ARRAY



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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