

REF29xx 100 ppm/°C, 50 μ A in 3-Pin SOT-23 CMOS Voltage Reference

1 Features

- *Micro*SIZE Package: SOT-23
- Low Dropout: 1 mV
- High Output Current: 25 mA
- Low Temperature Drift: Maximum of 100 ppm/°C
- High Accuracy: 2%
- Low I_Q : Maximum of 50 μ A

2 Applications

- Portable, Battery-Powered Equipment
- Data Acquisition Systems
- Medical Equipment
- Hand-Held Test Equipment

3 Description

The REF29xx is a precision, low-power, low-voltage dropout voltage reference family available in a tiny 3-pin SOT-23 package.

The small size and low power consumption (50 μ A maximum) of the REF29xx make it ideal for portable and battery-powered applications. The REF29xx does not require a load capacitor, but it is stable with any capacitive load.

Unloaded, the REF29xx can be operated with supplies within 1 mV of output voltage. All models are specified for the wide temperature range, -40°C to 125°C .

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
REF29xx	SOT-23 (3)	2.92 mm x 1.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Dropout Voltage vs Load Current

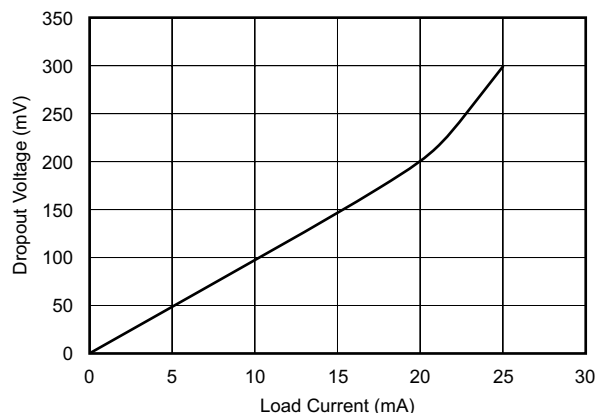


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4 Revision History

Changes from Revision B (February 2008) to Revision C

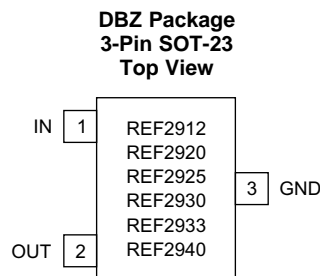
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- Added *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section..... **1**
- Deleted *Ordering Information* table; see POA at the end of the data sheet..... **1**

5 Device Comparison Table

PRODUCT	VOLTAGE (V)
REF2912	1.25
REF2920	2.048
REF2925	2.5
REF2930	3
REF2933	3.3
REF2940	4.096

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Input supply voltage
2	OUT	O	Reference output voltage
3	GND	—	Ground

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage, V+ to V–		7	V
Output short circuit ⁽²⁾	Continuous		°C
Lead temperature (soldering, 10 s)		300	°C
Operating temperature	–40	125	°C
Junction temperature		150	°C
Storage temperature, T _{stg}	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to ground.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{IN}	Input voltage	V _{REF} + 0.05 ⁽¹⁾	5.5	V
I _{LOAD}	Load current		25	mA
T _A	Operating temperature	–40	125	°C

- (1) Minimum supply voltage for the REF2912 is 1.8 V.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		REF29xx	UNIT
		DBZ (SOT-23)	
		3 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	297.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	128.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	91.7	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	12.8	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	90.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to 125°C . At $T_A = 25^{\circ}\text{C}$, $I_{\text{LOAD}} = 0\text{ mA}$, $V_{\text{IN}} = 5\text{ V}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REF2912 – 1.25 V						
V_{OUT}	Output voltage		1.225	1.25	1.275	V
	Initial accuracy				2%	
	Output voltage noise	$f = 0.1\text{ Hz to }10\text{ Hz}$,		14		μV_{PP}
	Voltage noise	$f = 10\text{ Hz to }10\text{ kHz}$		42		μV_{RMS}
	Line regulation	$1.8\text{ V} \leq V_{\text{IN}} \leq 5.5\text{ V}$		60	190	$\mu\text{V}/\text{V}$
REF2920						
V_{OUT}	Output voltage		2.007	2.048	2.089	V
	Initial accuracy				2%	
	Output voltage noise	$f = 0.1\text{ Hz to }10\text{ Hz}$,		23		μV_{PP}
	Voltage noise	$f = 10\text{ Hz to }10\text{ kHz}$		65		μV_{RMS}
	Line regulation	$V_{\text{REF}} + 50\text{ mV} \leq V_{\text{IN}} \leq 5.5\text{ V}$		110	290	$\mu\text{V}/\text{V}$
REF2925						
V_{OUT}	Output voltage		2.45	2.5	2.55	V
	Initial accuracy				2%	
	Output voltage noise	$f = 0.1\text{ Hz to }10\text{ Hz}$		28		μV_{PP}
	Voltage noise	$f = 10\text{ Hz to }10\text{ kHz}$		80		μV_{RMS}
	Line regulation	$V_{\text{REF}} + 50\text{ mV} \leq V_{\text{IN}} \leq 5.5\text{ V}$		120	325	$\mu\text{V}/\text{V}$
REF2930						
V_{OUT}	Output voltage		2.94	3	3.06	V
	Initial accuracy				2%	
	Output voltage noise	$f = 0.1\text{ Hz to }10\text{ Hz}$,		33		μV_{PP}
	Voltage noise	$f = 10\text{ Hz to }10\text{ kHz}$		94		μV_{RMS}
	Line regulation	$V_{\text{REF}} + 50\text{ mV} \leq V_{\text{IN}} \leq 5.5\text{ V}$		120	375	$\mu\text{V}/\text{V}$
REF2933						
V_{OUT}	Output voltage		3.234	3.3	3.366	V
	Initial accuracy				2%	
	Output voltage noise	$f = 0.1\text{ Hz to }10\text{ Hz}$,		36		μV_{PP}
	Voltage noise	$f = 10\text{ Hz to }10\text{ kHz}$		105		μV_{RMS}
	Line regulation	$V_{\text{REF}} + 50\text{ mV} \leq V_{\text{IN}} \leq 5.5\text{ V}$		130	400	$\mu\text{V}/\text{V}$
REF2940						
V_{OUT}	Output voltage		4.014	4.096	4.178	V
	Initial accuracy				2%	
	Output voltage noise	$f = 0.1\text{ Hz to }10\text{ Hz}$,		45		μV_{PP}
	Voltage noise	$f = 10\text{ Hz to }10\text{ kHz}$		128		μV_{RMS}
		$V_{\text{REF}} + 50\text{ mV} \leq V_{\text{IN}} \leq 5.5\text{ V}$		160	410	$\mu\text{V}/\text{V}$
REF2912, REF2920, REF2925, REF2930, REF2933, REF2940						
dV_{OUT}/dT	Output voltage temperature drift ⁽¹⁾	$-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$		35	100	ppm/ $^{\circ}\text{C}$
I_{LOAD}	Output current				25	mA
	Long-term stability	0 to 1000 _H		24		ppm
		1000 to 2000 _H		15		
$dV_{\text{OUT}}/dI_{\text{LOAD}}$	Load regulation ⁽²⁾	$0\text{ mA} < I_{\text{LOAD}} < 25\text{ mA}$, $V_{\text{IN}} = V_{\text{REF}} + 500\text{ mV}$ ⁽³⁾		3	100	$\mu\text{V}/\text{mA}$

(1) Box Method used to determine overtemperature drift.

(2) Typical value of load regulation reflects measurements using a force and sense contacts, see [Load Regulation](#).

(3) Minimum supply voltage for REF2912 is 1.8 V.

Electrical Characteristics (continued)

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to 125°C . At $T_A = 25^{\circ}\text{C}$, $I_{\text{LOAD}} = 0$ mA, $V_{\text{IN}} = 5$ V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dT	Thermal Hysteresis ⁽⁴⁾			25	100	ppm
$V_{\text{IN}} - V_{\text{OUT}}$	Dropout voltage			1	50	mV
I_{SC}	Short-circuit current			45		mA
	Turnon settling time	to 0.1% at $V_{\text{IN}} = 5$ V with $C_L = 0$		120		μs
POWER SUPPLY						
V_S	Voltage	$I_L = 0$		$V_{\text{REF}} + 0.001$ ⁽⁵⁾	5.5	V
	Voltage over temperature	$-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$		$V_{\text{REF}} + 0.05$	5.5	
I_Q	Quiescent current			42	50	μA
	Quiescent current over temperature	$-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$			59	
TEMPERATURE RANGE						
	Specified range			-40	125	$^{\circ}\text{C}$
	Operating range			-40	125	$^{\circ}\text{C}$
	Storage range			-65	150	$^{\circ}\text{C}$
$R_{\theta\text{JC}}$	Thermal resistance for SOT-23 surface-mount			110		$^{\circ}\text{C}/\text{W}$
$R_{\theta\text{JA}}$				336		$^{\circ}\text{C}/\text{W}$

(4) Thermal hysteresis procedure is explained in more detail in [Thermal Hysteresis](#).

(5) For $I_L > 0$, see [Typical Characteristics](#).

7.6 Typical Characteristics

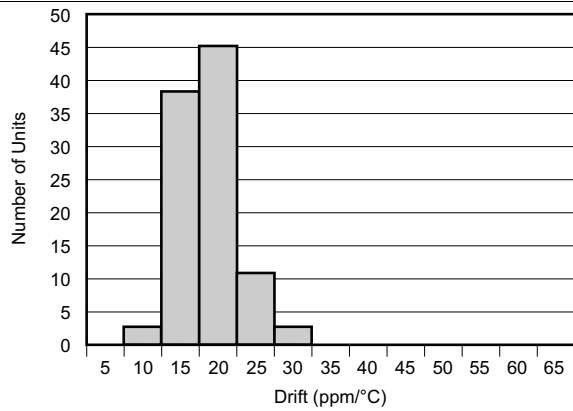


Figure 1. Temperature Drift (0°C to 70°C)

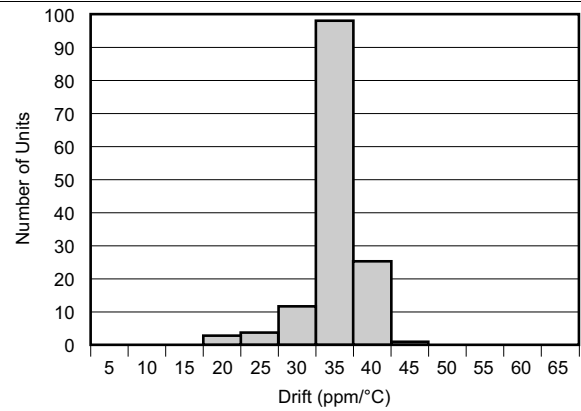


Figure 2. Temperature Drift (-40°C to 125°C)

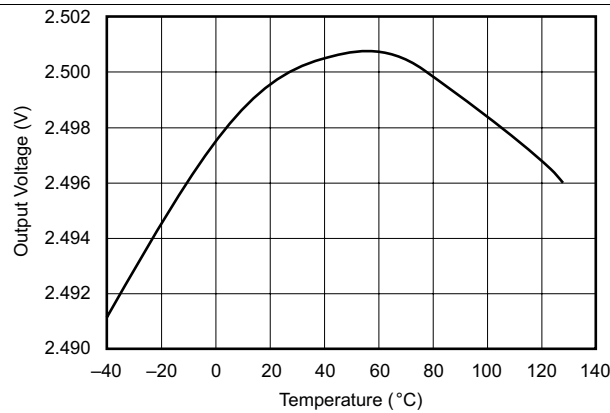


Figure 3. Output Voltage vs Temperature

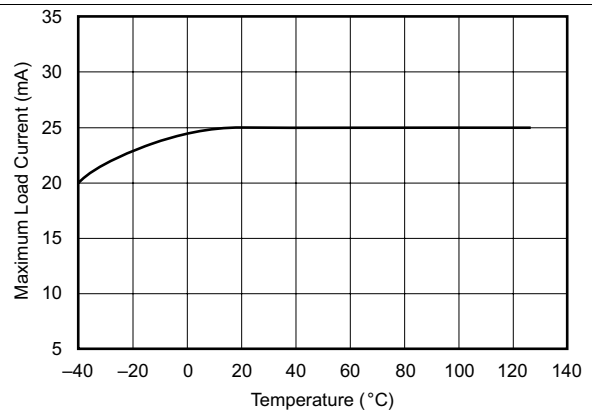


Figure 4. Maximum Load Current vs Temperature

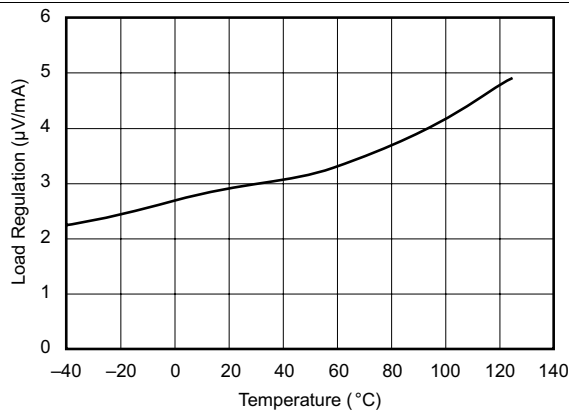


Figure 5. Load Regulation vs Temperature

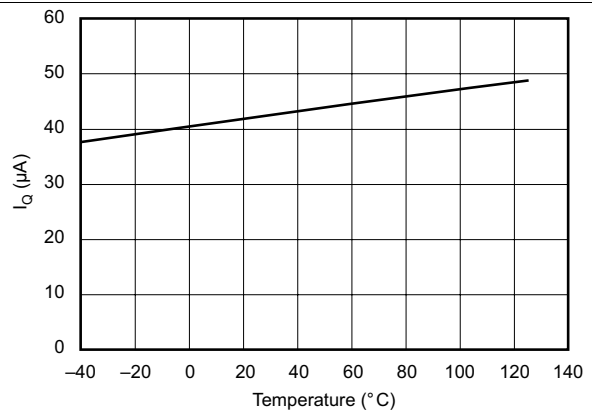


Figure 6. Quiescent Current vs Temperature

Typical Characteristics (continued)

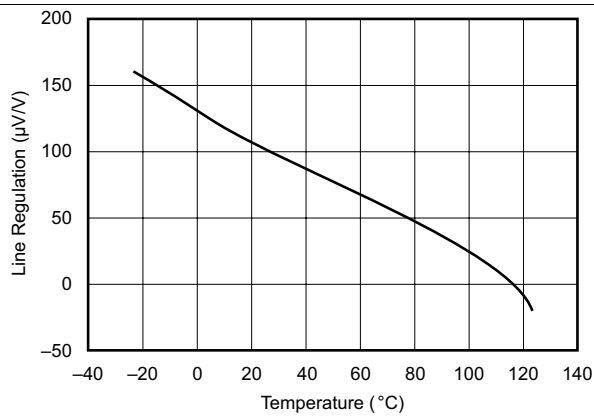


Figure 7. Line Regulation vs Temperature

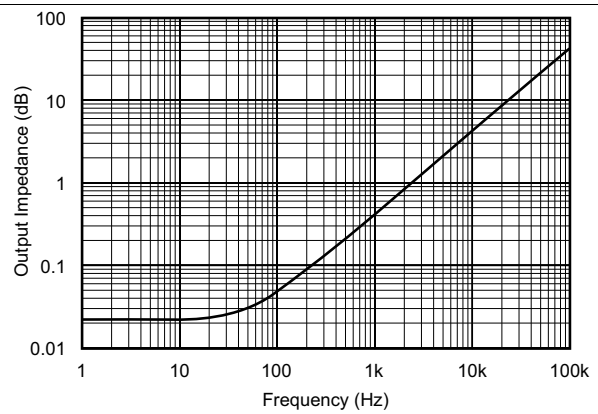


Figure 8. Output Impedance vs Frequency

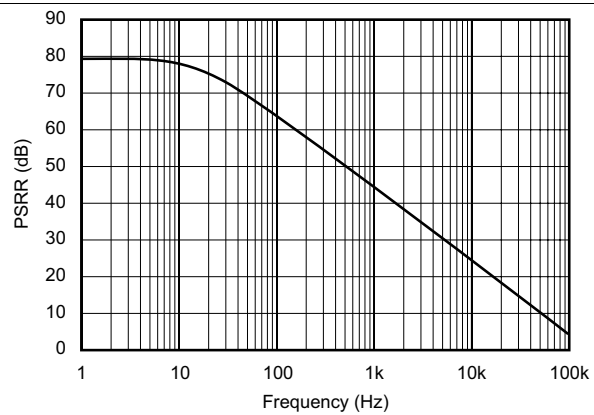


Figure 9. Power-Supply Rejection Ratio vs Frequency

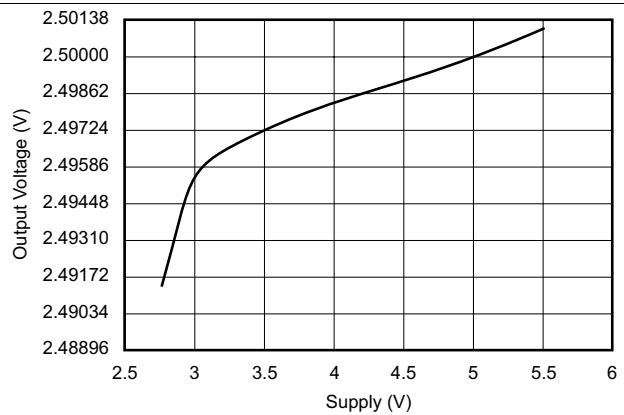


Figure 10. Output Voltage vs Supply Voltage (No Load)

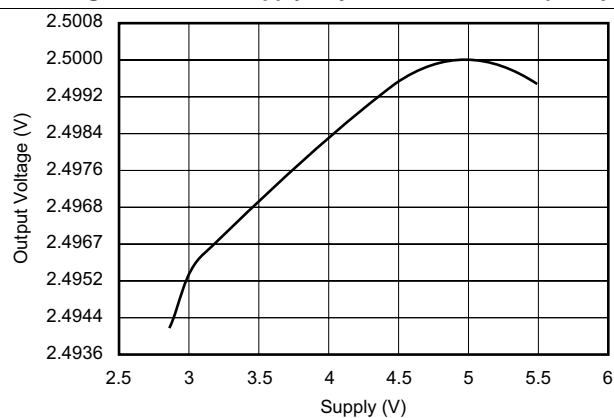


Figure 11. Output Voltage vs Supply Voltage ($I_{LOAD} = 25\text{ mA}$)

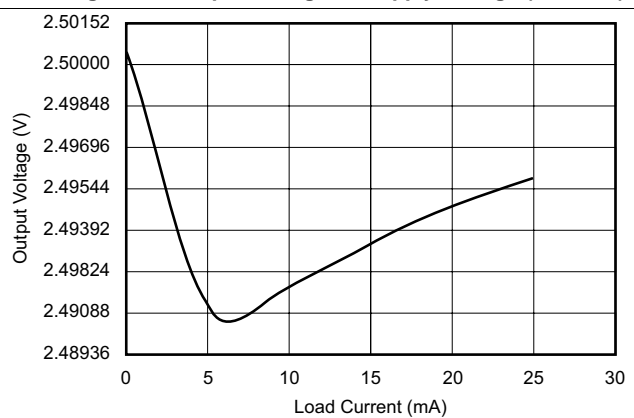


Figure 12. Output Voltage vs Load Current

Typical Characteristics (continued)

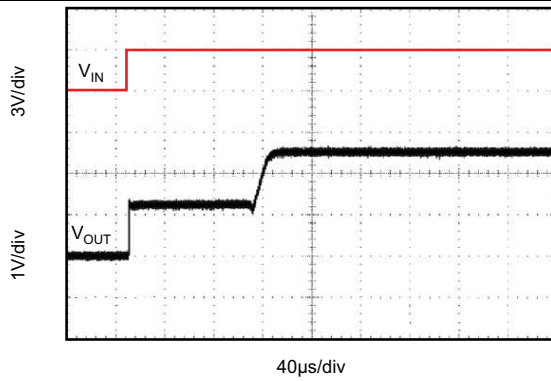


Figure 13. Step Response, $C_L = 0$, 3-V Start-Up

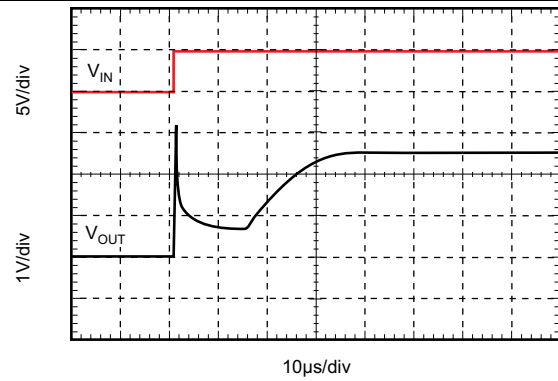


Figure 14. Step Response, $C_L = 0$, 5-V Start-Up

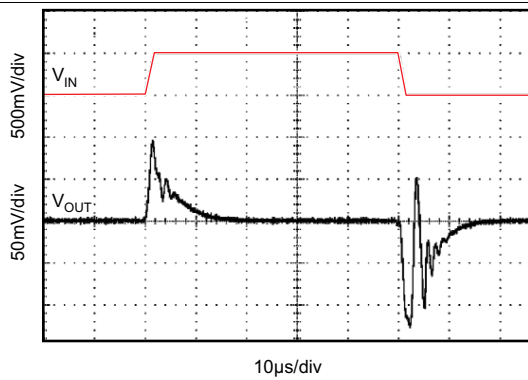


Figure 15. Line Transient Response

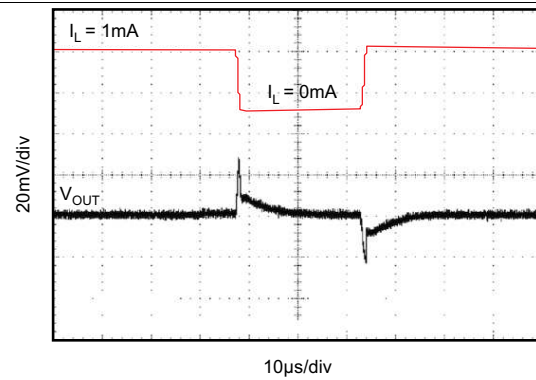


Figure 16. 0 to 1-mA Load Transient ($C_L = 0$)

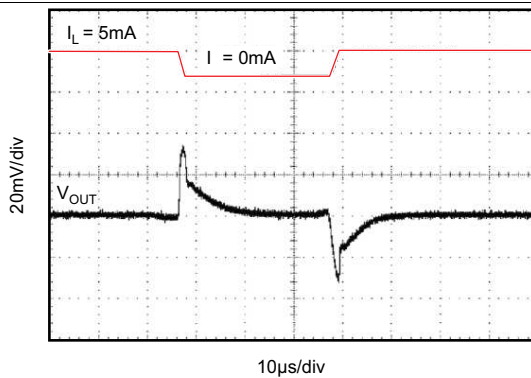


Figure 17. 0 to 5-mA Load Transient ($C_L = 0$)

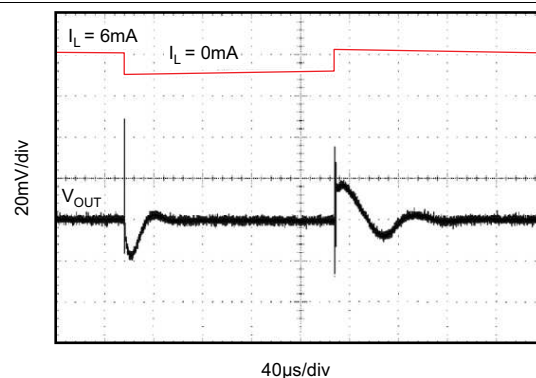


Figure 18. 1 to 6-mA Load Transient ($C_L = 1 \mu\text{F}$)

Typical Characteristics (continued)

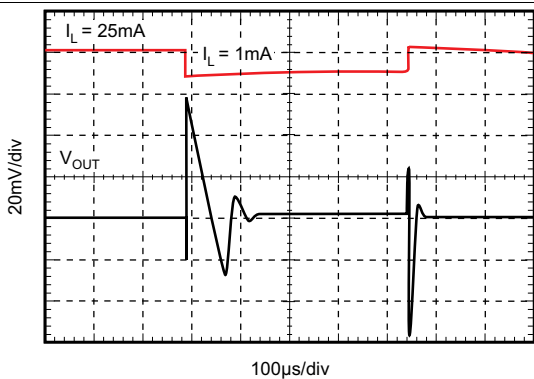


Figure 19. 1 to 25-mA Load Transient ($C_L = 1 \mu\text{F}$)

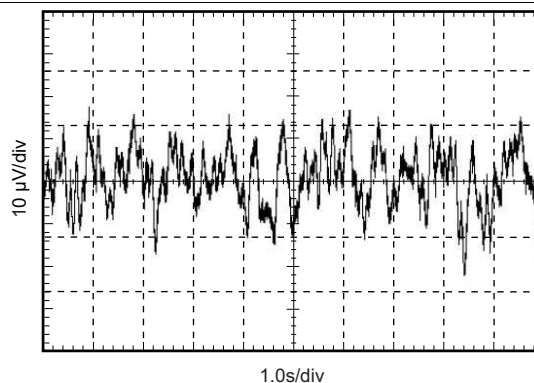


Figure 20. 0.1 to 10-Hz Noise

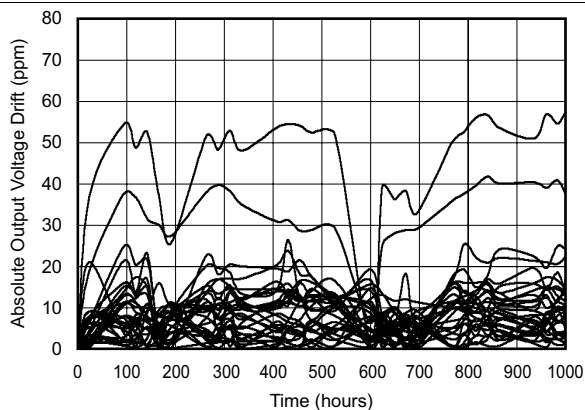


Figure 21. Long-Term Stability 0 to 1000 Hours

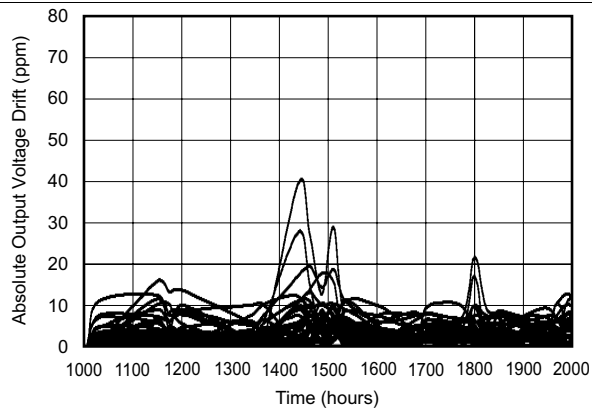


Figure 22. Long-Term Stability 1000 to 2000 Hours

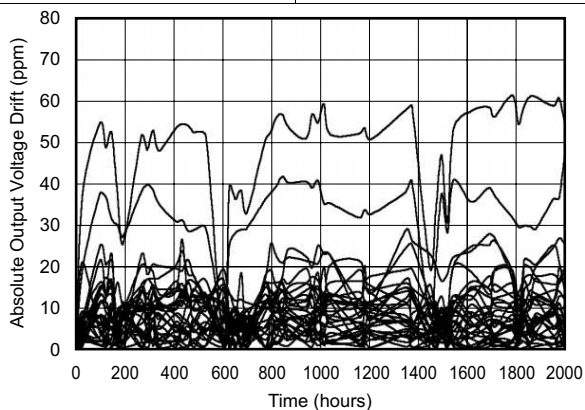


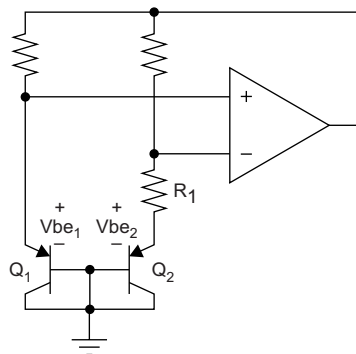
Figure 23. Long-Term Stability 0 to 2000 Hours

8 Detailed Description

8.1 Overview

The REF29xx is a series, CMOS, precision band-gap voltage reference. Its basic topology is shown in [Functional Block Diagram](#). The transistors Q_1 and Q_2 are biased such that the current density of Q_1 is greater than that of Q_2 . The difference of the two base-emitter voltages, $V_{be1} - V_{be2}$, has a positive temperature coefficient and is forced across resistor R_1 . This voltage is gained up and added to the base-emitter voltage of Q_2 , which has a negative coefficient. The resulting output voltage is virtually independent of temperature. The curvature of the band-gap voltage, as seen in [Figure 3](#), is due to the slightly nonlinear temperature coefficient of the base-emitter voltage of Q_2 .

8.2 Functional Block Diagram



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Figure 24. Simplified Schematic of Band-Gap Reference

8.3 Feature Description

8.3.1 Supply Voltage

The REF29xx family of references features an extremely low dropout voltage. With the exception of the REF2912, which has a minimum supply requirement of 1.8 V, the REF29xx can be operated with a supply of only 1 mV above the output voltage in an unloaded condition. For loaded conditions, see [Dropout Voltage vs Load Current](#).

The REF29xx features a low quiescent current, which is extremely stable over changes in both temperature and supply. The typical room temperature quiescent current is 42 μ A, and the maximum quiescent current over temperature is just 59 μ A. Additionally, the quiescent current typically changes less than 2.5 μ A over the entire supply range, as shown in [Figure 25](#).

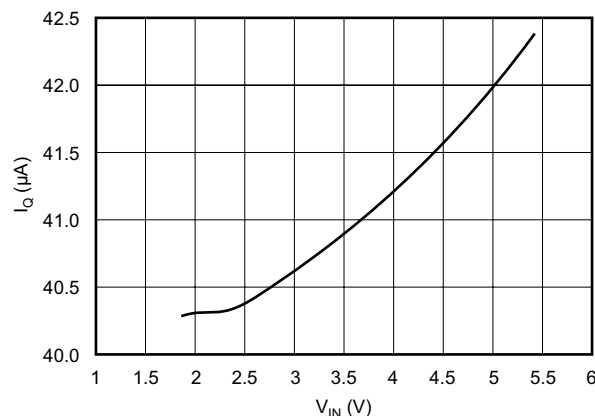


Figure 25. Supply Current vs Supply Voltage

Feature Description (continued)

Supply voltages below the specified levels can cause the REF29xx to momentarily draw currents greater than the typical quiescent current. Using a power supply with a fast rising edge and low output impedance easily prevents this.

8.3.2 Thermal Hysteresis

Thermal hysteresis for the REF29xx is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C, and can be expressed as shown in [Equation 1](#).

$$V_{\text{HYST}} = \left(\frac{\text{abs}|V_{\text{PRE}} - V_{\text{POST}}|}{V_{\text{NOM}}} \right) \times 10^6 \text{ (ppm)}$$

where

- V_{HYST} = calculated hysteresis
 - V_{PRE} = output voltage measured at 25°C pretemperature cycling
 - V_{POST} = output voltage measured when device has been operated at 25°C, cycled through specified range –40°C to 125°C and returned to operation at 25°C
- (1)

8.3.3 Temperature Drift

The REF29xx is designed to exhibit minimal drift error, defined as the change in output voltage over varying temperature. Using the *box* method of drift measurement, the REF29xx features a typical drift coefficient of 20 ppm from 0°C to 70°C—the primary temperature range of use for many applications. For industrial temperature ranges of –40°C to 125°C, the REF29xx family drift increases to a typical value of 50 ppm.

8.3.4 Noise Performance

The REF29xx generates noise less than 50 μV_{PP} between frequencies of 0.1 Hz to 10 Hz, and can be seen in [Figure 20](#). The noise voltage of the REF29xx increases with output voltage and operating temperature. Additional filtering may be used to improve output noise levels, however, take care ensuring the output impedance does not degrade AC performance.

8.3.5 Long-Term Stability

Long-term stability refers to the change of the output voltage of a reference over a period of months or years. This effect lessens as time progresses as is apparent by the long-term stability curves. The typical drift value for the REF29xx is 24 ppm from 0 to 1000 hours, and 15 ppm from 1000 to 2000 hours. This parameter is characterized by measuring 30 units at regular intervals for a period of 2000 hours.

8.3.6 Load Regulation

Load regulation is defined as the change in output voltage due to changes in load current. Load regulation for the REF29xx is measured using force and sense contacts as pictured in [Figure 26](#). The force and sense lines tied to the contact area of the output pin reduce the impact of contact and trace resistance, resulting in accurate measurement of the load regulation contributed solely by the REF29xx. For applications requiring improved load regulation, force and sense lines must be used.

Feature Description (continued)

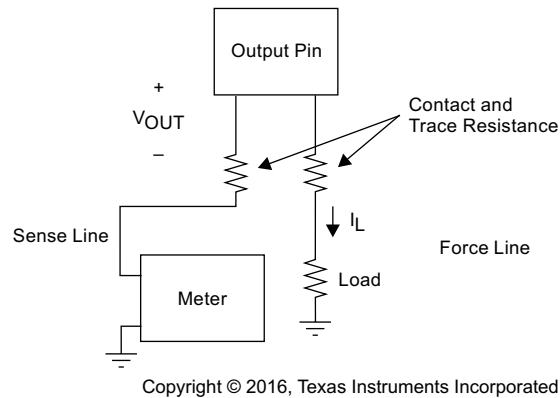


Figure 26. Accurate Load Regulation of REF29xx

8.4 Device Functional Modes

8.4.1 Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the OPA703 and REF29xx can be used to provide a dual-supply reference from a ± 5 -V supply. Figure 27 shows the REF2925 used to provide a ± 2.5 -V supply reference voltage. The low offset voltage and low drift of the OPA703 complement the low drift performance of the REF29xx to provide an accurate solution for split-supply applications.

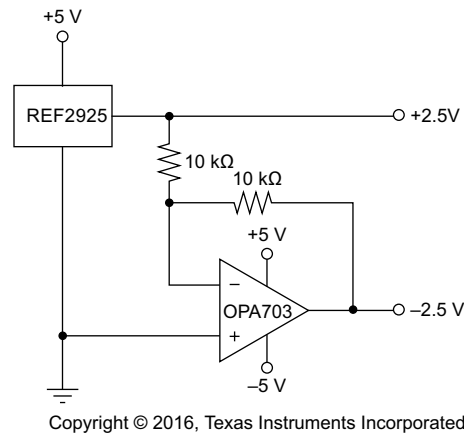
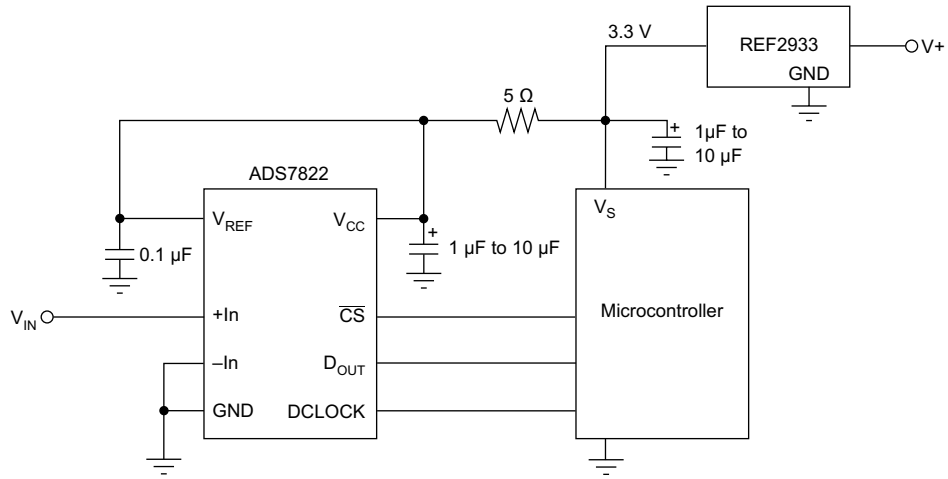


Figure 27. REF2925 Combined With OPA703 to Create Positive and Negative Reference Voltages

8.4.2 Data Acquisition

Often data acquisition systems require stable voltage references to maintain necessary accuracy. The REF29xx family features stability and a wide range of voltages suitable for most micro-controllers and data converters. See Figure 28 for a basic data acquisition system.

Device Functional Modes (continued)



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Figure 28. Basic Data Acquisition System 1

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

For normal operation, the REF29xx does not require a capacitor on the output. If a capacitive load is connected, take special care when using low equivalent series resistance (ESR) capacitors and high capacitance. This precaution is especially true for low-output voltage devices; therefore, for the REF2912 use a low-ESR capacitance of 10 μF or less. [Figure 29](#) shows the typical connections required for operation of the REF29xx. TI always recommends a supply bypass capacitor of 0.47 μF .

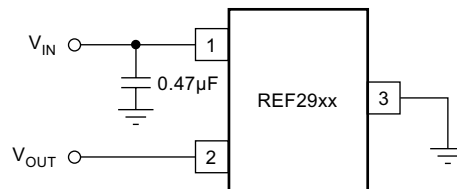
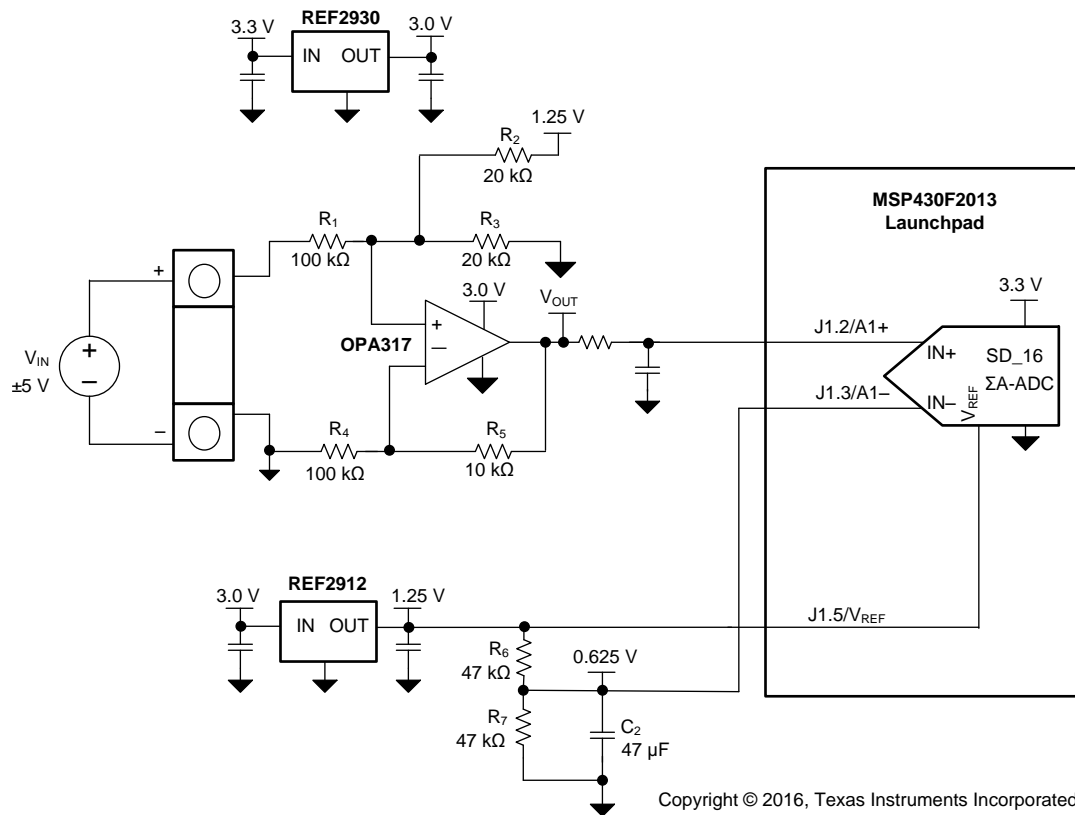


Figure 29. Typical Connections for Operating REF29xx

9.2 Typical Application

[Figure 30](#) shows a low-power reference and conditioning circuit. This circuit attenuates and level-shifts a bipolar input voltage within the proper input range of a single-supply low-power 16-bit $\Delta\Sigma$ ADC, such as the one inside the [MSP430](#) or other similar single-supply ADCs. Precision reference circuits are used to level-shift the input signal, provide the ADC reference voltage and to create a well-regulated supply voltage for the low-power analog circuitry. A low-power, zero-drift, operational amplifier circuit is used to attenuate and level-shift the input signal.

Typical Application (continued)



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Figure 30. Low-Power Reference and Bipolar Voltage Conditioning Circuit for Low-Power ADCs

Typical Application (continued)

9.2.1 Design Requirements

- Supply Voltage: 3.3 V
- Maximum Input Voltage: ± 6 V
- Specified Input Voltage: ± 5 V
- ADC Reference Voltage: 1.25 V

The goal for this design is to accurately condition a ± 5 -V bipolar input voltage into a voltage suitable for conversion by a low-voltage ADC with a 1.25-V reference voltage, V_{REF} , and an input voltage range of $V_{REF} / 2$. The circuit should function with reduced performance over a wider input range of at least ± 6 V to allow for easier protection of overvoltage conditions.

9.2.2 Detailed Design Procedure

Figure 30 depicts a simplified schematic for this design showing the MSP430 ADC inputs and full input-conditioning circuitry. The ADC is configured for a bipolar measurement where final conversion result is the differential voltage between the voltage at the positive and negative ADC inputs. The bipolar, GND referenced input signal must be level-shifted and attenuated by the operational amplifier so that the output is biased to $V_{REF} / 2$ and has a differential voltage that is within the $\pm V_{REF} / 2$ input range of the ADC.

9.2.3 Application Curves

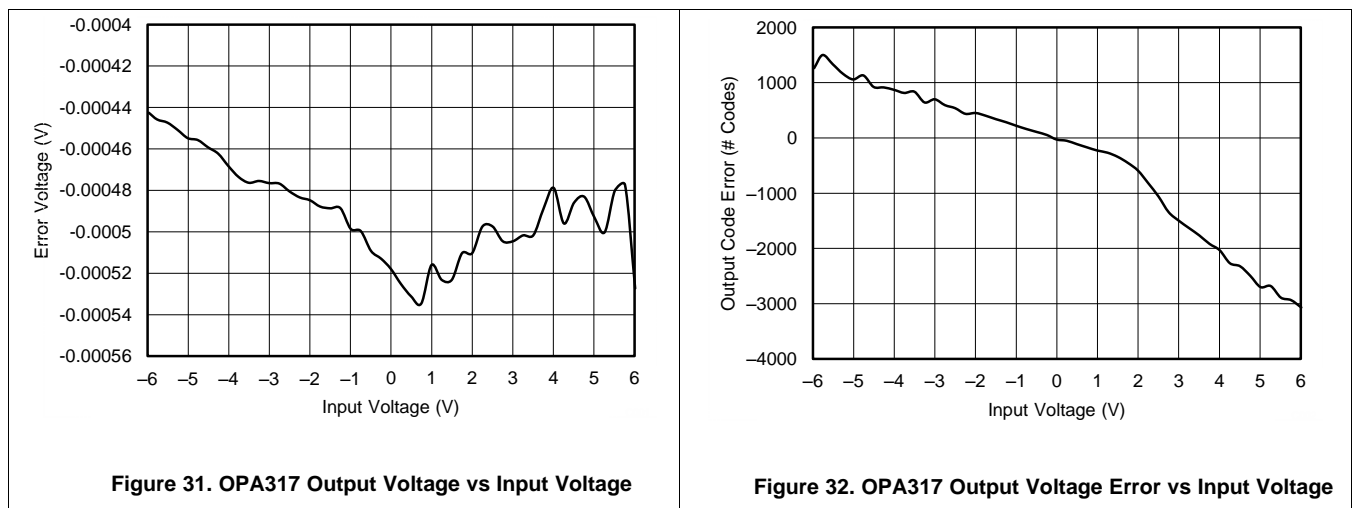


Figure 31. OPA317 Output Voltage vs Input Voltage

Figure 32. OPA317 Output Code Error vs Input Voltage

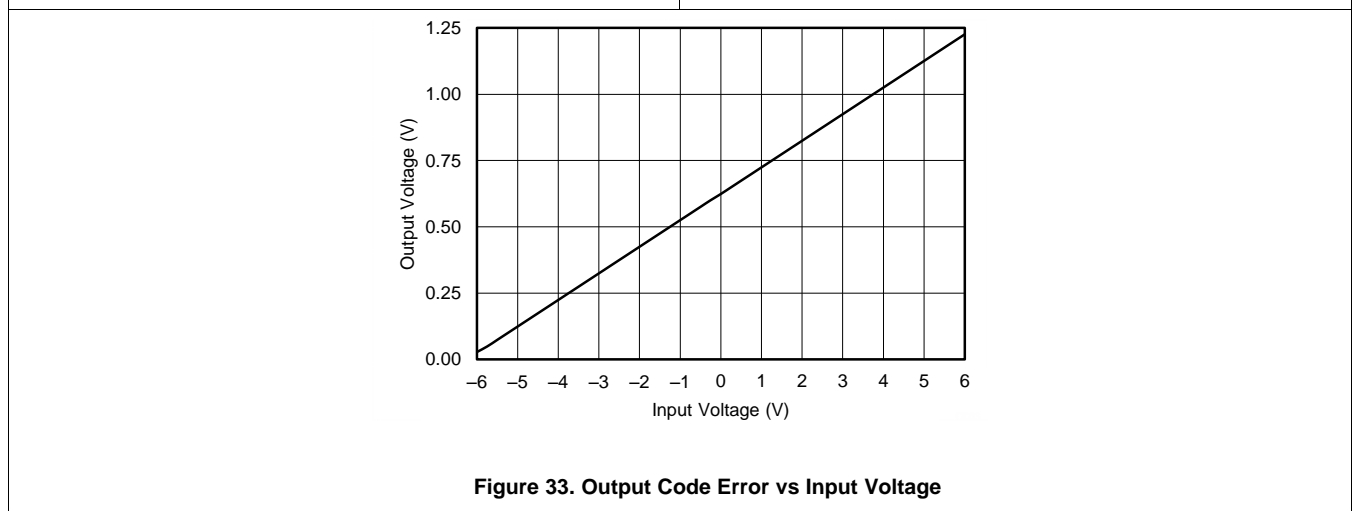


Figure 33. Output Code Error vs Input Voltage

10 Power Supply Recommendations

The REF29xx family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 50 mV above the output voltage. For loaded reference conditions, see [Dropout Voltage vs Load Current](#). Use a supply bypass capacitor greater than 0.47 μ F.

11 Layout

11.1 Layout Guidelines

[Figure 34](#) illustrates an example of a printed-circuit board (PCB) layout using the REF29xx. Some key considerations are:

- Connect low-ESR, 0.1- μ F ceramic bypass capacitors at V_{IN} of the REF29xx
- Decouple other active devices in the system per the device specifications
- Use a solid ground plane to help distribute heat and reduces electromagnetic interference (EMI) noise pickup
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring
- Minimize trace length between the reference and bias connections to the INA and ADC to reduce noise pickup
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary

11.2 Layout Example

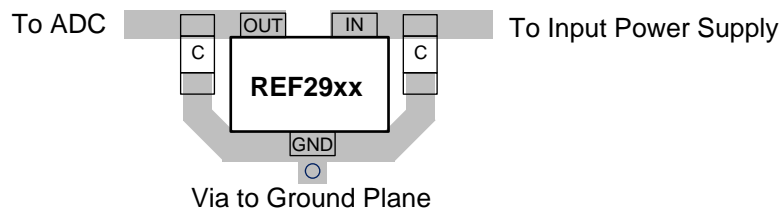


Figure 34. REF29xx Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
REF2912	Click here	Click here	Click here	Click here	Click here
REF2920	Click here	Click here	Click here	Click here	Click here
REF2925	Click here	Click here	Click here	Click here	Click here
REF2930	Click here	Click here	Click here	Click here	Click here
REF2933	Click here	Click here	Click here	Click here	Click here
REF2940	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF2912AIDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29A	Samples
REF2912AIDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29A	Samples
REF2912AIDBZTG4	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29A	Samples
REF2920AIDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29B	Samples
REF2920AIDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29B	Samples
REF2920AIDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29B	Samples
REF2920AIDBZTG4	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29B	Samples
REF2925AIDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29C	Samples
REF2925AIDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29C	Samples
REF2925AIDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29C	Samples
REF2925AIDBZTG4	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29C	Samples
REF2930AIDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29D	Samples
REF2930AIDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29D	Samples
REF2930AIDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29D	Samples
REF2930AIDBZTG4	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29D	Samples
REF2933AIDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29E	Samples
REF2933AIDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29E	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF2933AIDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29E	Samples
REF2933AIDBZTG4	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29E	Samples
REF2940AIDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29F	Samples
REF2940AIDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29F	Samples
REF2940AIDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29F	Samples
REF2940AIDBZTG4	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R29F	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF2912AIDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
REF2912AIDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
REF2920AIDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
REF2920AIDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
REF2925AIDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
REF2925AIDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
REF2930AIDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
REF2930AIDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
REF2933AIDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
REF2933AIDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
REF2940AIDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
REF2940AIDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF2912AIDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
REF2912AIDBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
REF2920AIDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
REF2920AIDBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
REF2925AIDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
REF2925AIDBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
REF2930AIDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
REF2930AIDBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
REF2933AIDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
REF2933AIDBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
REF2940AIDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
REF2940AIDBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0

GENERIC PACKAGE VIEW

DBZ 3

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203227/C

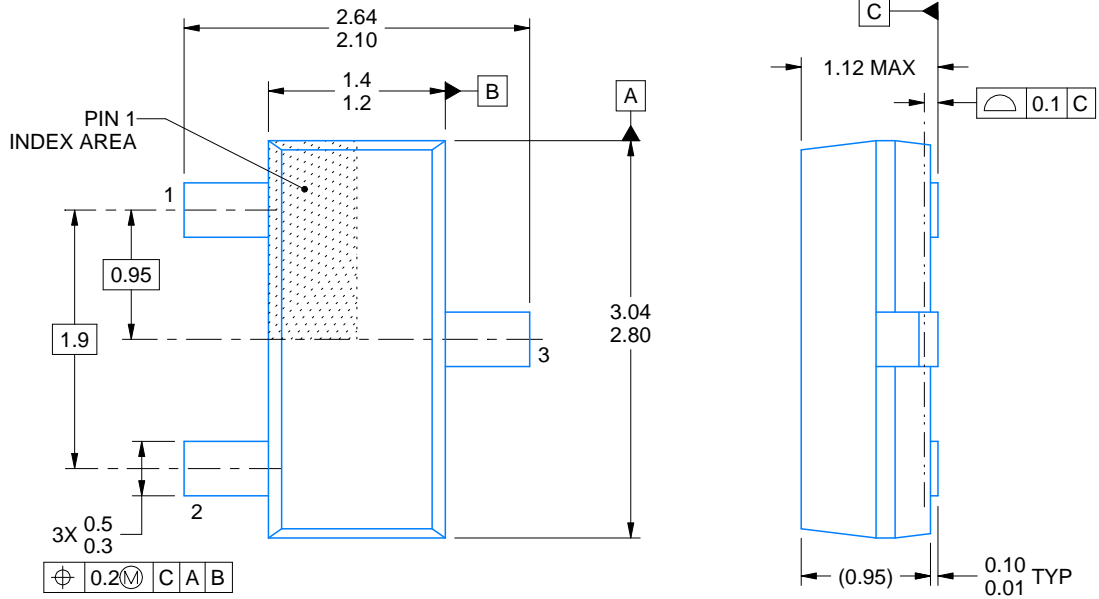
DBZ0003A



PACKAGE OUTLINE

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



4214838/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.

EXAMPLE BOARD LAYOUT

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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