TS3A474x 0.9-Ω Low-Voltage Single-Supply 2-Channel SPST Analog Switches

1 Features

- Low ON-State Resistance (R_{on})
  - 0.9-Ω Max (3-V Supply)
  - 1.5-Ω Max (1.8-V Supply)
- 0.4-Ω Max R_{on} Flatness (3-V Supply)
- 1.6-V to 3.6-V Single-Supply Operation
- Available in SOT-23 and VSSOP Packages
- High Current-Handling Capacity (100 mA Continuous)
- 1.8-V CMOS Logic Compatible (3-V Supply)
- Fast Switching: t_{ON} = 14 ns, t_{OFF} = 9 ns

2 Applications

- Power Routing
- Battery-Powered Systems
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communications Circuits
- PCMCIA Cards
- Cellular Phones
- Modems
- Hard Drives

3 Description

The TS3A4741 and TS3A4742 are bi-directional, 2-channel single-pole/single-throw (SPST) analog switches with low ON-state resistance (R_{on}), low-voltage, that operate from a single 1.6-V to 3.6-V supply. These devices have fast switching speeds, handle rail-to-rail analog signals, and consume very low quiescent power.

The digital logic input is 1.8-V CMOS compatible when using a single 3-V supply.

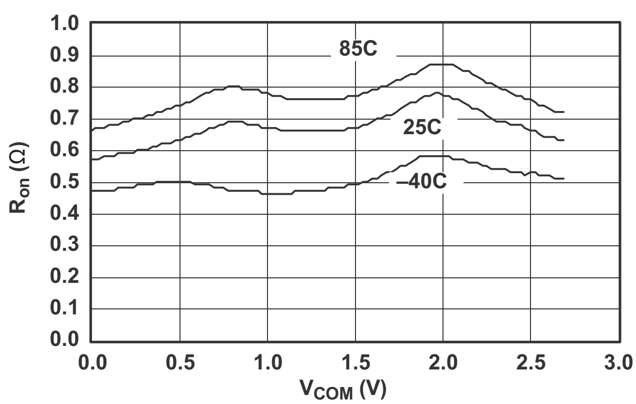
The TS3A4741 has two normally open (NO) switches, and the TS3A4742 has two normally closed (NC) switches.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3A4741	SOT (8)	2.90 mm × 1.63 mm
	VSSOP (8)	3.00 mm × 3.00 mm
TS3A4742	SOT (8)	2.90 mm × 1.63 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

R_{on} vs V_{COM} (V_{CC} = 2.7 V)



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4 Revision History

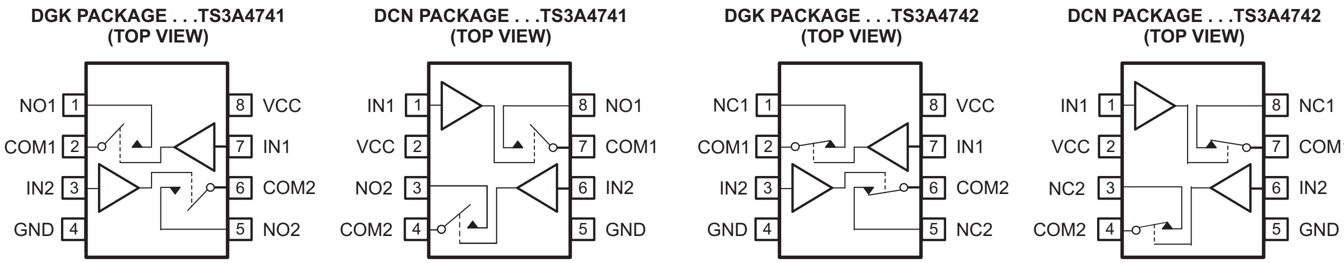
Changes from Revision E (December 2014) to Revision F — **Page**

- Changed DCN package to clarify switch configuration. 3
- Changed the V_{IN} MAX value in the *Recommended Operating Conditions* table from: 1.8 V to: V_{CC} 4

Changes from Revision D (June 2014) to Revision E — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

5 Pin Configuration and Functions



Pin Functions

PIN					I/O	DESCRIPTION
NAME	TS3A4741		TS3A4742			
	MSOP	SOT	MSOP	SOT		
COM1	2	7	2	7	I/O	Common
COM2	6	4	6	4	I/O	Common
GND	4	5	4	5	—	Ground
IN1	7	1	7	1	I	Digital control to connect COM to NO or NC
IN2	3	6	3	6	I	Digital control to connect COM to NO or NC
NC1	—	—	1	8	I/O	Normally closed
NC2	—	—	5	3	I/O	Normally closed
NO1	1	8	—	—	I/O	Normally open
NO2	5	3	—	—	I/O	Normally open
VCC	8	2	8	2	I	Power supply

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage reference to GND[2]		–0.3	4	V
V_{NO} V_{COM} V_{IN}	Analog and digital voltage		–0.3	V_{CC} + 0.3	V
I_{NO} I_{COM}	On-state switch current	V_{NO}, V_{COM} = 0 to V_{CC}	–100	100	mA
I_{CC} I_{GND}	Continuous current through V_{CC} or GND			±100	mA
	Peak current pulsed at 1 ms, 10% duty cycle	COM, V_{NO}, V_{COM}		±200	mA
T_A	Operating temperature		–40	85	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Signals on COM or NO exceeding V_{CC} or GND are clamped by internal diodes. Limit forward diode current to maximum current rating.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage reference to ground	1.6	3.6	V
V_{NO} V_{COM}	Analog voltage	0	3.6	V
V_{IN}	Digital Voltage	0	V_{CC}	V

6.4 Thermal Information

THERMAL METRIC[1]		TS3A474x DCN/DGK 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	214.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	191.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	113.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	52.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	110.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics (3-V Supply)[1][2]

V_{CC} = 2.7 V to 3.6 V, T_A = –40 to 85°C, V_{IH} = 1.4 V, V_{IL} = 0.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP[3]	MAX	UNIT
ANALOG SWITCH								
V_{COM}, V_{NO}, V_{NC}	Analog signal range				0		V_+	V
R_{on}	ON-state resistance	V_{CC} = 2.7 V, I_{COM} = –100 mA, V_{NO}, V_{NC} = 1.5 V		25°C		0.7	0.9	Ω
				Full			1.1	
ΔR_{on}	ON-state resistance match between channels[4]	V_{CC} = 2.7 V, I_{COM} = –100 mA, V_{NO}, V_{NC} = 1.5 V		25°C		0.03	0.05	Ω
				Full			0.15	
$R_{on(flat)}$	ON-state resistance flatness[5]	V_{CC} = 2.7 V, I_{COM} = –100 mA, V_{NO}, V_{NC} = 1 V, 1.5 V, 2 V		25°C		0.23	0.4	Ω
				Full			0.5	
$I_{NO(OFF)}$	NO OFF leakage current[6]	V_{CC} = 3.6 V, V_{COM} = 0.3 V, 3 V, V_{NO} = 3 V, 0.3 V		25°C	–2	1	2	nA
				Full	–18		18	
$I_{COM(OFF)}$	COM OFF leakage current[6]	V_{CC} = 3.6 V, V_{COM} = 0.3 V, 3 V, V_{NO} = 3 V, 0.3 V		25°C	–2	1	2	nA
				Full	–18		18	
$I_{COM(ON)}$	COM ON leakage current[6]	V_{CC} = 3.6 V, V_{COM} = 0.3 V, 3 V, V_{NO} = 0.3 V, 3 V, or floating		25°C	–2.5	0.01	2.5	nA
				Full	–5		5	
DYNAMIC								
t_{ON}	Turn-on time	V_{NO}, V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 14		25°C		5	14	ns
				Full			15	
t_{OFF}	Turn-off time	V_{NO}, V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 14		25°C		4	9	ns
				Full			10	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF, See Figure 15		25°C		3		pC
$C_{NO(OFF)}$	NO OFF capacitance	f = 1 MHz, See Figure 16		25°C		23		pF
$C_{COM(OFF)}$	COM OFF capacitance	f = 1 MHz, See Figure 16		25°C		20		
$C_{COM(ON)}$	COM ON capacitance	f = 1 MHz, See Figure 16		25°C		43		
BW	Bandwidth	R_L = 50 Ω, Switch ON		25°C		125		MHz
O_{ISO}	OFF isolation[7]	R_L = 50 Ω, C_L = 5 pF, See Figure 17	f = 10 MHz	25°C		–40		dB
			f = 1 MHz			–62		
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF, See Figure 17	f = 10 MHz	25°C		–73		dB
			f = 1 MHz			–95		
THD	Total harmonic distortion	f = 20 Hz to 20 kHz, V_{COM} = 2 V_{P-P}	R_L = 32 Ω	25°C		0.04%		
			R_L = 600 Ω			0.003%		
DIGITAL CONTROL INPUTS (IN1, IN2)								
V_{IH}	Input logic high			Full	1.4			V
V_{IL}	Input logic low			Full			0.5	
I_{IN}	Input leakage current	V_I = 0 or V_{CC}		25°C		0.5	1	nA
				Full	–20		20	
SUPPLY								

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Parts are tested at 85°C and specified by design and correlation over the full temperature range.
(3) Typical values are at V_{CC} = 3 V, T_A = 25°C.
(4) $\Delta R_{on} = R_{on(max)} - R_{on(min)}$
(5) Flatness is defined as the difference between the maximum and minimum value of r_{on} as measured over the specified analog signal ranges.
(6) Leakage parameters are 100% tested at the maximum-rated hot operating temperature and specified by correlation at T_A = 25°C.
(7) OFF isolation = $20_{log}10$ (V_{COM}/V_{NO}), V_{COM} = output, V_{NO} = input to OFF switch

Electrical Characteristics (3-V Supply)[1][2] (continued)

V_{CC} = 2.7 V to 3.6 V, T_A = –40 to 85°C, V_{IH} = 1.4 V, V_{IL} = 0.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP[3]	MAX	UNIT
V_{CC}	Power-supply range			2.7		3.6	V
I_{CC}	Positive-supply current	V_{CC} = 3.6 V, V_{IN} = 0 or V_{CC}	25°C			0.075	μA
			Full			0.75	

6.6 Electrical Characteristics (1.8-V Supply)(1) (2)

V_{CC} = 1.65 V to 1.95 V, T_A = –40 to 85°C, V_{IH} = 1 V, V_{IL} = 0.4 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP(2)	MAX	UNIT
ANALOG SWITCH								
V_{COM}, V_{NO}, V_{NC}	Analog signal range				0		V_+	V
R_{on}	ON-state resistance	V_{CC} = 1.8 V, I_{COM} = –10 mA, V_{NO}, V_{NC} = 0.9 V		25 °C		1	1.5	Ω
				Full			2	
ΔR_{on}	ON-state resistance match between channels(1)	V_{CC} = 1.8 V, I_{COM} = –10 mA, V_{NO}, V_{NC} = 0.9 V		25 °C		0.09	0.15	Ω
				Full			0.25	
$R_{on(flat)}$	ON-state resistance flatness(3)	V_{CC} = 1.8 V, I_{COM} = –10 mA, $0 \le V_{NO}, V_{NC} \le V_{CC}$		25 °C		0.7	0.9	Ω
				Full			1.5	
$I_{NO(OFF)}$	NO OFF leakage current(4)	V_{CC} = 1.95 V, V_{COM} = 0.15 V, 1.65 V, V_{NO} = 1.8 V, 0.15 V		25 °C	–1	0.5	1	nA
				Full	–10		10	
$I_{COM(OFF)}$	COM OFF leakage current(4)	V_{CC} = 1.95 V, V_{COM} = 0.15 V, 1.65 V, V_{NO}, = 1.8 V, 0.15 V		25 °C	–1	0.5	1	nA
				Full	–10		10	
$I_{COM(ON)}$	COM ON leakage current(4)	V_{CC} = 1.95 V, V_{COM} = 0.15 V, 1.65 V, V_{NO} = 0.15 V, 1.65 V, or floating		25 °C	–1	0.01	1	nA
				Full	–3		3	
DYNAMIC								
t_{ON}	Turn-on time	V_{NO}, V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 14		25 °C		6	18	ns
				Full			20	
t_{OFF}	Turn-off time	V_{NO}, V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 14		25 °C		5	10	ns
				Full			12	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF, See Figure 15		25 °C		3.2		pC
$C_{NO(OFF)}$	NO OFF capacitance	f = 1 MHz, See Figure 16		25 °C		23		pF
$C_{COM(OFF)}$	COM OFF capacitance	f = 1 MHz, See Figure 16		25 °C		20		
$C_{COM(ON)}$	COM ON capacitance	f = 1 MHz, See Figure 16		25 °C		43		
BW	Bandwidth	R_L = 50 Ω, Switch ON		25 °C		123		MHz
O_{ISO}	OFF isolation(5)	R_L = 50 Ω, C_L = 5 pF, See Figure 17	f = 10 MHz	25 °C		–61		dB
			f = 100 MHz			–36		
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF, See Figure 17	f = 10 MHz	25 °C		–95		dB
			f = 100 MHz			–73		
THD	Total harmonic distortion	f = 20 Hz to 20 kHz, V_{COM} = 2 V_{P-P}	R_L = 32 Ω	25 °C		0.14%		
			R_L = 600 Ω			0.013%		
DIGITAL CONTROL INPUTS (IN1, IN2)								
V_{IH}	Input logic high			Full	1			V
V_{IL}	Input logic low			Full			0.4	
I_{IN}	Input leakage current	V_I = 0 or V_{CC}		25 °C		0.1	5	nA
				Full	–10		10	
SUPPLY								
V_{CC}	Power-supply range				1.65		1.95	V
I_{CC}	Positive-supply current	V_I = 0 or V_{CC}		25 °C			0.05	μA
				Full			0.5	

(1) $\Delta R_{on} = R_{on(max)} - R_{on(min)}$
(2) Typical values are at T_A = 25°C.
(3) Flatness is defined as the difference between the maximum and minimum value of r_{on} as measured over the specified analog signal ranges.
(4) Leakage parameters are 100% tested at the maximum-rated hot operating temperature and specified by correlation at T_A = 25°C.
(5) OFF isolation = $20_{log}10$ (V_{COM}/V_{NO}), V_{COM} = output, V_{NO} = input to OFF switch

6.7 Typical Characteristics

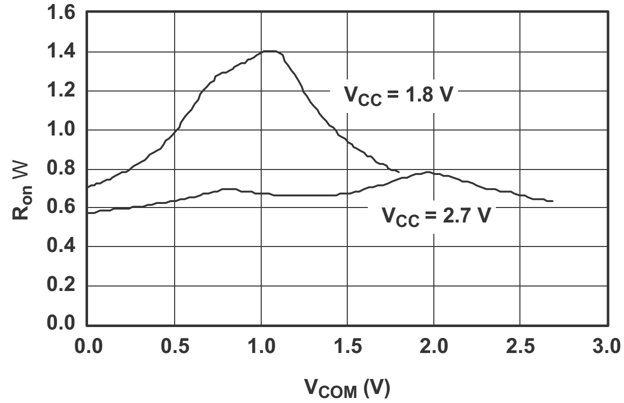


Figure 1. R_{on} vs V_{COM}

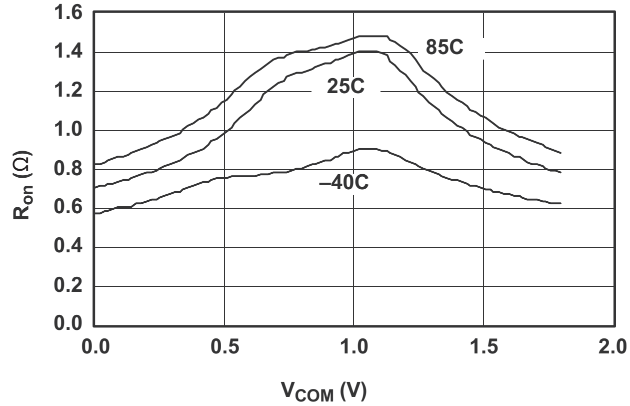


Figure 2. R_{on} vs V_{COM} (V_{CC} = 1.8 V)

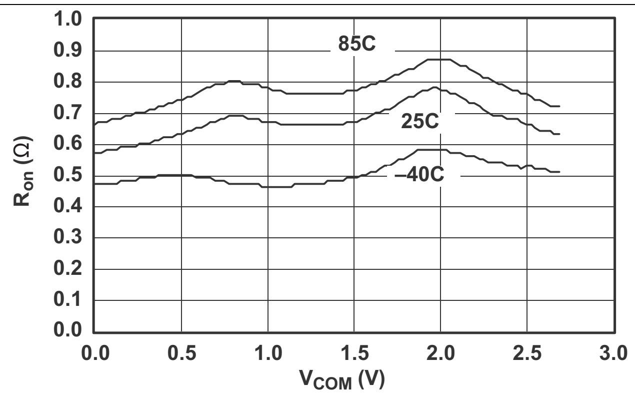


Figure 3. R_{on} vs V_{COM} (V_{CC} = 2.7 V)

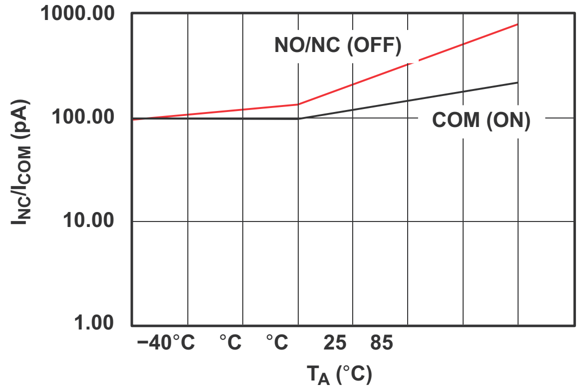


Figure 4. I_{ON} and I_{OFF} vs Temperature (V_{CC} = 3.6 V)

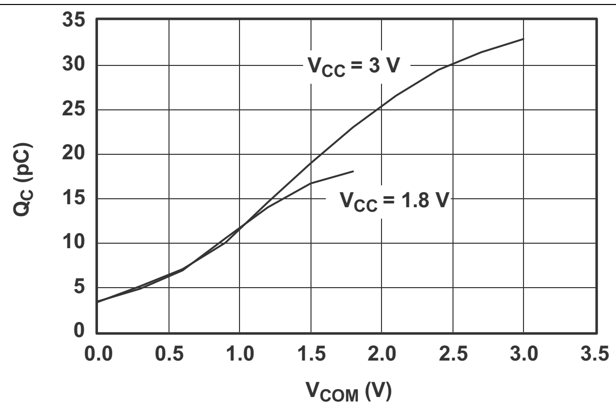


Figure 5. Q_C vs V_{COM}

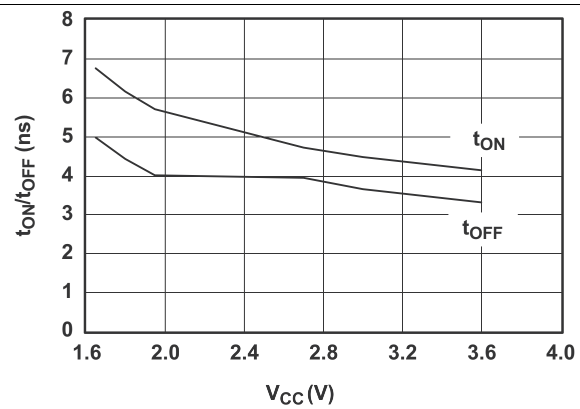


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

Typical Characteristics (continued)

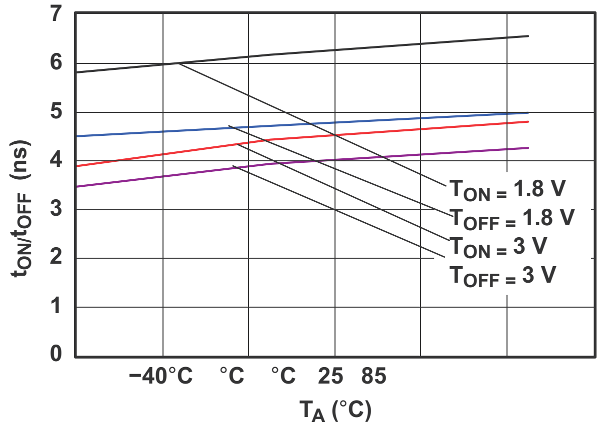


Figure 7. t_{ON} and t_{OFF} vs Temperature

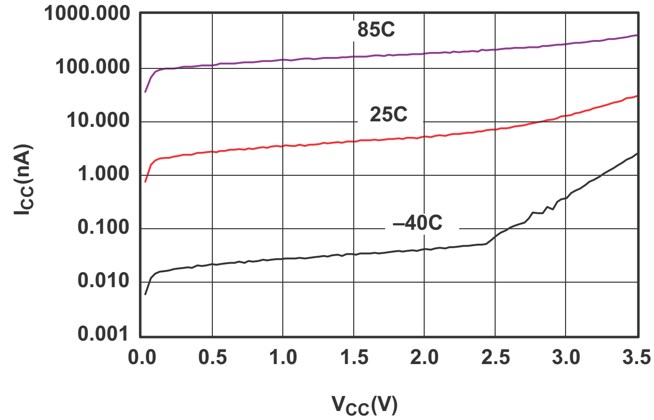


Figure 8. I_{CC} vs V_{CC}

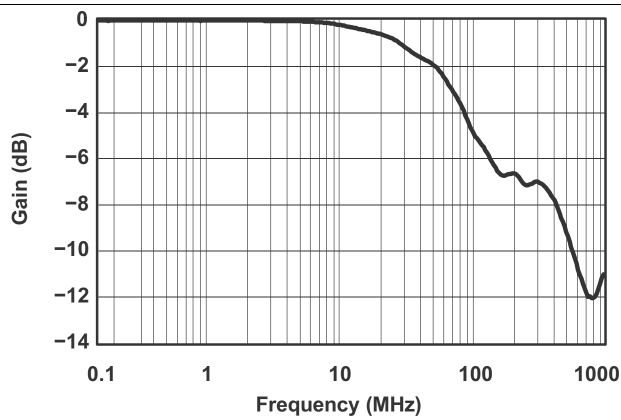


Figure 9. Gain vs Frequency (V_{CC} = 3 V)

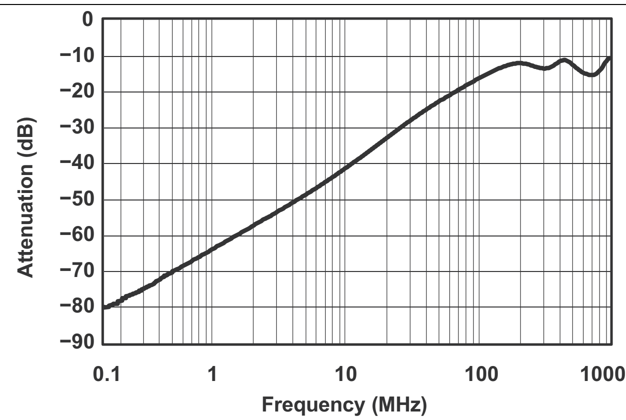


Figure 10. OFF Isolation vs Frequency (V_{CC} = 3 V)

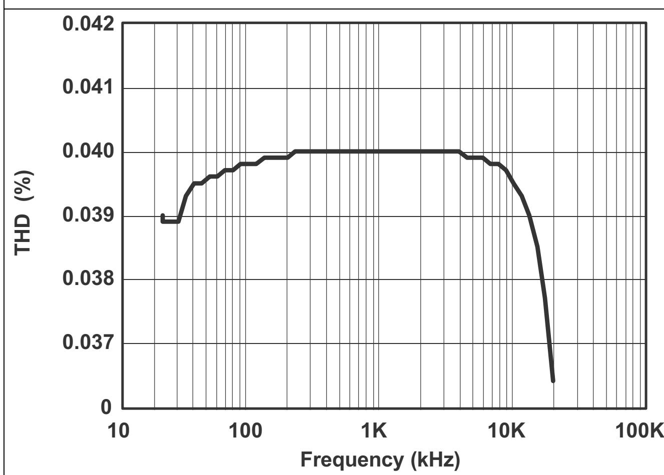


Figure 11. Total Harmonic Distortion vs Frequency (R_L = 32 Ω)

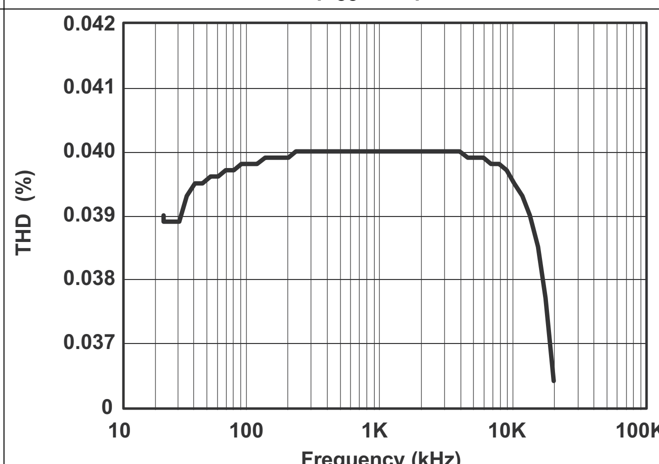


Figure 12. Total Harmonic Distortion vs Frequency (R_L = 600 Ω)

Typical Characteristics (continued)

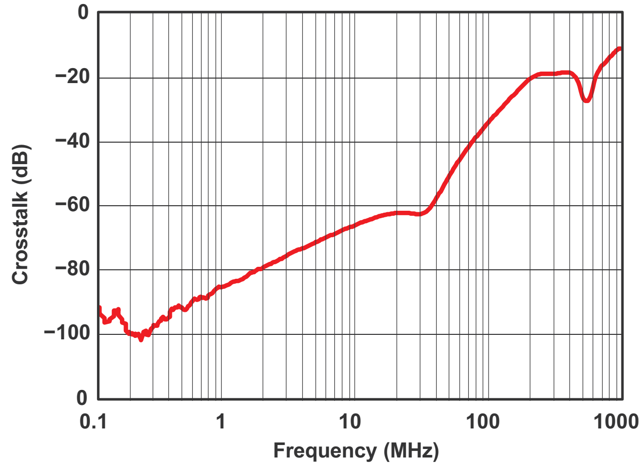


Figure 13. Crosstalk vs Frequency
(V_{CC} = 3 V)

7 Parameter Measurement Information

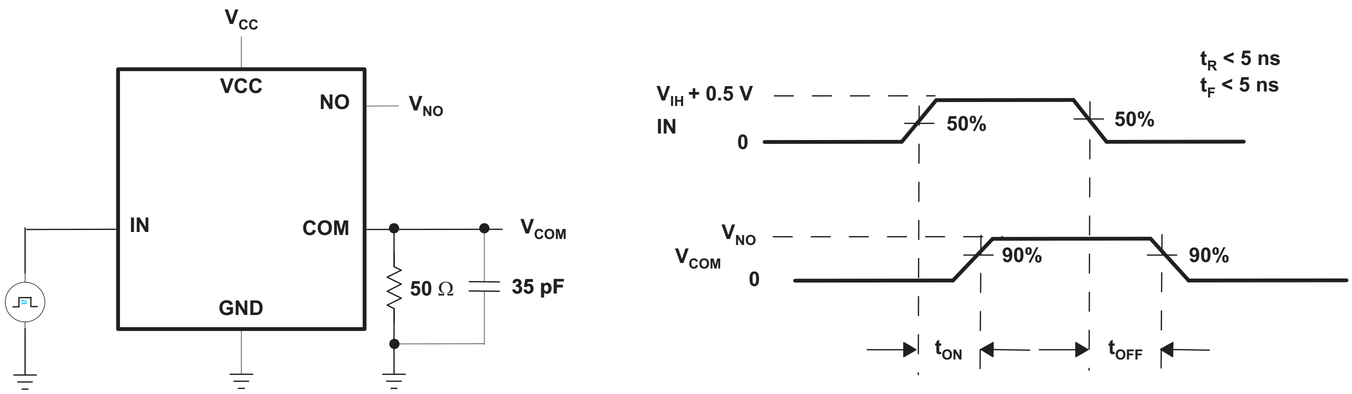


Figure 14. Switching Times

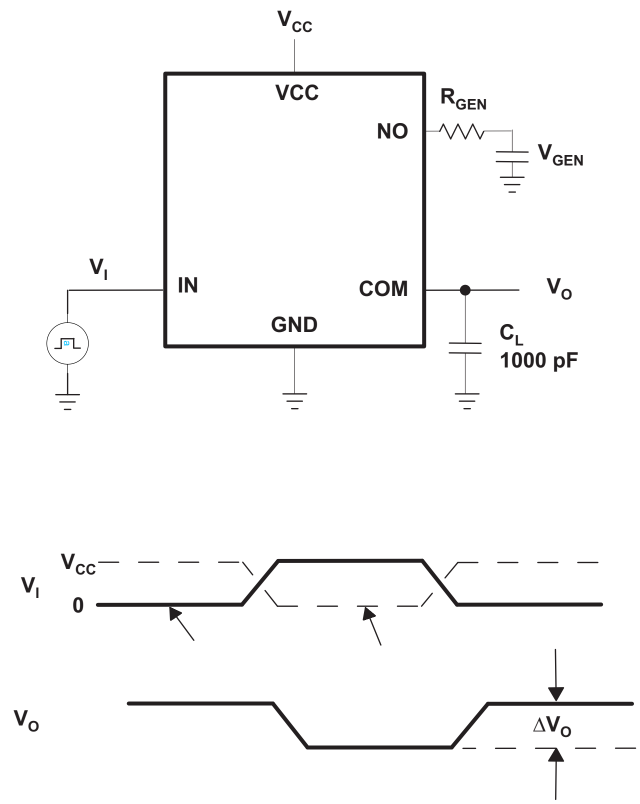


Figure 15. Charge Injection (Q_C)

Parameter Measurement Information (continued)

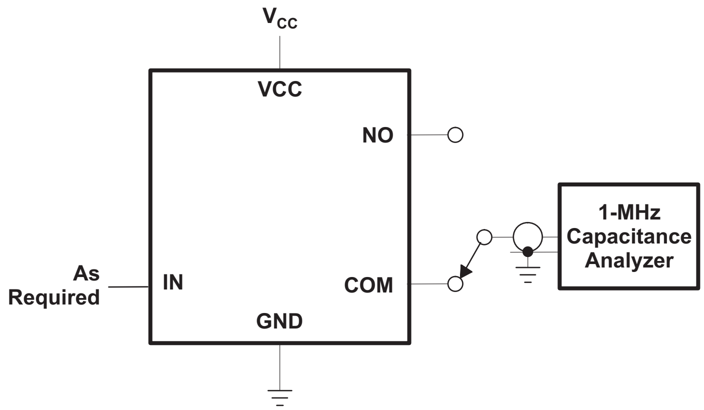


Figure 16. NO and COM Capacitance

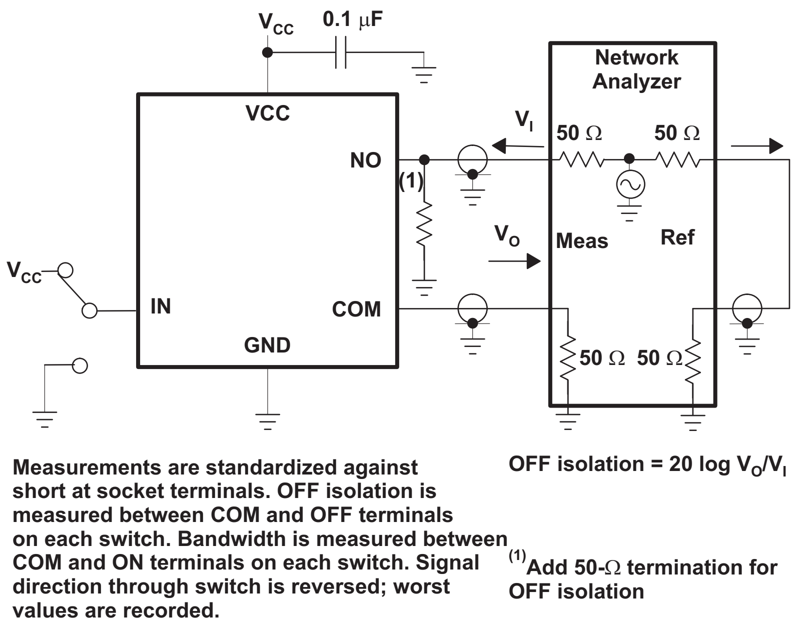
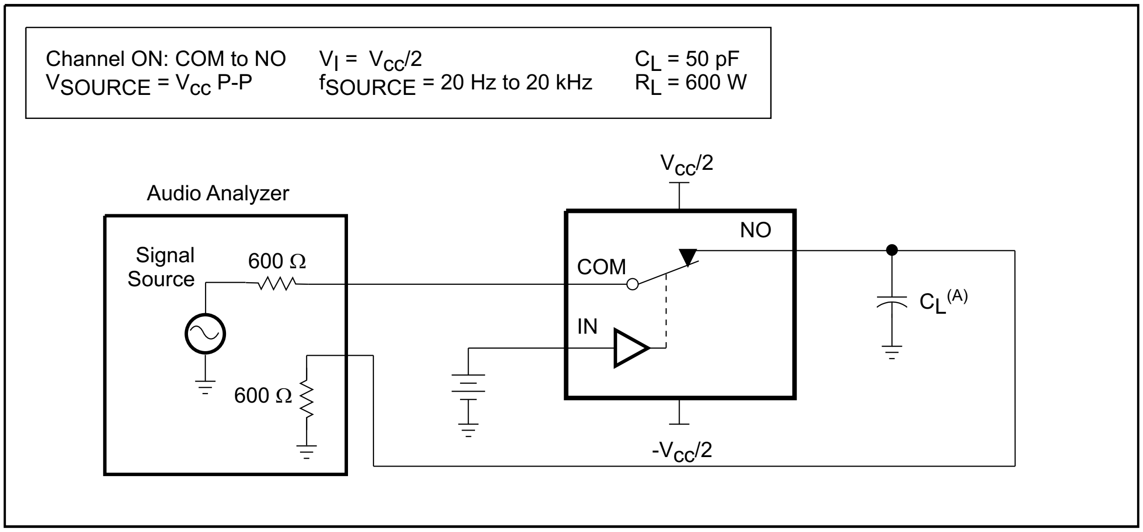


Figure 17. OFF Isolation, Bandwidth, and Crosstalk

Parameter Measurement Information (continued)



A. C_L includes probe and jig capacitance.

Figure 18. Total Harmonic Distortion (THD)

8 Detailed Description

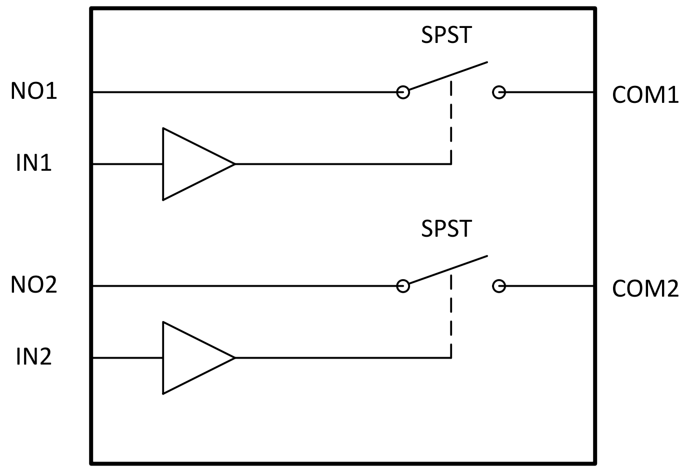
8.1 Overview

The TS3A4741 and TS3A4742 are bi-directional, 2-channel single-pole/single-throw (SPST) analog switches with low ON-state resistance (R_{on}), low-voltage, that operate from a single 1.6-V to 3.6-V supply. These devices have fast switching speeds, handle rail-to-rail analog signals, and consume very low quiescent power.

The digital logic input is 1.8-V CMOS compatible when using a single 3-V supply.

The TS3A4741 has two normally open (NO) switches, and the TS3A4742 has two normally closed (NC) switches.

8.2 Functional Block Diagram



8.3 Feature Description

The TS3A4741 and TS3A4742 has a low on resistance and high current handling capability up to 100 mA continuous current so it can be used for power sequencing and routing with minimal losses. The switch is also bi-directional with fast switching times in the 10 ns range which allows data acquisition and communication between multiple devices.

With a 3-V supply these devices are compatible with standard 1.8-V CMOS logic.

8.4 Device Functional Modes

Table 1. Function Table

IN	NO to COM, COM to NO (TS3A4741)	NC to COM, COM to NC (TS3A4742)
L	OFF	ON
H	ON	OFF

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Analog signals that range over the entire supply voltage (V_{CC} to GND) of the TS3A4741 and TS3A4742 can be passed with very little change in R_{on} (see *Typical Characteristics*). The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs.

9.2 Typical Application

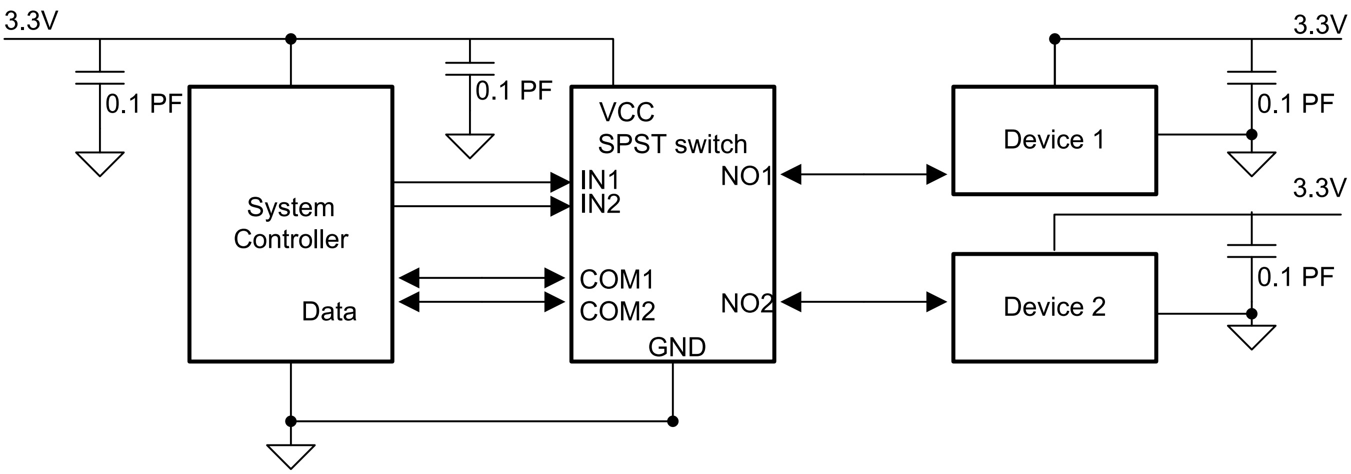


Figure 19. Typical Application Schematic

9.2.1 Design Requirements

Ensure that all of the signals passing through the switch are within the specified ranges to ensure proper performance.

9.2.2 Detailed Design Procedure

The TS3A474x can be properly operated without any external components. However, TI recommends that unused pins should be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device. TI also recommends that the digital control pins (INx) be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

Typical Application (continued)

9.2.3 Application Curve

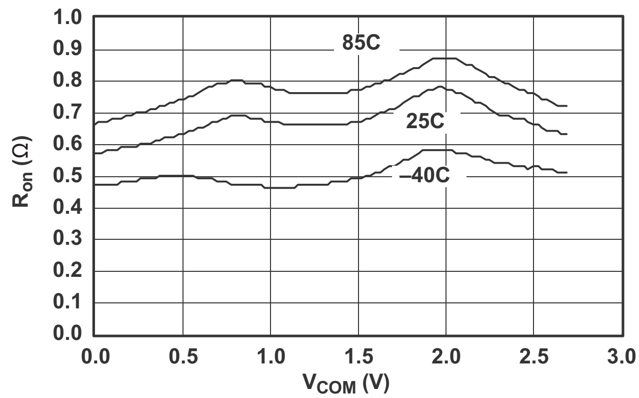


Figure 20. R_{on} vs V_{COM} (V_{CC} = 2.7 V)

10 Power Supply Recommendations

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence VCC on first, followed by NO, NC, or COM.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components. A 0.1-μF capacitor, connected from VCC to GND, is adequate for most applications.

11 Layout

11.1 Layout Guidelines

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

11.2 Layout Example

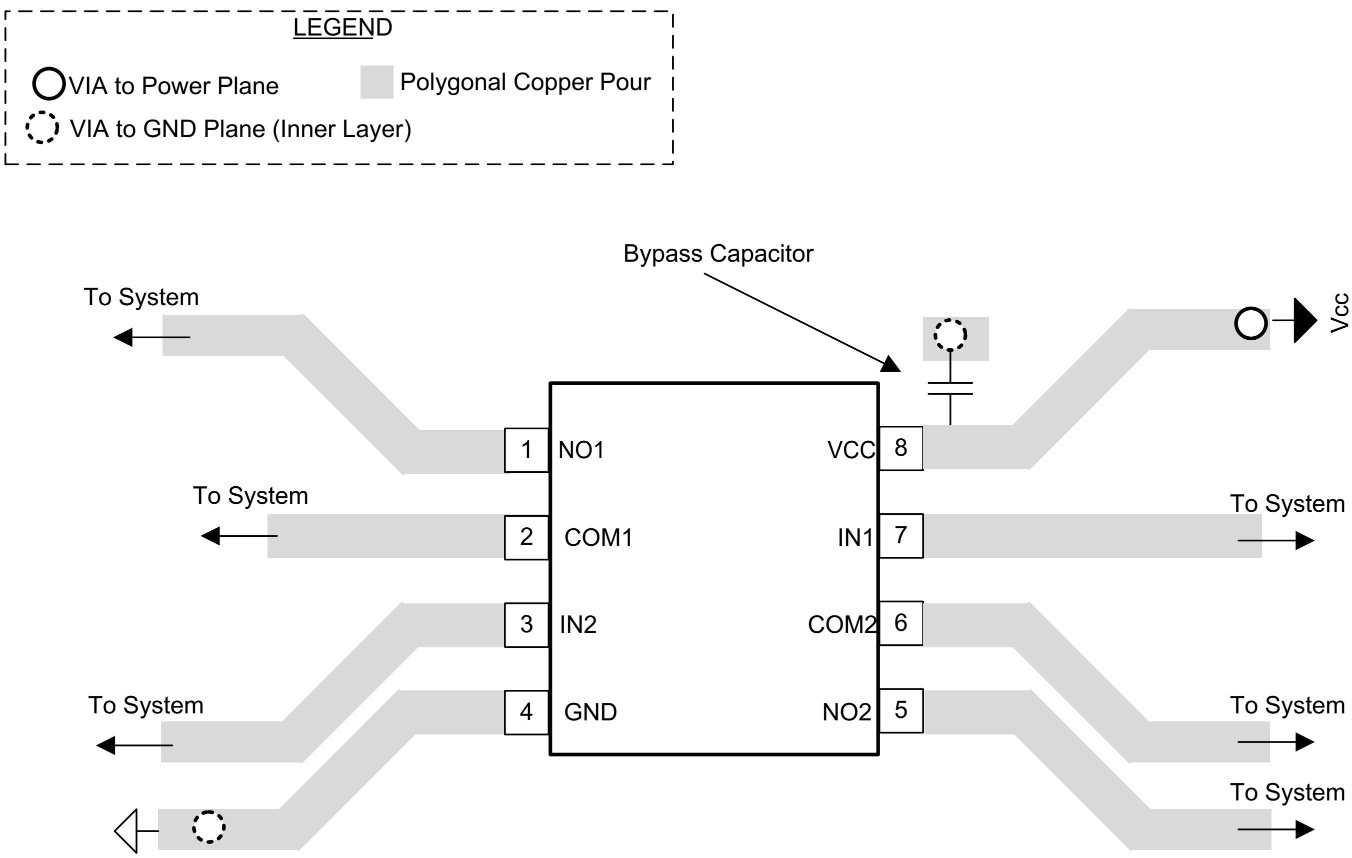


Figure 21. PCB Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TS3A4741	Click here	Click here	Click here	Click here	Click here
TS3A4742	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A4741DCNR	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(8BLO ~ 8BLR)	Samples
TS3A4741DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	JYR	Samples
TS3A4742DCNR	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	8BPR	Samples
TS3A4742DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	L7R	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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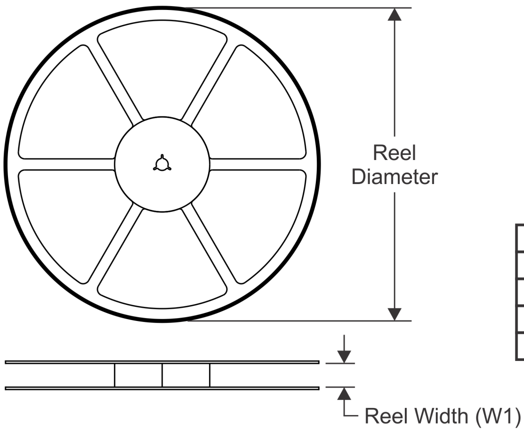
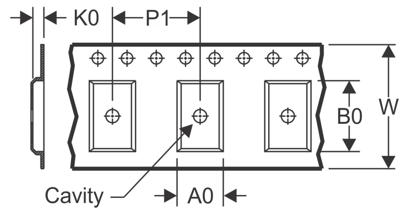
TAPE AND REEL INFORMATION

REEL DIMENSIONS

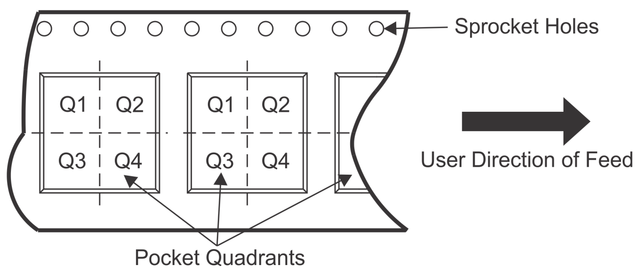


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

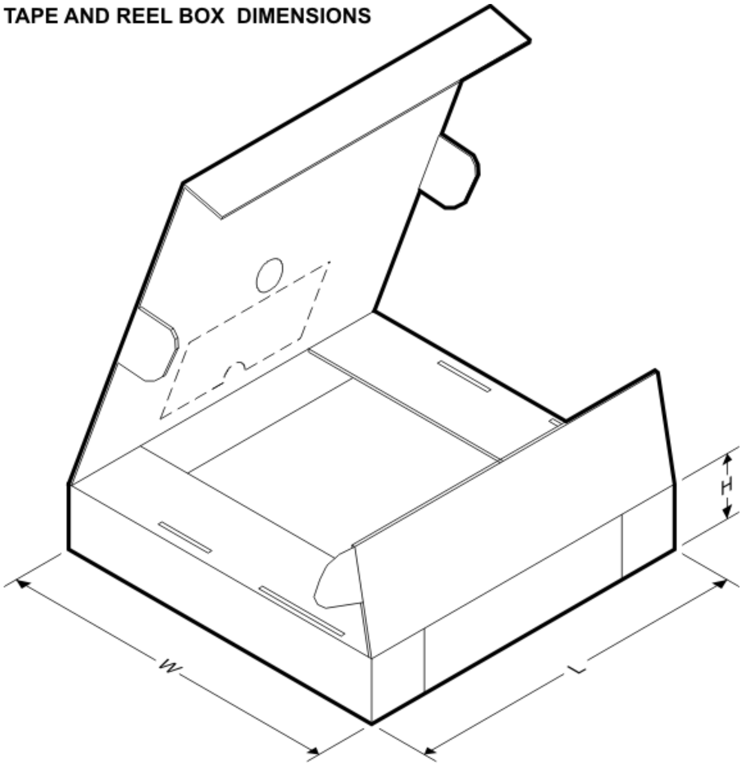
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A4741DCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS3A4741DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS3A4742DCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS3A4742DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

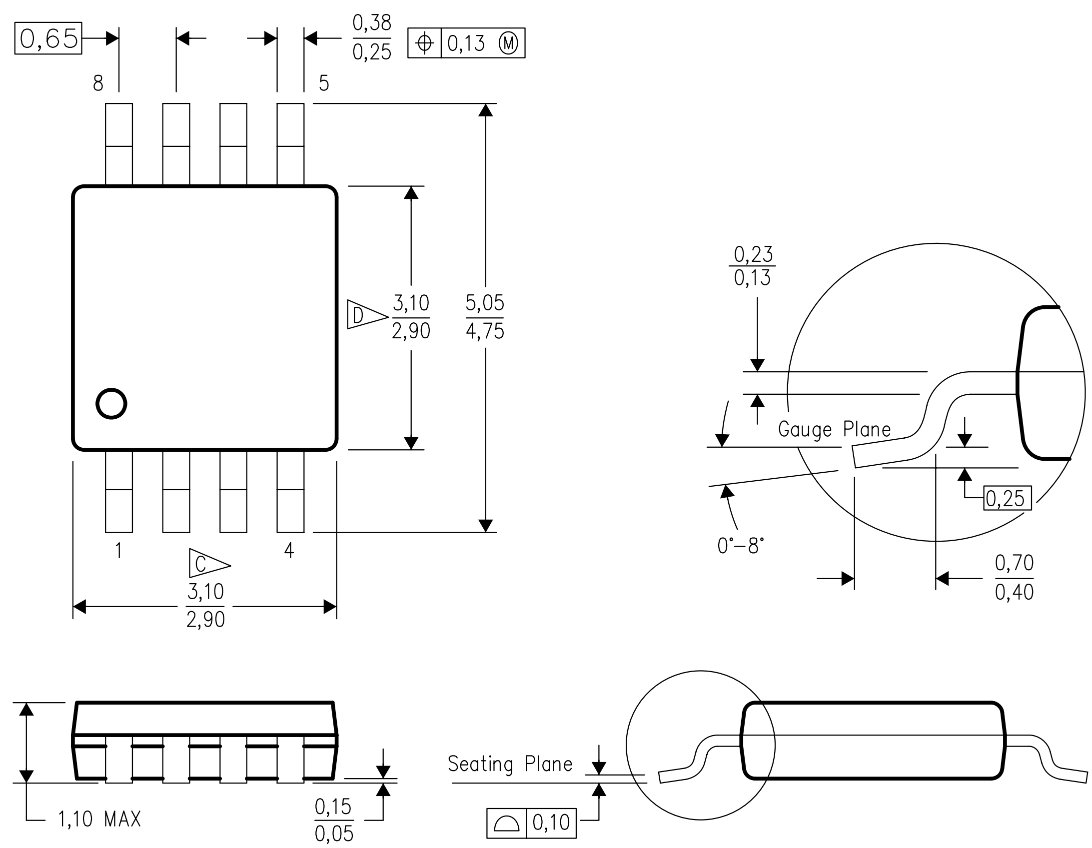
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A4741DCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TS3A4741DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TS3A4742DCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TS3A4742DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



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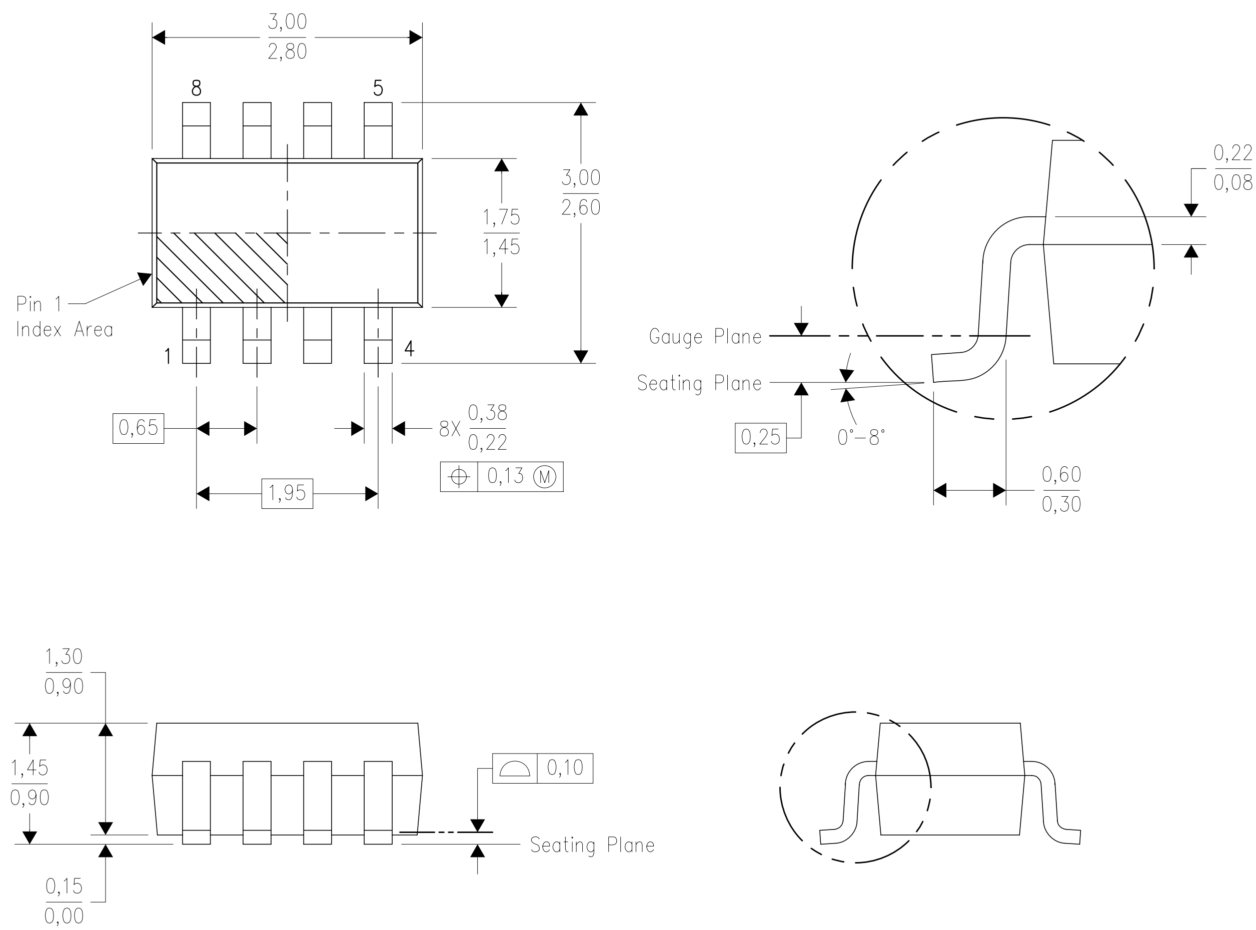
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO–187 variation AA, except interlead flash.

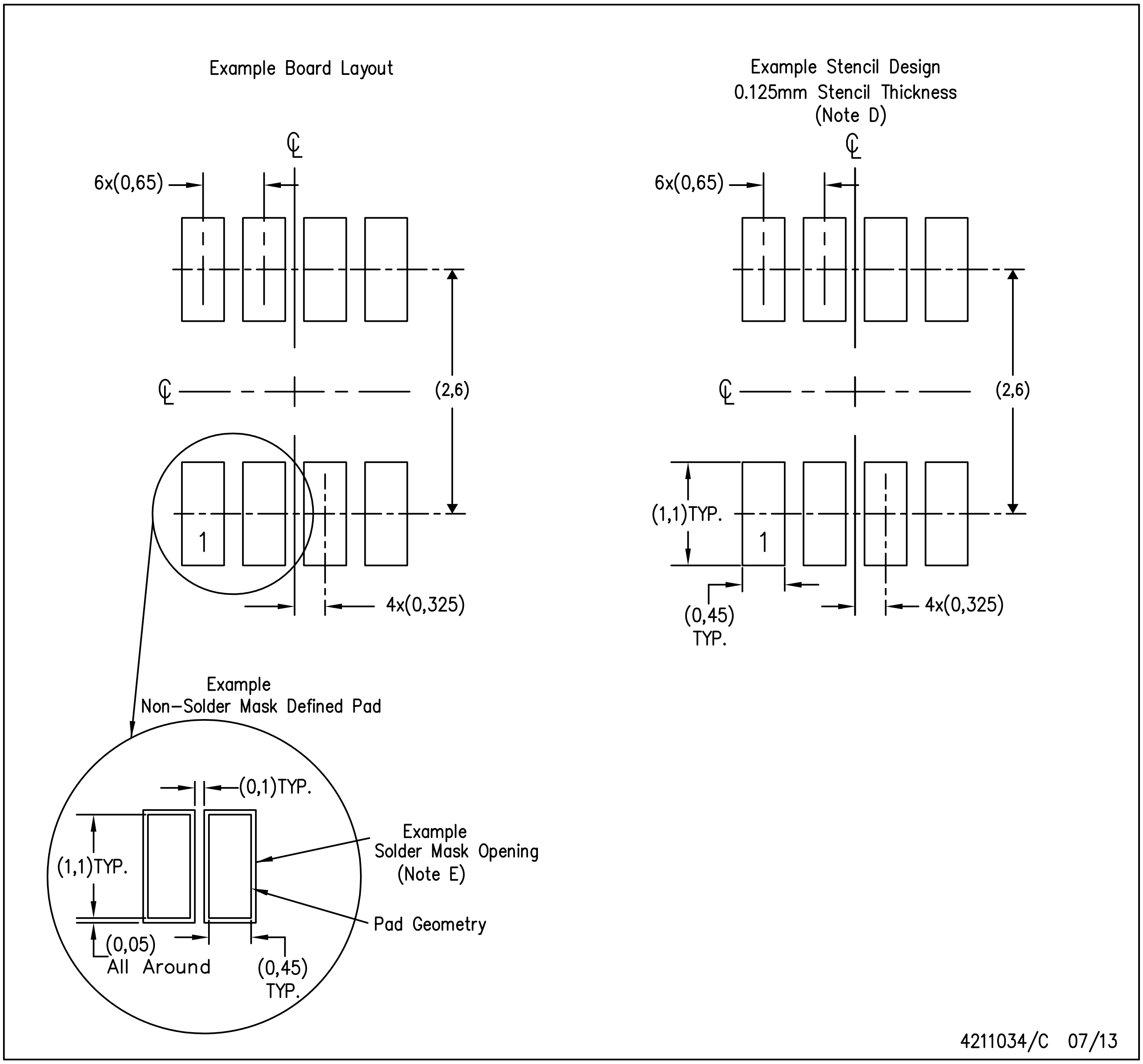
DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



4202106/D 11/2009

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
- D. Package outline inclusive of solder plating.
- E. A visual index feature must be located within the Pin 1 index area.
- F. Falls within JEDEC MO–178 Variation BA.
- G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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