TEXAS INSTRUMENTS

SN54AHC574, **SN74AHC574**

SCLS244J – OCTOBER 1995 – REVISED DECEMBER 2014

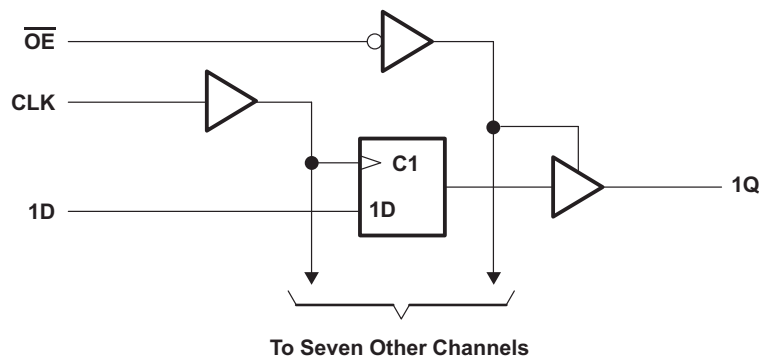# SNx4AHC574 Octal Edge-Triggered D-Type Flip-Flops With 3-State Outputs

1 Features

- Operating Range 2-V to 5.5-V V_{CC}
- 3-State Outputs Drive Bus Lines Directly
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 200-V Machine Model
  - 1000-V Charged-Device Model

2 Applications

- Smart Grids
- TVs
- Set Top Boxes
- Audio
- Servers
- Surveillance Cameras
- Network Switches
- Infotainment

3 Description

The SNx4AHC574 devices are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4AHC574	SSOP (20)	7.50 mm × 5.30 mm
	TVSOP (20)	5.00 mm × 4.40 mm
	SOIC (20)	12.80 mm × 7.50 mm
	PDIP (20)	25.40 mm × 6.35 mm
	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

To Seven Other Channels

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5 Revision History

Changes from Revision I (July 2003) to Revision J **Page**

6 Pin Configuration and Functions

SN54AHC574 . . . J OR W PACKAGE
SN74AHC574 . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)

OE	1	20	V_CC
1D	2	19	1Q
2D	3	18	2Q
3D	4	17	3Q
4D	5	16	4Q
5D	6	15	5Q
6D	7	14	6Q
7D	8	13	7Q
8D	9	12	8Q
GND	10	11	CLK
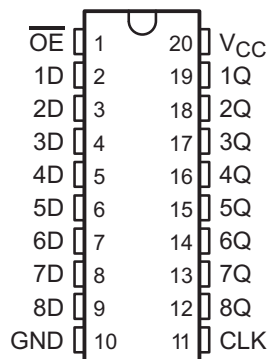
SN54AHC574 . . . FK PACKAGE
(TOP VIEW)

Top pins: 2D, 1D, OE, V_CC, 1Q (3, 2, 1, 20, 19)
Left: 3D 4, 4D 5, 5D 6, 6D 7, 7D 8
Right: 2Q 18, 3Q 17, 4Q 16, 5Q 15, 6Q 14
Bottom: 8D 9, GND 10, CLK 11, 8Q 12, 7Q 13
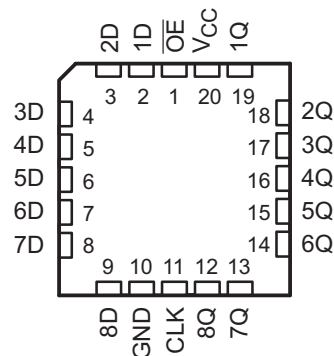
Pin Functions

PIN NO.	NAME	TYPE	DESCRIPTION
1	OE	I	Output Enable Pin
2	1D	I	1D Input
3	2D	I	2D Input
4	3D	I	3D Input
5	4D	I	4D Input
6	5D	I	5D Input
7	6D	I	6D Input
8	7D	I	7D Input
9	8D	I	8D Input
10	GND	—	Ground Pin
11	CLK	I	Clock Pin
12	8Q	O	8Q Output
13	7Q	O	7Q Output
14	6Q	O	6Q Output
15	5Q	O	5Q Output
16	4Q	O	4Q Output
17	3Q	O	3Q Output
18	2Q	O	2Q Output
19	1Q	O	1Q Output
20	V_CC	—	Power Pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I	Input voltage range[2]		−0.5	7	V
V_O	Output voltage range[2]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±75	mA
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	1000	
		Machine Model (MM)	200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			SN54AHC574 MIN	SN54AHC574 MAX	SN74AHC574 MIN	SN74AHC574 MAX	UNIT
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5		V
		$V_{CC} = 3$ V	2.1		2.1		
		$V_{CC} = 5.5$ V	3.85		3.85		
V_{IL}	Low-level Input voltage	$V_{CC} = 2$ V		0.5		0.5	V
		$V_{CC} = 3$ V		0.9		0.9	
		$V_{CC} = 5.5$ V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V		−50		−50	µA
		$V_{CC} = 3.3$ V ± 0.3 V		−4		−4	mA
		$V_{CC} = 5$ V ± 0.5 V		−8		−8	
I_{OL}	Low-level output current	$V_{CC} = 2$ V		50		50	µA
		$V_{CC} = 3.3$ V ± 0.3 V		4		4	mA
		$V_{CC} = 5$ V ± 0.5 V		8		8	
Δt/Δv	Input transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V		100		100	ns/V
		$V_{CC} = 5$ V ± 0.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

Product Folder Links: *SN54AHC574 SN74AHC574*

7.4 Thermal Information

THERMAL METRIC[1]		SN74AHC574						UNIT
		DB	DGV	DW	N	NS	PW	
		20 PINS						
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.9	117.2	79.4	53.3	79.2	103.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.6	32.7	45.7	40.0	45.7	37.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	53.1	58.7	46.9	34.2	46.8	54.3	
ψ_{JT}	Junction-to-top characterization parameter	21.3	1.15	18.7	26.4	19.3	2.9	
ψ_{JB}	Junction-to-board characterization parameter	52.7	58.0	46.5	34.1	46.4	53.8	

(1)   For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			SN54AHC574		SN74AHC574				UNIT
						−40°C to 85°C		−40°C to 85°C		−40°C to 125°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50$ μA	2 V	1.9	2		1.9		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		4.4		
	$I_{OH} = -4$ mA	3 V	2.58			2.48		2.48		2.48		
	$I_{OH} = -8$ mA	4.5 V	3.94			3.8		3.8		3.8		
V_{OL}	$I_{OL} = 50$ μA	2 V			0.1		0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1		0.1	
	$I_{OH} = 4$ mA	3 V			0.36		0.5		0.44		0.44	
	$I_{OH} = 8$ mA	4.5 V			0.36		0.5		0.44		0.44	
I_I	$V_I = 5.5$ V or GND	0 V to 5.5 V			±0.1		±1 [1]		±1		±1	μA
I_{OZ}[2]	$V_O = V_{CC}$ or GND V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25		±2.5		±2.5		±2.5	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40		40		40	μA
C_i	$V_I = V_{CC}$ or GND	5 V		3	10				10		10	pF
C_O	$V_O = V_{CC}$ or GND	5 V		3								pF

(1)   On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0$ V.
(2)   For input and output pins, I_{OZ} includes the input leakage current.

7.6 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER		$T_A = 25°C$		SN54AHC574		SN74AHC574				UNIT
				−40°C to 85°C		−40°C to 85°C		−40°C to 125°C		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low	5		5		5		5.5		ns
t_{su}	Setup time, data before CLK↑	3.5		3.5		3.5		4		ns
t_h	Hold time, data after CLK↑	1.5		1.5		1.5		2		ns

7.7 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER		T_A = 25°C		SN54AHC574		SN74AHC574				UNIT
				–40°C to 85°C		–40°C to 85°C		–40°C to 125°C		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low	5		5		5		5.5		ns
t_{su}	Setup time, data before CLK↑	3		3		3		3.5		ns
t_h	Hold time, data after CLK↑	1.5		1.5		1.5		2		ns

7.8 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC574		SN74AHC574				UNIT
							–40°C to 85°C		–40°C to 85°C		–40°C to 125°C		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{MAX}			C_L = 15 pF	80[1]	125[1]		65[1]		65		65		MHz
			C_L = 50 pF	50	75		45		45		45		
t_{PLH}	CLK	Q	C_L = 15 pF		8.5[1]	13.2[1]	1[1]	15.5[1]	1	15.5	1	17	ns
t_{PHL}					8.5[1]	13.2[1]	1[1]	15.5[1]	1	15.5	1	17	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF		8.2[1]	12.8[1]	1[1]	15[1]	1	15	1	16	ns
t_{PZL}					8.2[1]	12.8[1]	1[1]	15[1]	1	15	1	16	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF		8.5[1]	13[1]	1[1]	15[1]	1	15	1	16	ns
t_{PLZ}					8.5[1]	13[1]	1[1]	15[1]	1	15	1	16	
t_{PLH}	CLK	Q	C_L = 50 pF		11	16.7	1	19	1	19	1	20.5	ns
t_{PHL}					11	16.7	1	19	1	19	1	20.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		10.7	16.3	1	18.5	1	18.5	1	19.5	ns
t_{PZL}					10.7	16.3	1	18.5	1	18.5	1	19.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		11	15	1	17	1	17	1	18	ns
t_{PLZ}					11	15	1	17	1	17	1	18	
$t_{sk(o)}$			C_L = 50 pF			1.5[2]						1.5	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

Product Folder Links: *SN54AHC574 SN74AHC574*

7.9 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC574 −40°C to 85°C		SN74AHC574 −40°C to 85°C		SN74AHC574 −40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{MAX}			C_L = 15 pF	130[1]	180[1]		110[1]		110		110		MHz
			C_L = 50 pF	85	115		75		75		75		
t_{PLH}	CLK	Q	C_L = 15 pF		5.6[1]	8.6[1]	1[1]	10[1]	1	10	1	11	ns
t_{PHL}					5.6[1]	8.6[1]	1[1]	10[1]	1	10	1	11	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF		5.9[1]	9[1]	1[1]	10.5[1]	1	10.5	1	11.5	ns
t_{PZL}					5.9[1]	9[1]	1[1]	10.5[1]	1	10.5	1	11.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF		5.5[1]	9[1]	1[1]	10.5[1]	1	10.5	1	11.5	ns
t_{PLZ}					5.5[1]	9[1]	1[1]	10.5[1]	1	10.5	1	11.5	
t_{PLH}	CLK	Q	C_L = 50 pF		7.1	10.6	1	12	1	12	1	13	ns
t_{PHL}					7.1	10.6	1	12	1	12	1	13	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		7.4	11	1	12.5	1	12.5	1	13.5	ns
t_{PZL}					7.4	11	1	12.5	1	12.5	1	13.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		7.1	10.1	1	11.5	1	11.5	1	12.5	ns
t_{PLZ}					7.1	10.1	1	11.5	1	11.5	1	12.5	
$t_{sk(o)}$			C_L = 50 pF		1[2]					1		1	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

7.10 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C[1]

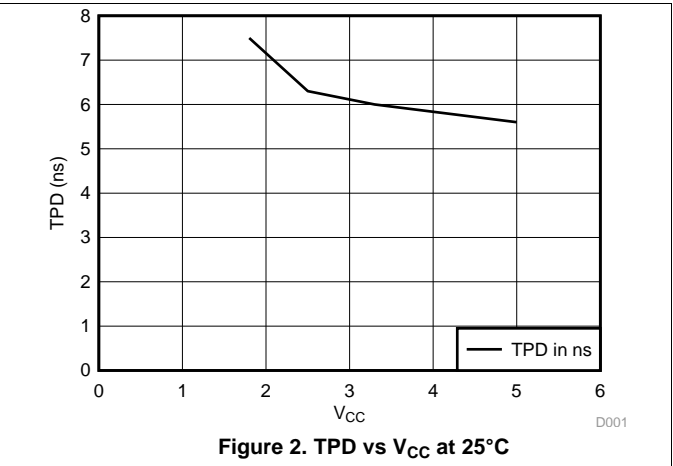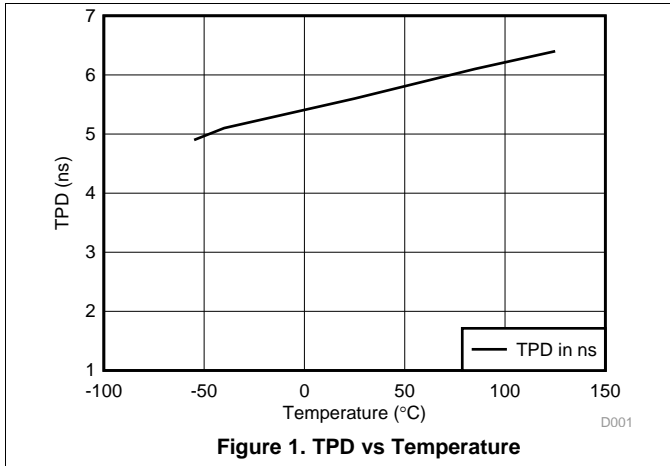| PARAMETER		SN74AHC574		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.2		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

(1) Characteristics are for surface-mount packages only.

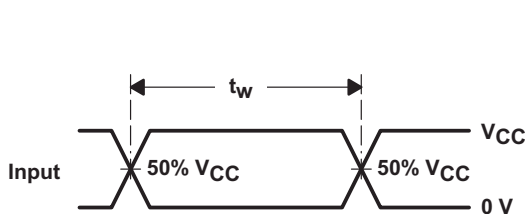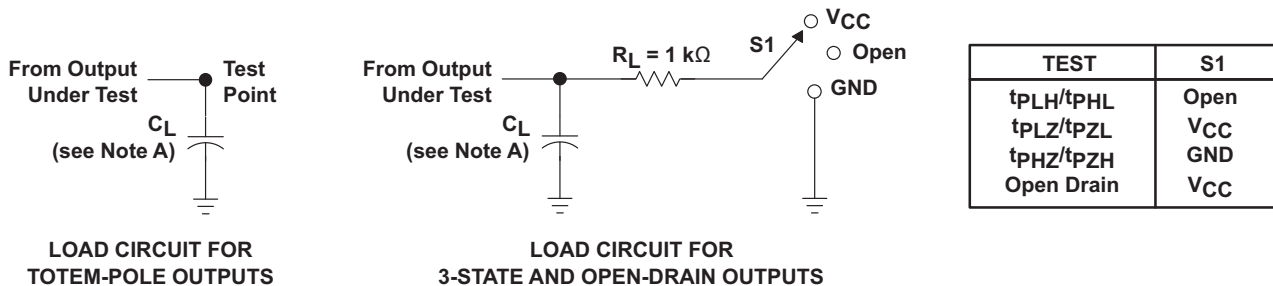## 7.11 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	28	pF

7.12 Typical Characteristics

Figure 1. TPD vs Temperature

Figure 2. TPD vs V$_{CC}$ at 25°C

Product Folder Links: *SN54AHC574 SN74AHC574*

8 Parameter Measurement Information
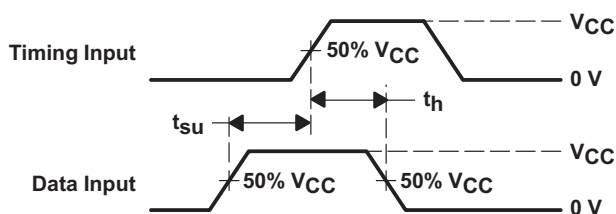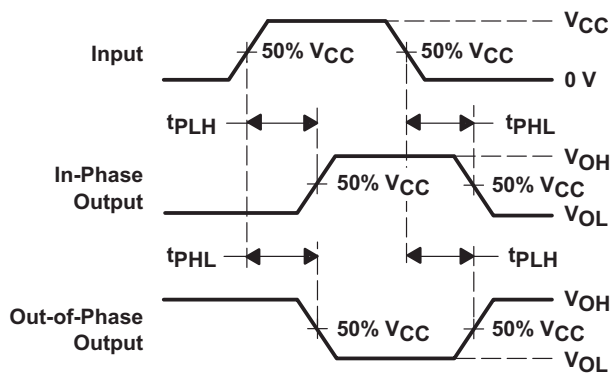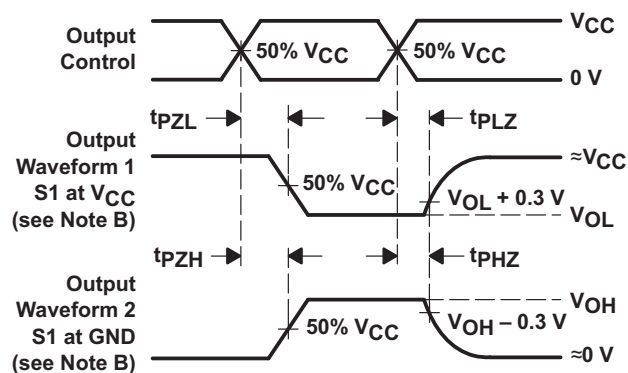
NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SNx4AHC574 devices are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

The states of the Q outputs are not predictable until the first valid clock.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pull-up components.

9.2 Functional Block Diagram

To Seven Other Channels
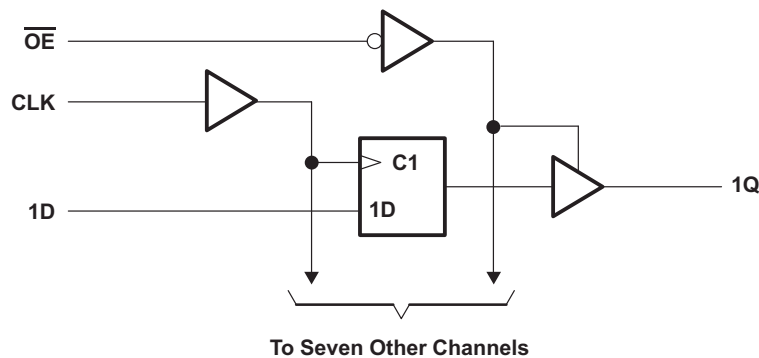
9.3 Feature Description

- 5.5-V tolerant input allows for 5 V to 3.3 V voltage translation
- Slow edges reduce output ringing

9.4 Device Functional Modes

Table 1. Function Table
(Each Flip-Flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

Product Folder Links: *SN54AHC574 SN74AHC574*

10 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

SN74AHC574 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid V_{CC} making it Ideal for down translation
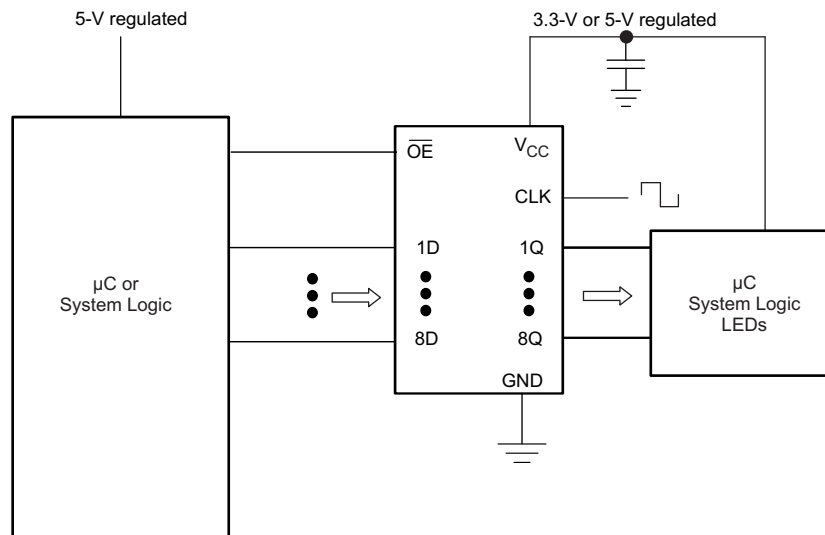
10.2 Typical Application

Figure 4. Typical Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   – For rise time and fall time specifications, see Δt/ΔV in the *Recommended Operating Conditions* table.
   – For specified High and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
2. Recommend Output Conditions
   – Load currents should not exceed 25 mA per output and 75 mA total for the part.
   – Outputs should not be pulled above V_{CC}.

Typical Application (continued)

10.2.3 Application Curves

Figure 5. Switching Charactersitics Comparison
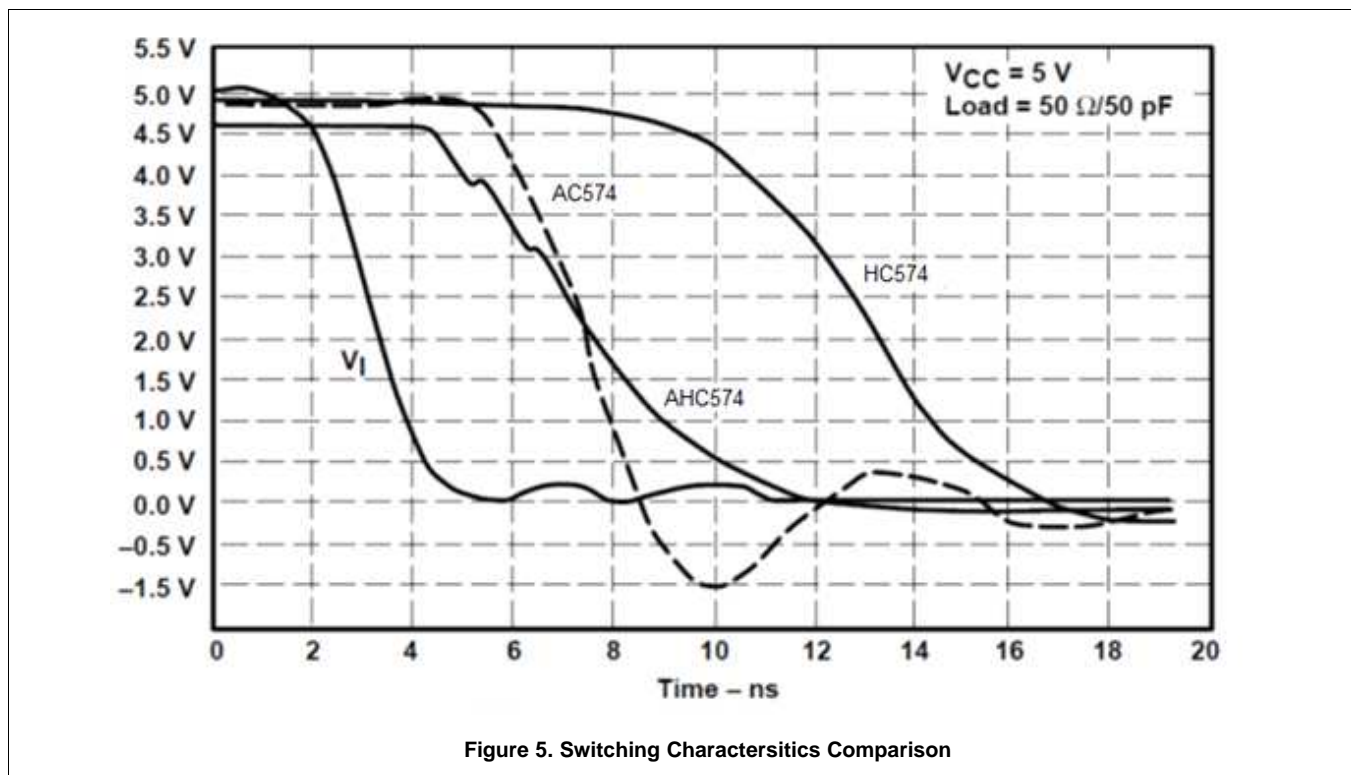
11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple V_{CC} pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

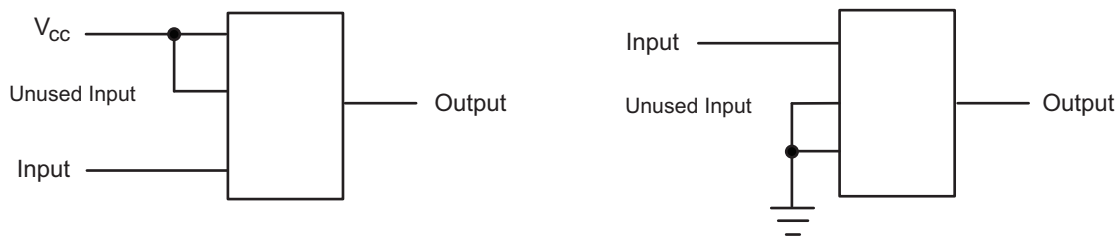# 12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 6 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

12.2 Layout Example

Figure 6. Layout Diagram

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

   This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TEXAS INSTRUMENTS

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9685401Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9685401Q2A SNJ54AHC 574FK	Samples
5962-9685401QRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9685401QR A SNJ54AHC574J	Samples
5962-9685401QSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9685401QS A SNJ54AHC574W	Samples
SN74AHC574DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574	Samples
SN74AHC574DGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574	Samples
SN74AHC574DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC574	Samples
SN74AHC574DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC574	Samples
SN74AHC574DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC574	Samples
SN74AHC574DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC574	Samples
SN74AHC574N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC574N	Samples
SN74AHC574NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC574	Samples
SN74AHC574PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574	Samples
SN74AHC574PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574	Samples
SN74AHC574PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574	Samples
SN74AHC574PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC574PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574	Samples
SNJ54AHC574FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9685401Q2A SNJ54AHC 574FK	Samples
SNJ54AHC574J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9685401QR A SNJ54AHC574J	Samples
SNJ54AHC574W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9685401QS A SNJ54AHC574W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC574, SN74AHC574 :

- Catalog: SN74AHC574

- Military: SN54AHC574

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC574DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHC574DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC574DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHC574NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	12.0	24.0	Q1
SN74AHC574PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC574DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74AHC574DGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74AHC574DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHC574NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AHC574PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

W (R−GDFP−F20)   CERAMIC DUAL FLATPACK

Base and Seating Plane

0.045 (1,14)
0.026 (0,66)

0.300 (7,62)
0.245 (6,22)

0.009 (0,23)
0.004 (0,10)

0.100 (2,45)
0.045 (1,14)

0.320 (8,13) MAX

1   20

0.022 (0,56)
0.015 (0,38)

0.540 (13,72) MAX

0.050 (1,27)

0.005 (0,13) MIN
4 Places

10   11

0.370 (9,40)
0.250 (6,35)

0.370 (9,40)
0.250 (6,35)

4040180−4/F   04/14

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only.
         E.   Falls within Mil−Std 1835 GDFP2−F20

FK (S−CQCC−N**)   LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

$\frac{0.020\ (0,51)}{0.010\ (0,25)}$

$\frac{0.020\ (0,51)}{0.010\ (0,25)}$

$\frac{0.080\ (2,03)}{0.064\ (1,63)}$

$\frac{0.055\ (1,40)}{0.045\ (1,14)}$

$\frac{0.045\ (1,14)}{0.035\ (0,89)}$

$\frac{0.028\ (0,71)}{0.022\ (0,54)}$

0.050 (1,27)

$\frac{0.045\ (1,14)}{0.035\ (0,89)}$

4040140/D 01/11

NOTES: A.   All linear dimensions are in inches (millimeters).
            B.   This drawing is subject to change without notice.
            C.   This package can be hermetically sealed with a metal lid.
            D.   Falls within JEDEC MS−004

TEXAS
INSTRUMENTS
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NS (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°–15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

0,40

0,23
0,13   ⊕   0,07 Ⓜ

24   13

4,50   6,60
4,30   6,20

1   12

A

0,16 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌒ 0,08

DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
   D. Falls within JEDEC: 24/48 Pins – MO-153
        14/16/20/56 Pins – MO-194

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PW (R-PDSO-G20)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ | 0,10 Ⓜ

20   11

D   4,50   6,60
     4,30   6,20

1   10

6,60
6,40

Ⓒ

0,15 NOM

Gage Plane

0°-8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

◯ | 0,10

4040064-5/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
        B. This drawing is subject to change without notice.
        Ⓒ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed 0,15 each side.
        D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
        E. Falls within JEDEC MO-153

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

1,55

5,6

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

0,3

1,6

Pad Geometry

0,07
All Around

4211284−5/G   08/15

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate design.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS
INSTRUMENTS
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DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

DIM \\ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
            B. This drawing is subject to change without notice.
            C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
            D. Falls within JEDEC MO-150

N (R-PDIP-T**)   PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

A — dimensions across top view

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) /D\

0.045 (1,14) / 0.030 (0,76) /D\

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option /D\

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E   12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
/C\ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
/D\ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

SOIC

20X (2)

SYMM

1

20

20X (0.6)

18X (1.27)

SYMM

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
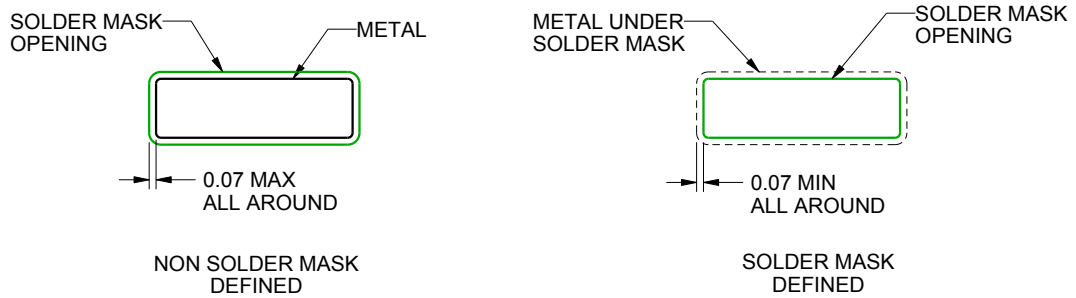
SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

20

SYMM

(9.3)

10

11

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE