

LP3470 Voltage Supervisor With Programmable Delay and 1% Reset Threshold

1 Features

- 5-Pin SOT-23 Package
- Open-Drain $\overline{\text{Reset}}$ Output
- Programmable Reset Time-Out Period Using an External Capacitor
- Immune to Short V_{CC} Transients
- $\pm 1\%$ Reset Threshold Accuracy Over Temperature
- Low Quiescent Current (16 μA typical)
- $\overline{\text{Reset}}$ Valid Down to $V_{\text{CC}} = 0.5\text{ V}$

2 Applications

- Critical μP and μC Power Monitoring
- Intelligent Instruments
- Computers
- Portable and Battery-Powered Equipment

3 Description

The LP3470 device is a micropower voltage supervisory circuit designed to monitor voltages within 1% of reset threshold over temperature. It provides maximum adjustability for power-on-reset (POR) and supervisory functions.

The LP3470 asserts a reset signal whenever the V_{CC} supply voltage falls below a reset threshold. The reset time-out period is adjustable using an external capacitor. Reset remains asserted for an interval (programmed by an external capacitor) after V_{CC} has risen above the threshold voltage.

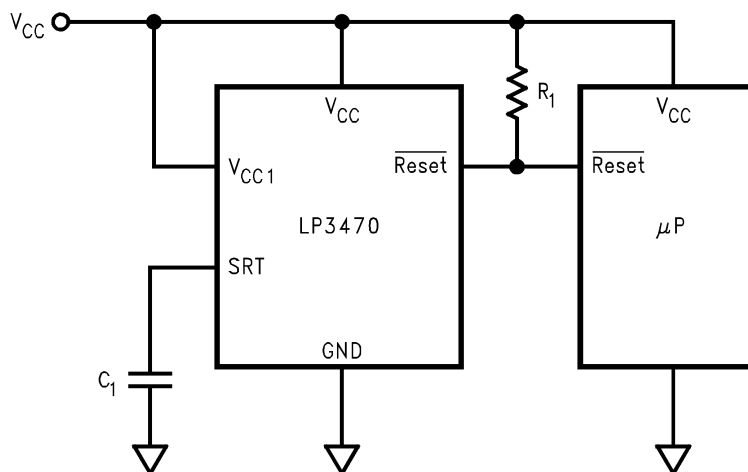
For information on available reset threshold voltage options, see [Mechanical, Packaging, and Orderable Information](#).

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP3470	SOT-23 (5)	1.60 mm x 2.90 mm

(1) For all available packages, see the Package Option Addendum at the end of the data sheet.

Basic Operating Circuit



Copyright © 2016, Texas Instruments Incorporated



Table of Contents

1 Features	1	7.3 Feature Description	8
2 Applications	1	7.4 Device Functional Modes	9
3 Description	1	8 Application and Implementation	10
4 Revision History	2	8.1 Application Information	10
5 Pin Configuration and Functions	3	8.2 Typical Application	10
6 Specifications	4	9 Power Supply Recommendations	12
6.1 Absolute Maximum Ratings	4	10 Layout	12
6.2 ESD Ratings	4	10.1 Layout Guidelines	12
6.3 Recommended Operating Conditions	4	10.2 Layout Example	12
6.4 Thermal Information	4	11 Device and Documentation Support	13
6.5 Electrical Characteristics	5	11.1 Community Resources	13
6.6 Typical Characteristics	6	11.2 Trademarks	13
7 Detailed Description	8	11.3 Electrostatic Discharge Caution	13
7.1 Overview	8	11.4 Glossary	13
7.2 Functional Block Diagram	8	12 Mechanical, Packaging, and Orderable Information	13

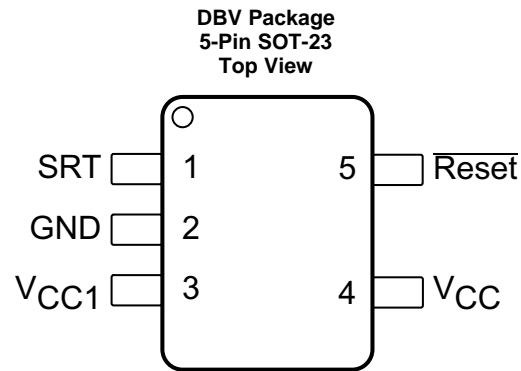
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (March 2013) to Revision G	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Moved <i>Operating temperature</i> parameters from <i>Absolute Maximum Ratings</i> to <i>Recommended Operating Conditions</i>	4

Changes from Revision E (September 2009) to Revision F	Page
• Changed layout of National Data Sheet to TI format	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SRT	O	Set reset time-out. Connect a capacitor between this pin and ground to select the reset time-out period (t_{RP}). $t_{RP} = 2000 \times C_1$ (C_1 in μF and t_{RP} in ms). If no capacitor is connected, leave this pin floating.
2	GND	—	Ground pin.
3	V_{CC1}	I	Always connect to pin V_{CC} (Pin 4).
4	V_{CC}	I	Supply voltage, and reset threshold monitor input.
5	$\overline{\text{Reset}}$	O	Open-drain, active-low reset output. Connect to an external pullup resistor. $\overline{\text{Reset}}$ changes from high to low whenever the monitored voltage (V_{CC}) drops below the reset threshold voltage (V_{RTH}). Once V_{CC} exceeds V_{RTH} , $\overline{\text{Reset}}$ remains low for the reset time-out period (t_{RP}) and then goes high.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

	MIN	MAX	UNIT
V _{CC} voltage	-0.3	6	V
Reset voltage	-0.3	6	V
Output current (Reset)		10	mA
Power dissipation (T _A = 25°C) ⁽³⁾		300	mW
Lead temperature (soldering, 5 sec)		260	°C
Junction temperature, T _{JMAX}		125	°C
Storage temperature, T _{stg}	-65	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is P_{Dmax} = (T_{Jmax} - T_A) / θ_{JA} or the number given in the *Absolute Maximum Ratings*, whichever is lower.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±200	

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC}	Operating voltage	0.5		5.5	V
T _A	Operating temperature	LP3470		85	°C
		LP3470I		85	

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LP3470	UNIT
		DBV (SOT-23)	
		5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	171	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	124.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	30.9	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	17.9	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	30.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	°C/W

- For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

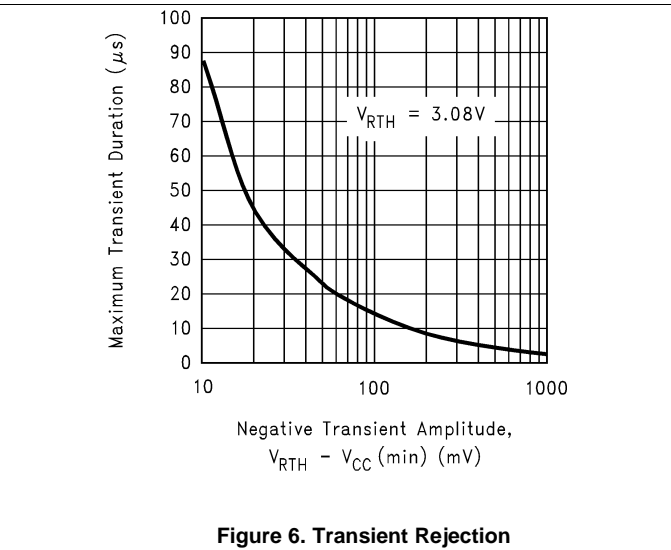
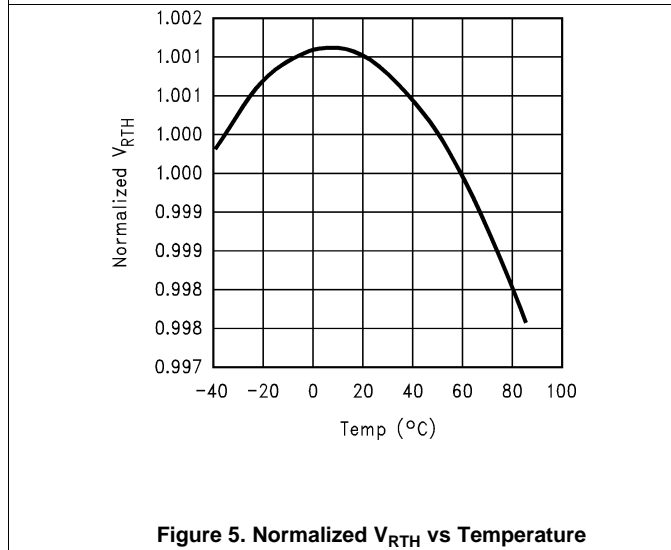
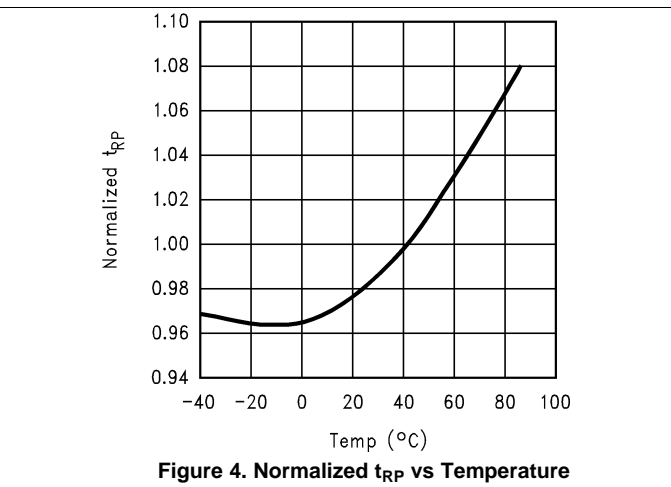
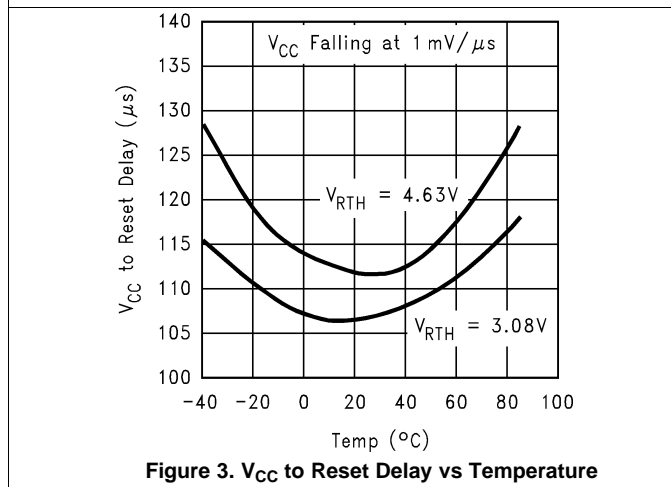
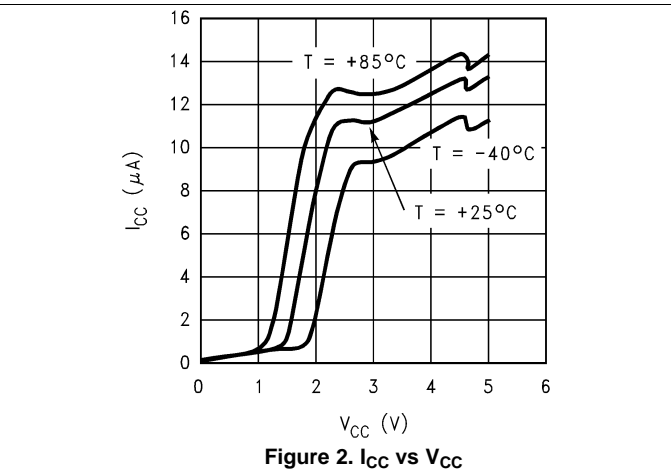
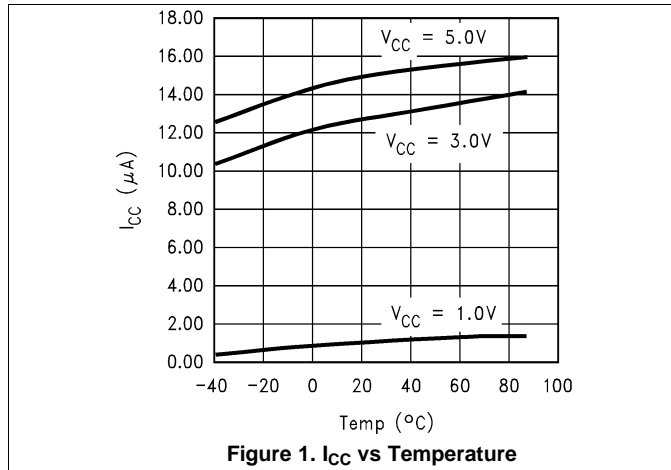
Limits and typical numbers are for $T_J = 25^\circ\text{C}$, and $V_{CC} = 2.4\text{ V to }5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN ⁽¹⁾	TYP ⁽²⁾	MAX ⁽¹⁾	UNIT
V_{CC}	Operating voltage	$T_J = -20^\circ\text{C to }85^\circ\text{C}$		0.5		5.5	V
I_{CC}	V_{CC} supply current	$V_{CC} = 4.5\text{ V}$	$T_J = 25^\circ\text{C}$	16			μA
			$T_J = -20^\circ\text{C to }85^\circ\text{C}$			30	
V_{RTH}	Reset threshold voltage	LP3470		$0.99 \times V_{RTH}$	V_{RTH}	$1.01 \times V_{RTH}$	V
		LP3470I	$T_J = 25^\circ\text{C}$	$0.99 \times V_{RTH}$	V_{RTH}	$1.01 \times V_{RTH}$	
			$T_J = -40^\circ\text{C to }85^\circ\text{C}$	$0.985 \times V_{RTH}$		$1.015 \times V_{RTH}$	
V_{HYST}	Hysteresis voltage ⁽³⁾	$T_J = 25^\circ\text{C}$		35			mV
		$T_J = -20^\circ\text{C to }85^\circ\text{C}$		15	65		
t_{PD}	V_{CC} to reset delay	V_{CC} falling at $1\text{ mV}/\mu\text{s}$	$T_J = 25^\circ\text{C}$	100			μs
			$T_J = -20^\circ\text{C to }85^\circ\text{C}$			300	
t_{RP}	Reset time-out period ⁽⁴⁾	$C_1 = 1\text{ nF}$	$T_J = 25^\circ\text{C}$	2			ms
			$T_J = -20^\circ\text{C to }85^\circ\text{C}$	1	3.5		
V_{OL}	Reset output voltage low	$V_{CC} = 0.5\text{ V}, I_{OL} = 30\text{ }\mu\text{A}, T_J = -20^\circ\text{C to }85^\circ\text{C}$				0.1	V
		$V_{CC} = 1\text{ V}, I_{OL} = 100\text{ }\mu\text{A}, T_J = -20^\circ\text{C to }85^\circ\text{C}$				0.1	
		$V_{CC} = V_{RTH} - 100\text{ mV}, I_{OL} = 4\text{ mA}, T_J = -20^\circ\text{C to }85^\circ\text{C}$				0.4	
R_1	External pullup resistor			0.68	20	68	k Ω
I_{LEAK}	Reset output leakage current	$T_J = 25^\circ\text{C}$		0.15		1	μA
		$T_J = -20^\circ\text{C to }85^\circ\text{C}$				6	

- (1) Minimum and maximum limits in standard typeface are 100% production tested at 25°C . Minimum and maximum limits in full operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
- (2) Typical numbers are at 25°C and represent the most likely parametric norm.
- (3) V_{HYST} affects the relation between V_{CC} and Reset as shown in the timing diagram.
- (4) t_{RP} is programmable by varying the value of the external capacitor (C_1) connected to pin SRT. The equation is: $t_{RP} = 2000 \times C_1$ (C_1 in μF and t_{RP} in ms).

6.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)



Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

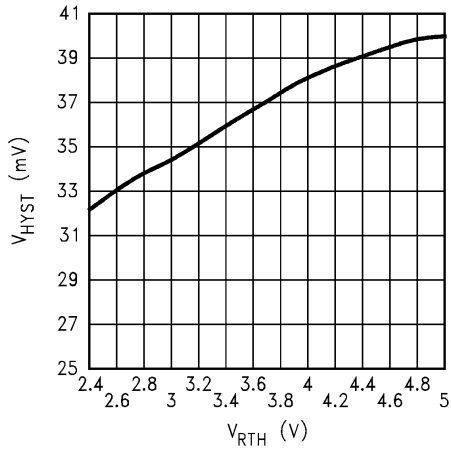


Figure 7. V_{HYST} vs V_{RTH}

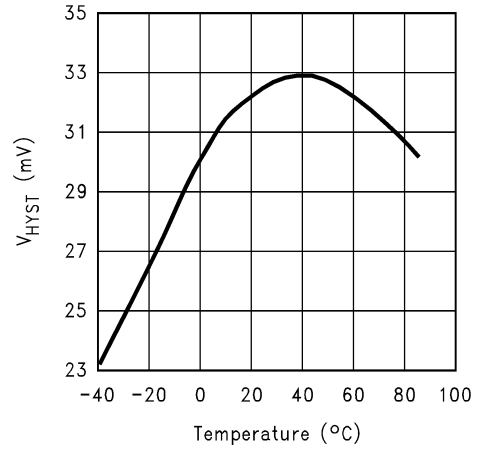


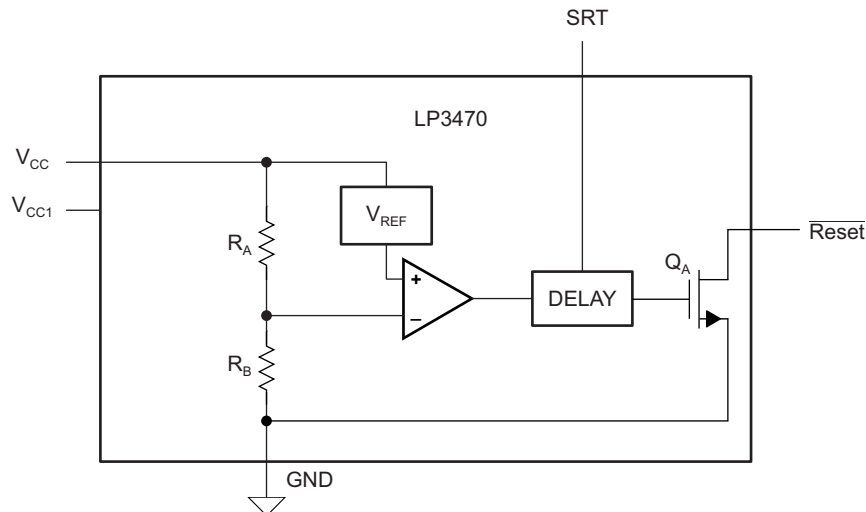
Figure 8. V_{HYST} vs Temperature

7 Detailed Description

7.1 Overview

The LP3470 micropower voltage supervisory circuit provides a simple solution to monitor the power supplies in microprocessor and digital systems and provides a reset controlled by the factory-programmed reset threshold on the V_{CC} supply voltage pin. When the voltage declines below the reset threshold, the reset signal is asserted and remains asserted for an interval programmed by an external capacitor after V_{CC} has risen above the threshold voltage. The reset threshold options are 2.63 V, 2.93 V, 3.08 V, 3.65 V, 4 V, 4.38 V, 4.63 V.

7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

7.3 Feature Description

7.3.1 $\overline{\text{Reset}}$ Time-Out Period

The reset time-out period (t_{RP}) is programmable using an external capacitor (C_1) connected to pin SRT of LP3470. A ceramic chip capacitor rated at or above 10 V is sufficient. The reset time-out period (t_{RP}) can be calculated using [Equation 1](#).

$$t_{RP} \text{ (ms)} = 2000 \times C_1 \text{ (\mu F)} \quad (1)$$

For example a C_1 of 100 nF will achieve a t_{RP} of 200 ms. If no delay due to t_{RP} is needed in a certain application, the pin SRT must be left floating.

7.3.2 $\overline{\text{Reset}}$ Output

In applications like microprocessor (μP) systems, errors might occur in system operation during power up, power down, or brownout conditions. It is imperative to monitor the power supply voltage to prevent these errors from occurring.

The LP3470 asserts a reset signal whenever the V_{CC} supply voltage is below a threshold (V_{RTH}) voltage. $\overline{\text{Reset}}$ is ensured to be a logic low for $V_{CC} > 0.5 \text{ V}$. Once V_{CC} exceeds the reset threshold, the reset is kept asserted for a time period (t_{RP}) programmed by an external capacitor (C_1); after this interval $\overline{\text{Reset}}$ goes to logic high. If a brownout condition occurs (monitored voltage falls below the reset threshold minus a small hysteresis), $\overline{\text{Reset}}$ goes low. When V_{CC} returns above the reset threshold, $\overline{\text{Reset}}$ remains low for a time period t_{RP} before going to logic high. [Figure 9](#) shows this behavior.

Feature Description (continued)

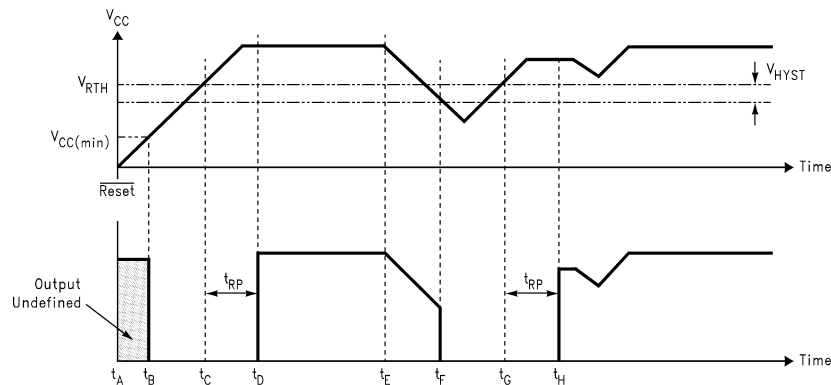


Figure 9. $\overline{\text{Reset}}$ Output Timing Diagram

7.3.3 Pullup Resistor Selection

The $\overline{\text{Reset}}$ output structure of the LP3470 is a simple open-drain N-channel MOSFET switch. A pullup resistor (R_1) must be connected to V_{CC} .

R_1 must be large enough to limit the current through the output MOSFET (Q_1) below 10 mA. A resistor value of more than 680 Ω ensures this. R_1 must also be small enough to ensure a logic high while supplying all the leakage current through the $\overline{\text{Reset}}$ pin. A resistor value of less than 68 k Ω satisfies this condition. A typical pullup resistor value of 20 k Ω is sufficient in most applications.

7.3.4 Negative-Going V_{CC} Transients

The LP3470 is relatively immune to short duration negative-going V_{CC} transients (glitches). The [Typical Characteristics](#) show the maximum transient duration versus negative transient amplitude (see [Figure 6](#)), for which reset pulses are not generated. This graph shows the maximum pulse width a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the transient amplitude increases (in other words, goes farther below the reset threshold), the maximum allowable pulse width decreases. A 0.1- μF bypass capacitor mounted close to V_{CC} provides additional transient immunity.

7.4 Device Functional Modes

7.4.1 $\overline{\text{Reset}}$ Output Low

When the V_{CC} supply voltage is below a threshold (V_{RTH}) voltage minus a hysteresis (V_{HYST}) voltage, the $\overline{\text{Reset}}$ pin will output logic low. Reset is ensured to be a logic low for $V_{CC} > 0.5$ V.

7.4.2 $\overline{\text{Reset}}$ Output High

When the V_{CC} supply voltage exceeds the reset threshold, the $\overline{\text{Reset}}$ is kept asserted for a time period (t_{RP}) programmed by an external capacitor (C_1); after this interval Reset goes to logic high.

8 Application and Implementation

NOTE

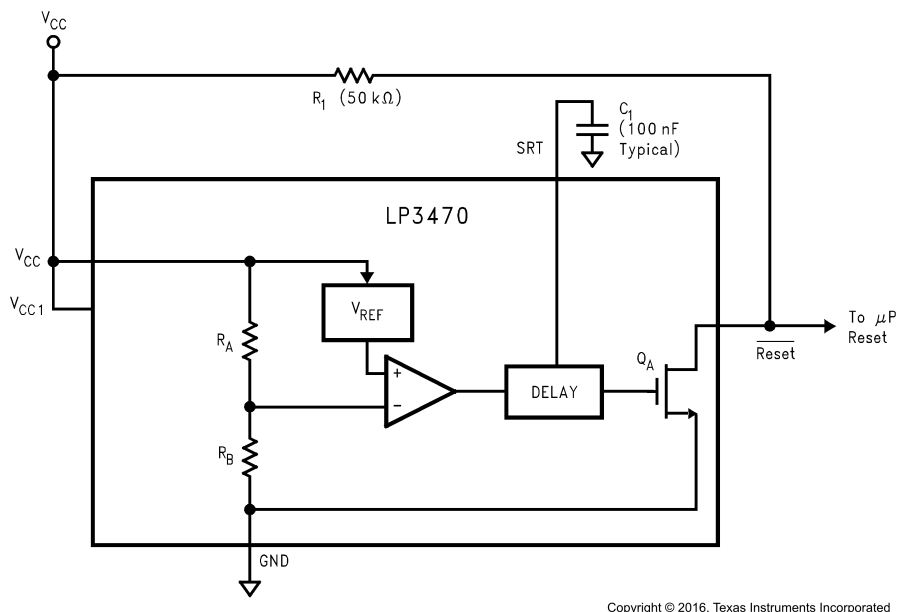
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP3470 is a micropower CMOS voltage supervisor that is ideal for use in battery-powered microprocessor and other digital systems. It is small in size and provides maximum adjustability for power-on-reset (POR) and supervisory functions, making it a good solution in a variety of applications. The LP3470 is available in six standard reset threshold voltage options, and the reset time-out period is adjustable using an external capacitor providing maximum flexibility in any application. This device can ensure system reliability and ensures that a connected microprocessor will operate only when a minimum V_{in} supply is satisfied.

8.2 Typical Application

The LP3470 can be used as a simple supervisor circuit to monitor the input supply to a microprocessor as shown in Figure 10.



Copyright © 2016, Texas Instruments Incorporated

Figure 10. Power-On Reset Circuit

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input supply voltage	0.5 to 5.5 V
Reset threshold voltage	2.63 V, 2.93 V, 3.08 V, 3.65 V, 4 V, 4.38 V, 4.63 V
External pullup resistor	0.68 to 68 kΩ
External reset time-out period capacitor	$C_1 = 1 \text{ nF}$
Reset time-out period	2 ms

8.2.2 Detailed Design Procedure

The minimum application circuit requires the LP3470 Power-On Reset Circuit IC and a pullup resistor connecting the reset pin to V_{CC} . The reset delay can be programmed with an additional capacitor connected from the SRT pin to GND. See [Reset Time-Out Period](#) and [Pullup Resistor Selection](#) for information on choosing specific values for components.

8.2.3 Application Curves

Two capacitor values for C_D (0.1 μF and 1 μF) are used as examples to show the programmability of the output time delay as shown in [Figure 11](#) and [Figure 12](#).

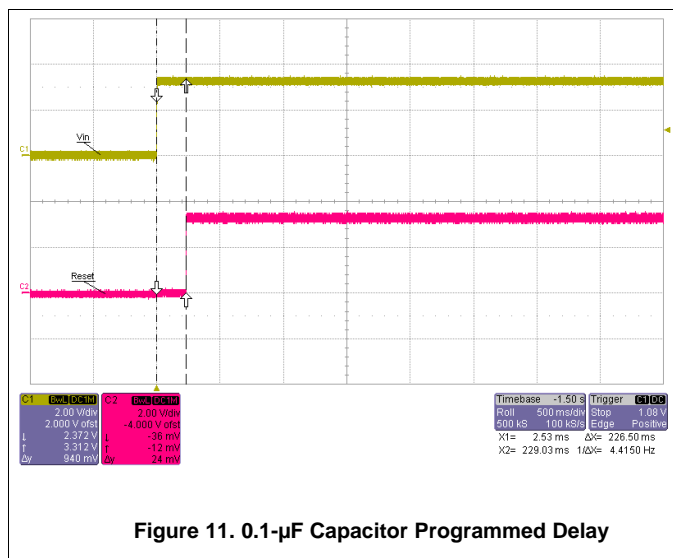


Figure 11. 0.1- μF Capacitor Programmed Delay

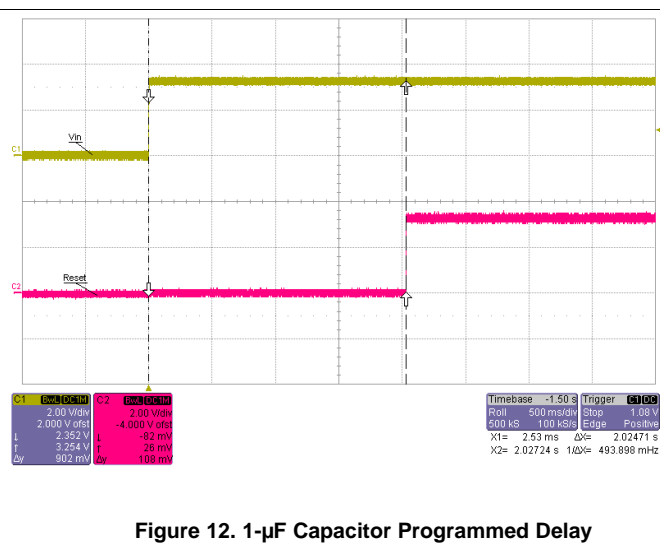


Figure 12. 1- μF Capacitor Programmed Delay

9 Power Supply Recommendations

The input of the LP3470 is designed to handle up to the supply voltage absolute maximum rating of 6 V. If the input supply is susceptible to any large transients above the maximum rating, then take extra precautions. An input capacitor is optional but not required to help avoid false reset output triggers due to noise.

10 Layout

10.1 Layout Guidelines

- Place components as close as possible to the IC
- Keep traces short between the IC and the C₁ capacitor to ensure the timing delay is as accurate as possible.

10.2 Layout Example

Figure 13 shows a layout example.

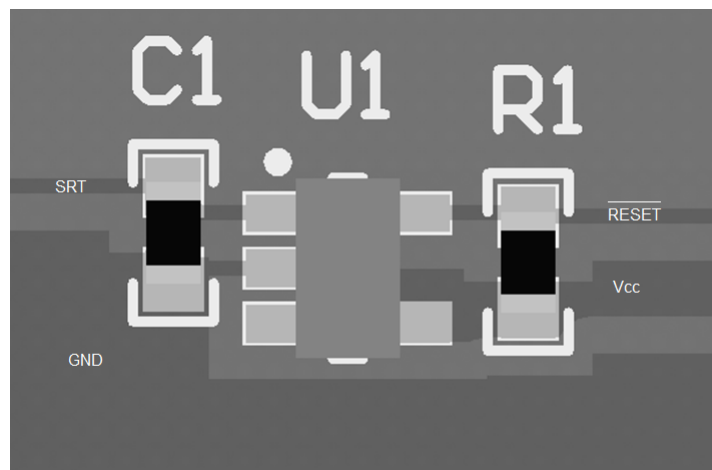


Figure 13. LP3470 Layout Example

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3470IM5-2.63/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D25C	Samples
LP3470IM5-2.75/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		D38C	Samples
LP3470IM5-2.83/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		D39C	Samples
LP3470IM5-2.93	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	D26C	
LP3470IM5-2.93/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D26C	Samples
LP3470IM5-3.08	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	D28C	
LP3470IM5-3.08/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D28C	Samples
LP3470IM5-3.65/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D37C	Samples
LP3470IM5-4.00	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	D29C	
LP3470IM5-4.00/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D29C	Samples
LP3470IM5-4.38	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	D30C	
LP3470IM5-4.38/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D30C	Samples
LP3470IM5-4.63	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	D31C	
LP3470IM5-4.63/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D31C	Samples
LP3470IM5-4.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		D15C	Samples
LP3470IM5X-2.63	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	D25C	
LP3470IM5X-2.63/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D25C	Samples
LP3470IM5X-2.83/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		D39C	Samples
LP3470IM5X-2.93/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D26C	Samples
LP3470IM5X-3.08	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	D28C	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3470IM5X-3.08/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D28C	Samples
LP3470IM5X-4.00	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	D29C	
LP3470IM5X-4.00/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D29C	Samples
LP3470IM5X-4.38/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D30C	Samples
LP3470IM5X-4.63/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	D31C	Samples
LP3470M5-2.63	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-20 to 85	D25B	
LP3470M5-2.63/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-20 to 85	D25B	Samples
LP3470M5-2.93/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-20 to 85	D26B	Samples
LP3470M5-3.08	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-20 to 85	D28B	
LP3470M5-3.08/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-20 to 85	D28B	Samples
LP3470M5-4.00/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-20 to 85	D29B	Samples
LP3470M5-4.38/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-20 to 85	D30B	Samples
LP3470M5-4.63	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-20 to 85	D31B	
LP3470M5-4.63/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-20 to 85	D31B	Samples
LP3470M5X-2.93/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-20 to 85	D26B	Samples
LP3470M5X-3.08/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-20 to 85	D28B	Samples
LP3470M5X-4.00/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-20 to 85	D29B	Samples
LP3470M5X-4.63/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-20 to 85	D31B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3470IM5-2.63/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-2.75/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-2.83/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-2.93	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-2.93/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-3.08	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-3.08/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-3.65/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-4.00	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-4.00/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-4.38	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-4.38/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-4.63	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-4.63/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5-4.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5X-2.63	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5X-2.63/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5X-2.83/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3470IM5X-2.93/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5X-3.08	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5X-3.08/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5X-4.00	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5X-4.00/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5X-4.38/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470IM5X-4.63/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5-2.63	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5-2.63/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5-2.93/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5-3.08	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5-3.08/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5-4.00/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5-4.38/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5-4.63	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5-4.63/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5X-2.93/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5X-3.08/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5X-4.00/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470M5X-4.63/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

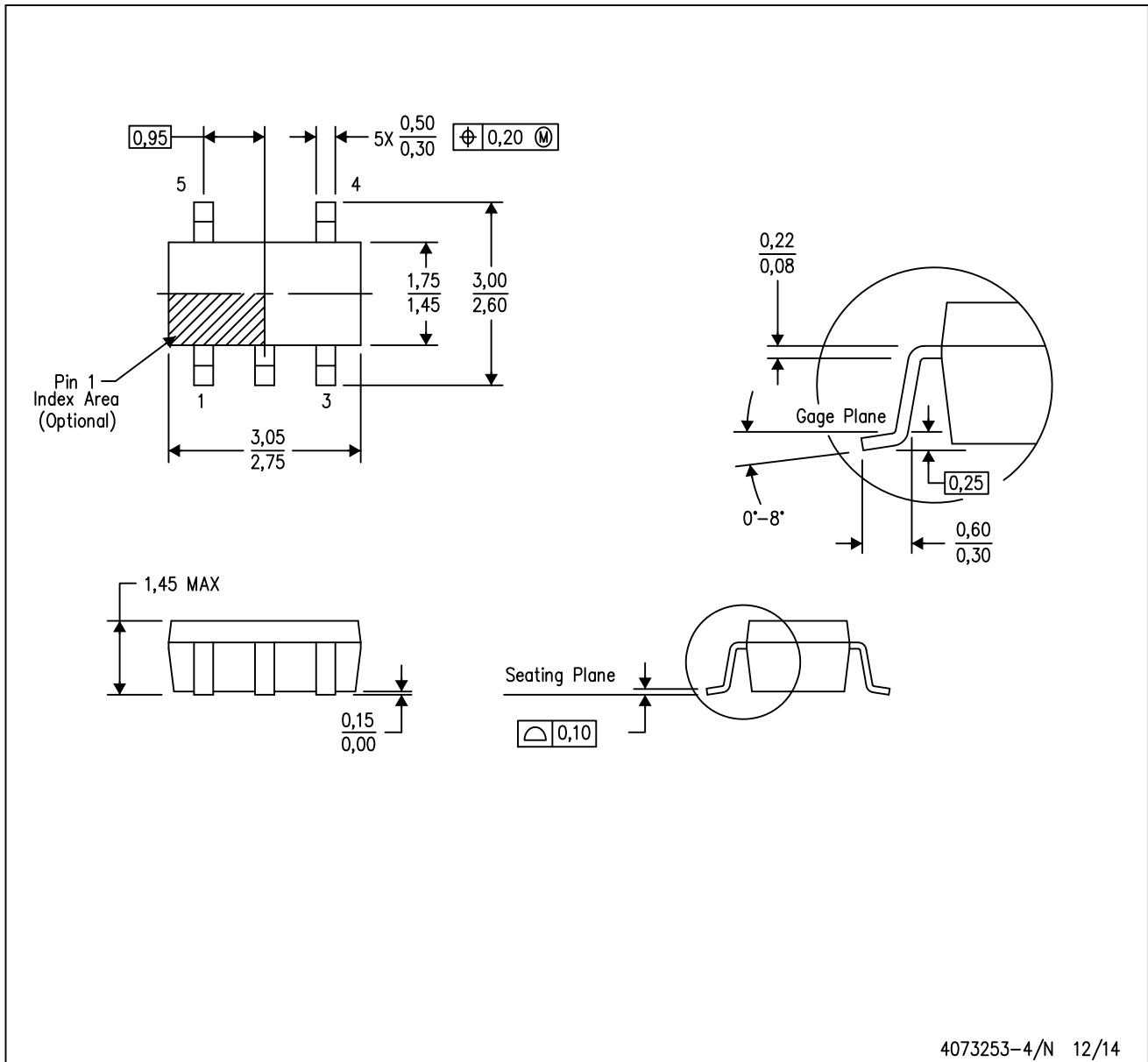
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3470IM5-2.63/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-2.75/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-2.83/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-2.93	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-2.93/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-3.08	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-3.08/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-3.65/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-4.00	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-4.00/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-4.38	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-4.38/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-4.63	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-4.63/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5-4.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470IM5X-2.63	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470IM5X-2.63/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470IM5X-2.83/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470IM5X-2.93/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470IM5X-3.08	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470IM5X-3.08/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470IM5X-4.00	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470IM5X-4.00/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470IM5X-4.38/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470IM5X-4.63/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470M5-2.63	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470M5-2.63/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470M5-2.93/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470M5-3.08	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470M5-3.08/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470M5-4.00/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470M5-4.38/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470M5-4.63	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470M5-4.63/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP3470M5X-2.93/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470M5X-3.08/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470M5X-4.00/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470M5X-4.63/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com