INA118 Precision, Low Power Instrumentation Amplifier

1 Features

- Low Offset Voltage: 50-µV Maximum
- Low Drift: 0.5-µV/°C Maximum
- Low Input Bias Current: 5-nA Maximum
- High CMR: 110-dB Minimum
- Inputs Protected to ±40 V
- Wide Supply Range: ±1.35 to ±18 V
- Low Quiescent Current: 350-µA
- 8-Pin Plastic DIP, SO-8

2 Applications

- Bridge Amplifiers
- Thermocouple Amplifiers
- RTD Sensor Amplifiers
- Medical Instrumentation
- Data Acquisition

3 Description

The INA118 is a low-power, general-purpose instrumentation amplifier offering excellent accuracy. The device's versatile, 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth, even at high gain (70 kHz at G = 100).

A single external resistor sets any gain from 1 to 10000. Internal input protection can withstand up to ±40 V without damage.

The INA118 is laser-trimmed for low offset voltage (50 µV), drift (0.5 µV/°C), and high common-mode rejection (110 dB at G = 1000). The INA118 operates with power supplies as low as ±1.35 V, and quiescent current is only 350 µA, making the device ideal for battery-operated systems.

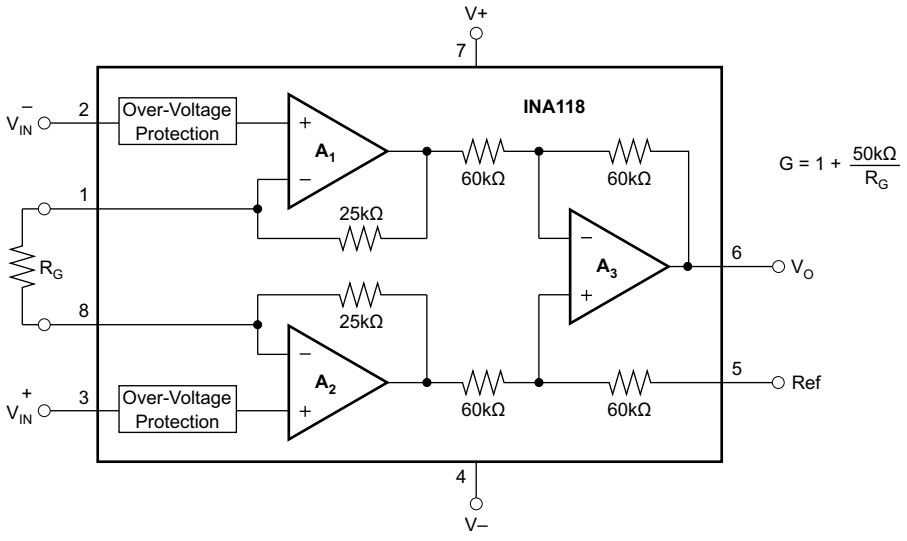
The INA118 is available in 8-pin plastic DIP and SO-8 surface-mount packages, specified for the –40°C to +85°C temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA118	SOIC (8)	3.91 mm × 4.90 mm
	PDIP (8)	6.35 mm × 9.81 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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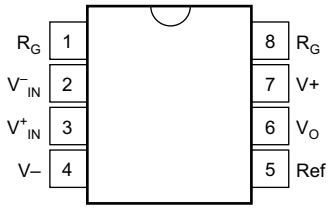
4 Revision History

Changes from Original (September 2000) to Revision A **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1

5 Pin Configuration and Functions

P and D Packages
8-Pin PDIP and SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	R_G	—	Gain setting pin. For gains greater than 1, place a gain resistor between pin 1 and pin 8.
2	V^-_{IN}	I	Negative input
3	V^+_{IN}	I	Positive input
4	V^-	—	Negative supply
5	Ref	I	Reference input. This pin must be driven by low impedance or connected to ground.
6	V_O	O	Output
7	V^+	—	Positive supply
8	R_G	—	Gain setting pin. For gains greater than 1, place a gain resistor between pin 1 and pin 8.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	Supply voltage		±18	V
	Analog input voltage		±40	V
	Output short-circuit (to ground)	Continuous		
	Operating temperature	–40	125	°C
	Junction temperature		150	°C
	Lead temperature (soldering, 10 s)		300	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V	Power supply	±2.25	±15	±18	V
$V_O = 0$	Input common-mode voltage	V^- + 1.1		V^+ – 1	V
T_A	Ambient temperature	–55		150	°C

6.4 Thermal Information

THERMAL METRIC (1)		INA118		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115	48	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62	37	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59	25	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14	14	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58	25	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
Offset voltage, RTI	Initial	T_A = 25°C	INA118PB, UB		±10 ± 50/G	±50 ± 500/G	µV
			INA118P, U		±25 ±100/G	±125±1000/G	
	vs Temperature	T_A = T_{MIN} to T_{MAX}	INA118PB, UB		±0.2 ± 2/G	±0.5 ± 20/G	µV/°C
			INA118P, U		±0.2 ± 5/G	±1 ± 20/G	
	vs Power supply	V_S = ±1.35 V to ±18 V	INA118PB, UB		±1 ±10/G	±5 ± 100/G	µV/V
			INA118P, U		±1 ±10/G	±10 ±100/G	
	Long-term stability				±0.4 ±5/G		µV/mo
Impedance	Differential				10^{10} || 1		Ω || pF
	Common-mode				10^{10} || 4		
Linear input voltage range				(V^+) – 1	(V^+) – 0.65		V
				(V^-) + 1.1	(V^-) + 0.95		
Safe input voltage						±40	V
Common-mode rejection		V_{CM} = ±10 V, ΔR_S = 1 kΩ, G = 1	INA118PB, UB	80	90		dB
			INA118P, U	73	90		
		V_{CM} = ±10 V, ΔR_S = 1 kΩ, G = 10	INA118PB, UB	97	110		
			INA118P, U	89	110		
		V_{CM} = ±10 V, ΔR_S = 1 kΩ, G = 100	INA118PB, UB	107	120		
			INA118P, U	98	120		
		V_{CM} = ±10 V, ΔR_S = 1 kΩ, G = 1000	INA118PB, UB	110	125		
			INA118P, U	100	125		
BIAS CURRENT			INA118PB, UB		±1	±5	nA
			INA118P, U		±1	±10	
vs temperature					±40		pA/°C
OFFSET CURRENT			INA118PB, UB		±1	±5	nA
			INA118P, U		±1	±10	
vs temperature					±40		pA/°C
NOISE VOLTAGE, RTI							
	f = 10 Hz	G = 1000, R_S = 0 Ω			11		nV/√Hz
	f = 100 Hz				10		nV/√Hz
	f = 1 kHz				10		nV/√Hz
	f_B = 0.1 Hz to 10 Hz				0.28		µVp-p
Noise current	f = 10 Hz				2		pA/√Hz
	f = 1 kHz				0.3		
	f_B = 0.1 Hz to 10 Hz				80		pAp-p
GAIN							
Gain equation					1 + (50 kΩ/R_G)		V/V
Range of gain				1		10000	V/V
Gain error		G = 1			±0.01%	±0.024%	
		G = 10			±0.02%	±0.4%	
		G = 100			±0.05%	±0.5%	
		G = 1000			±0.5%	±1%	
Gain vs temperature		G = 1			±1	±10	ppm/°C
50-kΩ resistance(1)					±25	±100	ppm/°C
Nonlinearity		G = 1			±0.0003	±0.001	% of FSR
		G = 10			±0.0005	±0.002	
		G = 100			±0.0005	±0.002	
		G = 1000			±0.002	±0.01	

(1) Temperature coefficient of the **50-kΩ** term in the gain equation.

Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
Voltage:	Positive	R_L = 10 kΩ	(V^+) – 1	(V^+) – 0.8		V
	Negative		(V^-) + 0.35	(V^-) + 0.2		
	Single supply high	V_S = 2.7 V/0 V(2), R_L = 10 kΩ	1.8	2		
	Single supply low		60	35		mV
Load capacitance stability				1000		pF
Short circuit current				+5/–12		mA
FREQUENCY RESPONSE						
Bandwidth, –3 dB		G = 1		800		kHz
		G = 10		500		
		G = 100		70		
		G = 1000		7		
Slew rate		V_O = ±10 V, G = 10		0.9		V/µs
Settling time, 0.01%		G = 1		15		µs
		G = 10		15		
		G = 100		21		
		G = 1000		210		
Overload recovery		50% Overdrive		20		µs
POWER SUPPLY						
Voltage range			±1.35	±15	±18	V
Current		V_{IN} = 0 V		±350	±385	µA
TEMPERATURE RANGE						
Specification			–40		85	°C
Operating			–40		125	°C

(2) Common-mode input voltage range is limited. See text for discussion of low power supply and single power supply operation.

6.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V (unless otherwise noted).

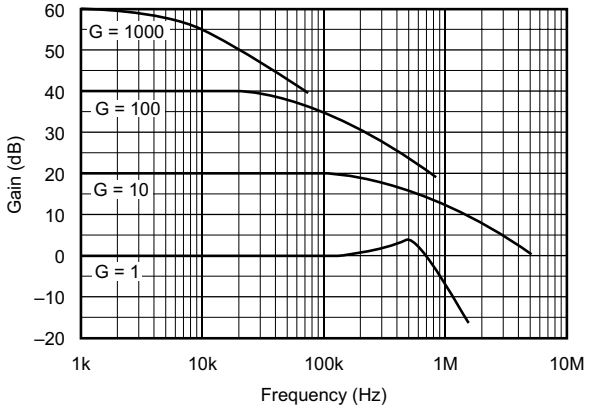


Figure 1. Gain vs Frequency

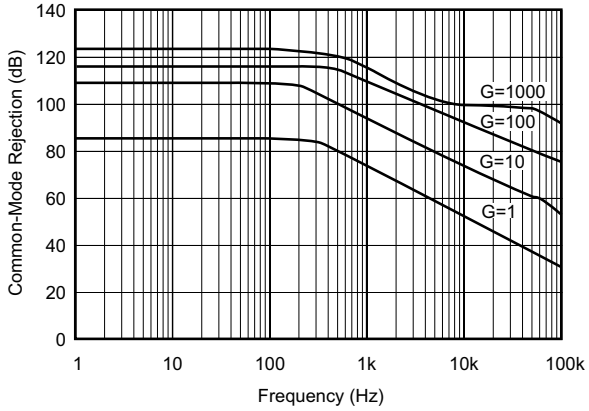


Figure 2. Common-Mode Rejection vs Frequency

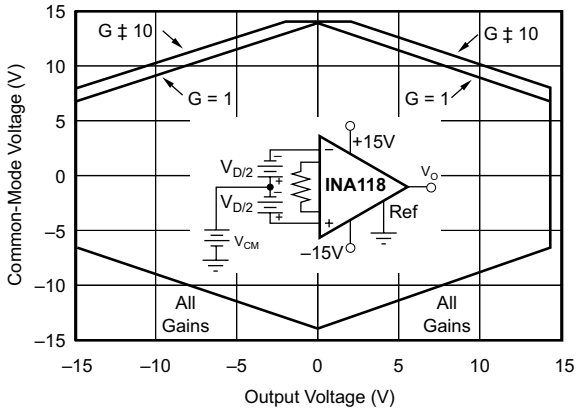


Figure 3. Input Common-Mode Range vs Output Voltage

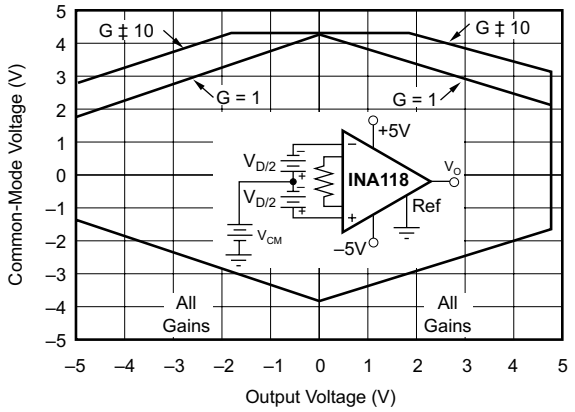


Figure 4. Input Common-Mode Range vs Output Voltage

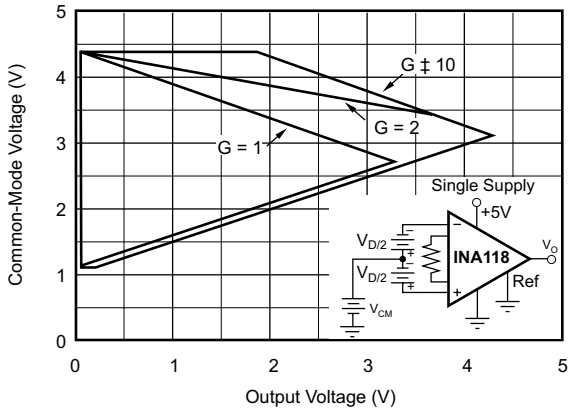


Figure 5. Input Common-Mode Range vs Output Voltage

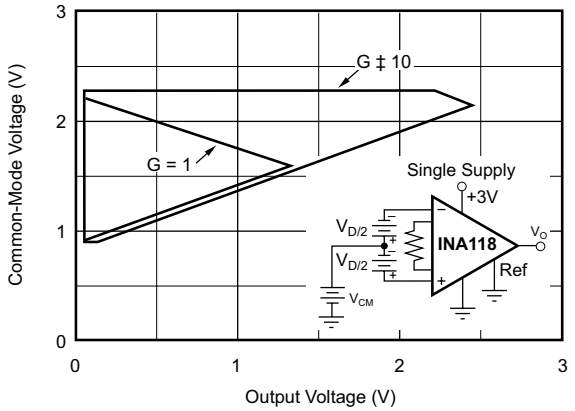


Figure 6. Input Common-Mode Range vs Output Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V (unless otherwise noted).

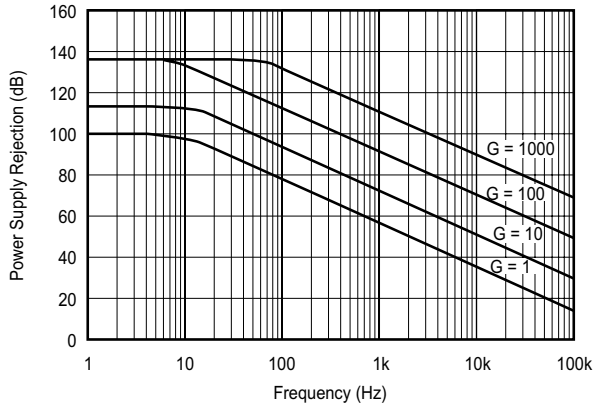


Figure 7. Positive Power Supply Rejection vs Frequency

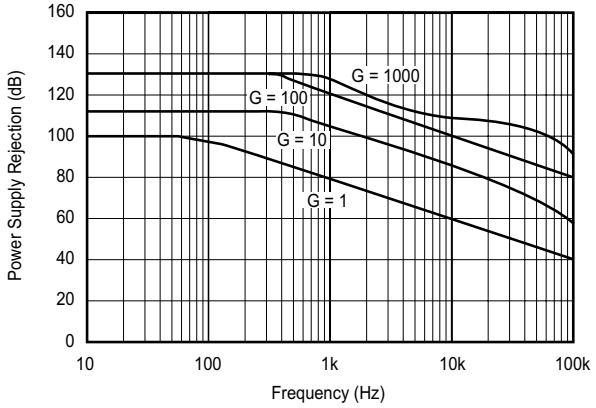


Figure 8. Negative Power Supply Rejection vs Frequency

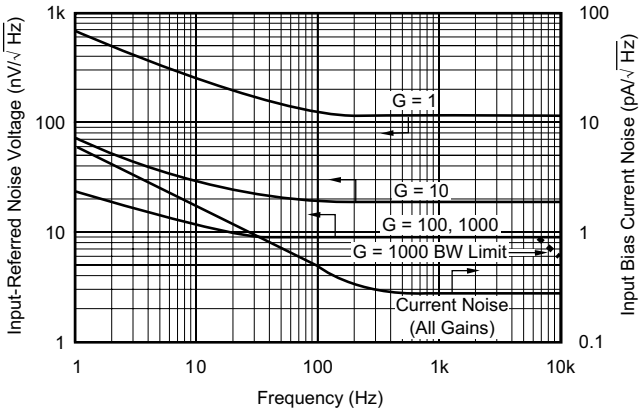


Figure 9. Input-Referred Noise Voltage vs Frequency

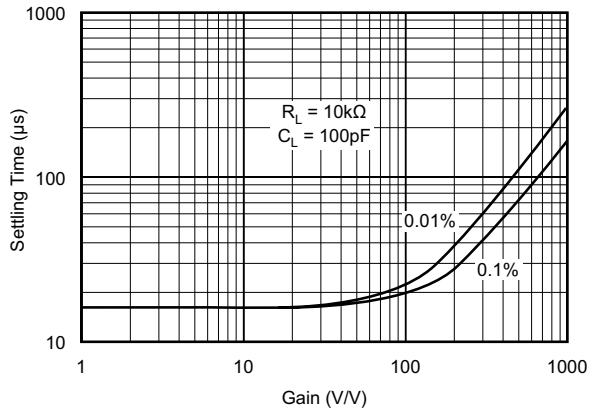


Figure 10. Settling Time vs Gain

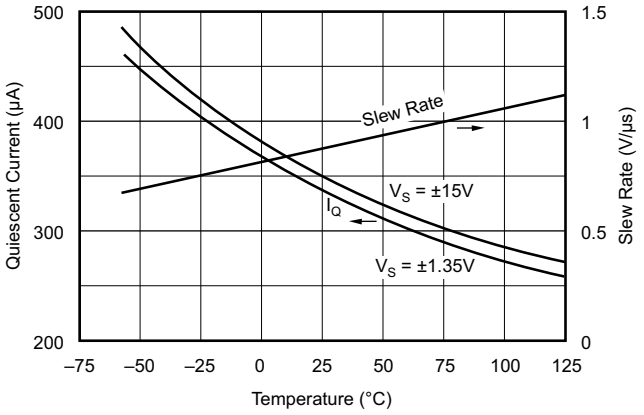


Figure 11. Quiescent Current and Slew Rate vs Temperature

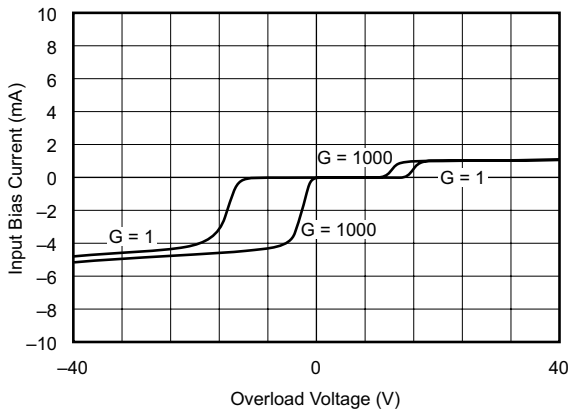


Figure 12. Input Bias Current vs Input Overload Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V (unless otherwise noted).

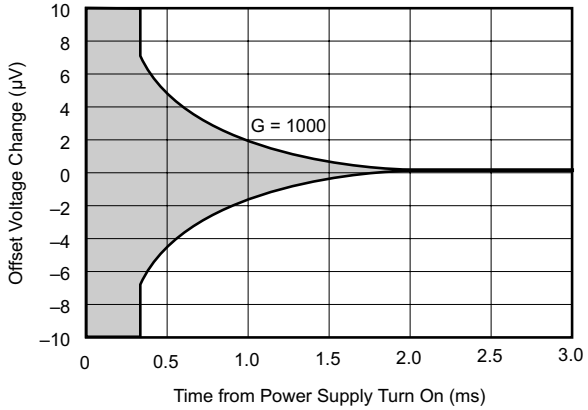


Figure 13. Offset Voltage vs Warm-Up Time

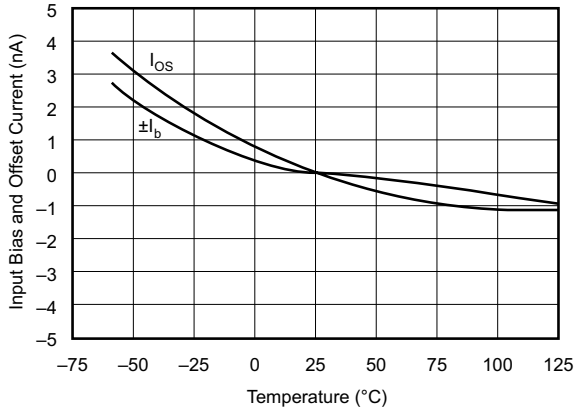


Figure 14. Input Bias and Offset Current vs Temperature

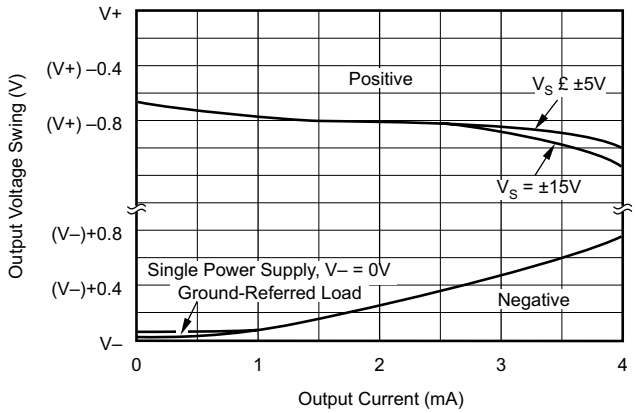


Figure 15. Output Voltage Swing vs Output Current

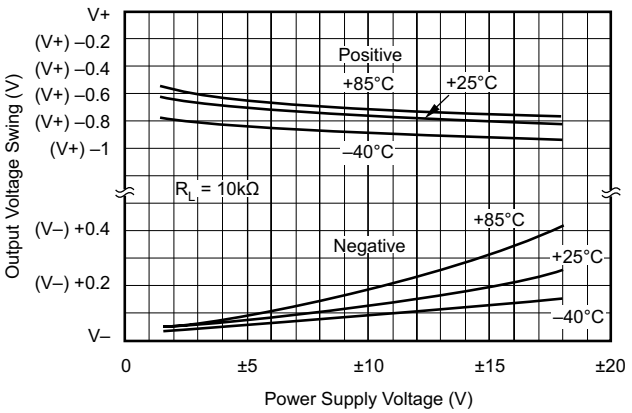


Figure 16. Output Voltage Swing vs Power Supply Voltage

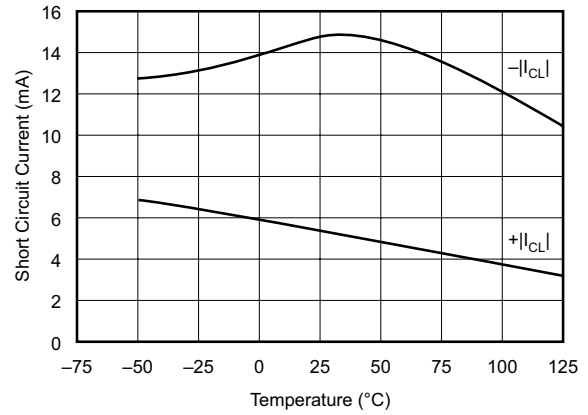


Figure 17. Output Current Limit vs Temperature

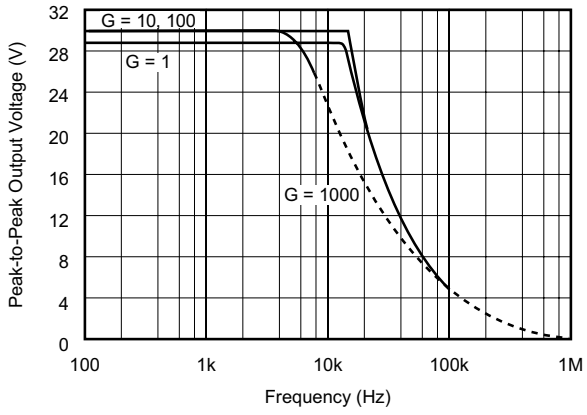


Figure 18. Maximum Output Swing vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V (unless otherwise noted).

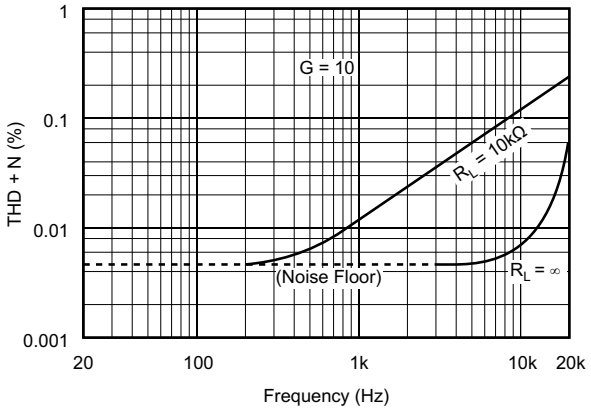


Figure 19. THD + N vs Frequency

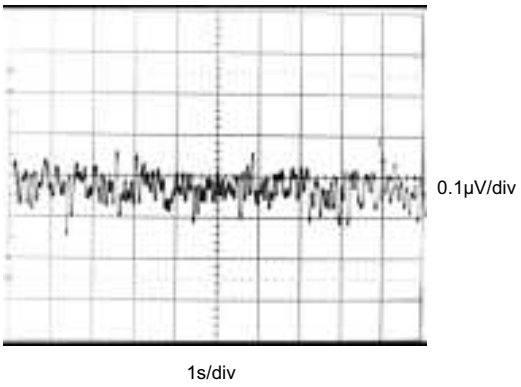


Figure 20. Input-Referred Noise, 0.1 Hz to 10 Hz

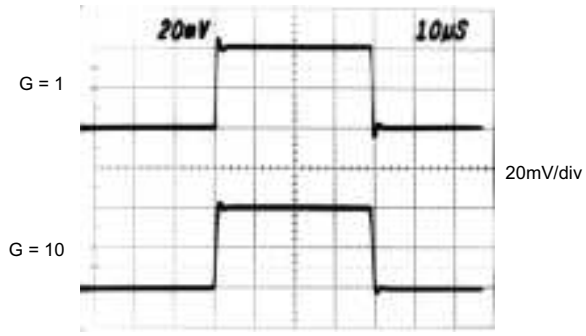


Figure 21. Small-Signal Response

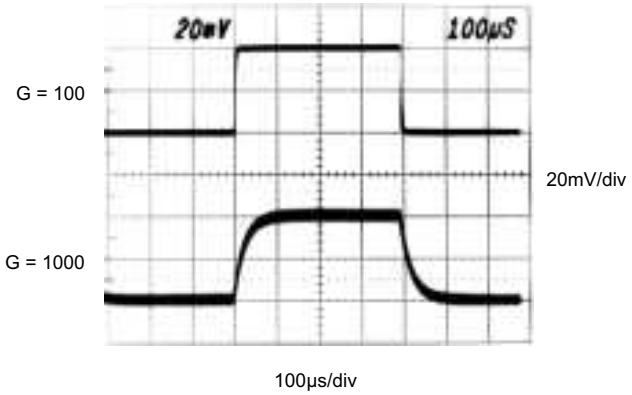


Figure 22. Small-Signal Response

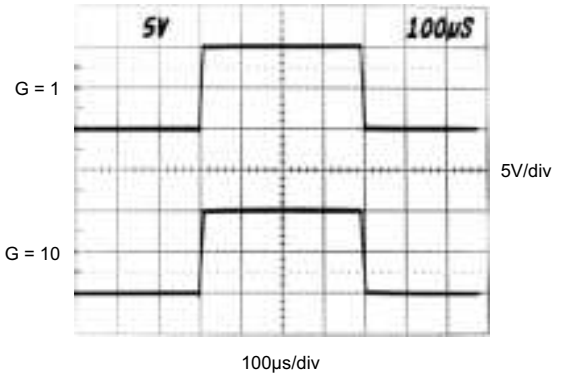


Figure 23. Large-Signal Response

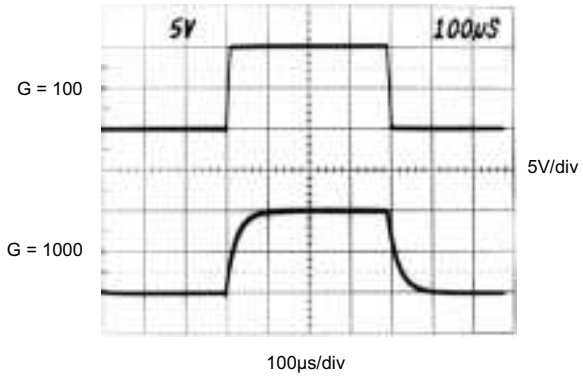


Figure 24. Large-Signal Response

7 Detailed Description

7.1 Overview

Figure 25 shows a simplified representation of the INA118 and provides insight into its operation. Each input is protected by two FET transistors that provide a low series resistance under normal signal conditions, preserving excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 1.5 to 5 mA.

The differential input voltage is buffered by Q_1 and Q_2 and impressed across R_G, causing a signal current to flow through R_G, R_1 and R_2. The output difference amp, A_3, removes the common-mode component of the input signal and refers the output signal to the Ref terminal.

The equations in Figure 25 describe the output voltages of A_1 and A_2. The V_{BE} and IR drop across R_1 and R_2 produce output voltages on A_1 and A_2 that are approximately 1-V lower than the input voltages.

7.2 Functional Block Diagram

A_1 Out = $V_{CM} - V_{BE} - (10\mu A \cdot 25k\Omega) - V_O/2$
A_2 Out = $V_{CM} - V_{BE} - (10\mu A \cdot 25k\Omega) + V_O/2$
Output Swing Range A_1, A_2; (V+) – 0.65V to (V–) + 0.06V
Amplifier Linear Input Range: (V+) – 0.65V to (V–) + 0.98V

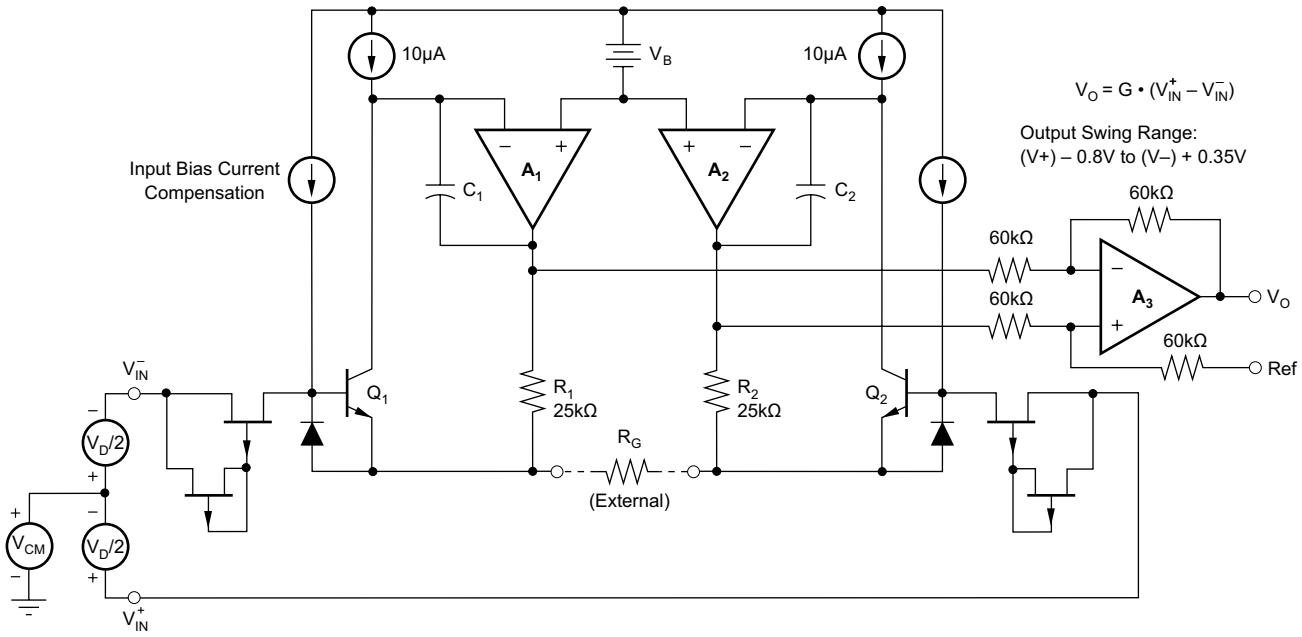


Figure 25. INA118 Simplified Circuit Diagram

7.3 Feature Description

The INA118 input sections use junction field effect transistors (JFET) connected to provide protection up to ±40 V. The current-feedback architecture provides maximum bandwidth over the full range of gain settings.

7.4 Device Functional Modes

7.4.1 Noise Performance

The INA118 provides low noise in most applications. For differential source impedances less than 1 kΩ, the INA103 may provide lower noise. For source impedances greater than 50 kΩ, the INA111 FET-Input Instrumentation Amplifier may provide lower noise.

Device Functional Modes (continued)

Low-frequency noise of the INA118 is approximately 0.28 µVp-p, measured from 0.1 to 10 Hz (G≥100). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

7.4.2 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA118 is from approximately 0.6-V less than the positive supply voltage to 1-V greater than the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2. Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage; see Figure 6.

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA118 is near 0 V even though both inputs are overloaded.

7.4.3 Input Protection

The inputs of the INA118 are individually protected for voltages up to ±40 V. For example, a condition of –40 V on one input and +40 V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.5 to 5 mA. Figure 12 shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA118 measures a small differential voltage with a high common-mode voltage developed between the noninverting and inverting input. The high common-mode rejection makes the INA118 suitable for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations

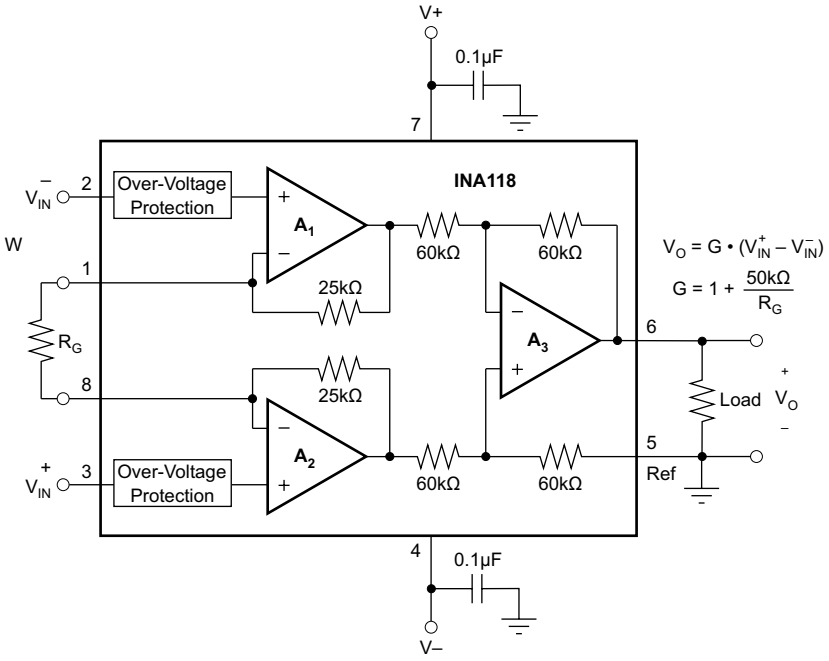
8.2 Typical Application

Figure 26 shows the basic connections required for operation of the INA118. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown. The output is referred to the output reference (Ref) terminal, which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 12 Ω in series with the Ref pin causes a typical device to degrade to approximately 80-dB CMR (G = 1).

Figure 26 depicts an input signal with a 5-mV, 1-kHz signal with a 1-Vp-p common-mode signal, a condition often observed in process control systems. Figure 27 depicts the output of the INA118 (gain = 250) depicting the clean recovered 1-kHz waveform.

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

NC: No Connection.



Also drawn in simplified form:

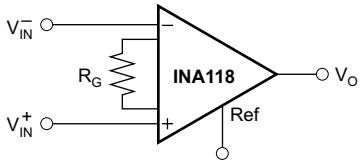


Figure 26. Basic Connections

Typical Application (continued)

8.2.1 Design Requirements

Figure 30 and Figure 29 depict the performance of a typical application of the INA118 in a shop floor vibration sensing application. Because industrial process control systems often involve the interconnecting of multiple subsystems, ground loops are frequently encountered and often are not easily solved. The inherent common-mode rejection of instrumentation amplifiers enables accurate measurements even in the presence of ground loop potentials.

The typical application was tested in a system with these requirements:

- Transducer signal ≈ 5 mVp-p
- Transducer center frequency = 1 kHz
- Common-Mode signal (required to be rejected): 1 Vp-p at 60 Hz

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Gain

As shown in Equation 1, the gain of the INA118 is set by connecting a single external resistor, R_G, connected between pins 1 and 8.

$$G = 1 + \frac{50\,k\Omega}{R_G} \tag{1}$$

Commonly used gains and resistor values are shown in Figure 26.

The 50-kΩ term in Equation 1 comes from the sum of the two internal feedback resistors of A_1 and A_2. These on-chip metal film resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA118.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. The contribution of R_G to gain accuracy and drift can be directly inferred from Equation 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which contributes additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

8.2.2.2 Dynamic Performance

The Figure 1 shows that, despite its low quiescent current, the INA118 achieves wide bandwidth, even at high gain. This is due to the current-feedback topology of the INA118. Settling time also remains excellent at high gain.

The INA118 exhibits approximately 3-dB peaking at 500 kHz in unity gain. This is a result of its current-feedback topology and is not an indication of instability. Unlike an op amp with poor phase margin, the rise in response is a predictable 6-dB/octave due to a response zero. A simple pole at 300 kHz or lower produces a flat passband unity gain response.

8.2.2.3 Offset Trimming

The INA118 is laser-trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 27 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref terminal is summed at the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

Typical Application (continued)

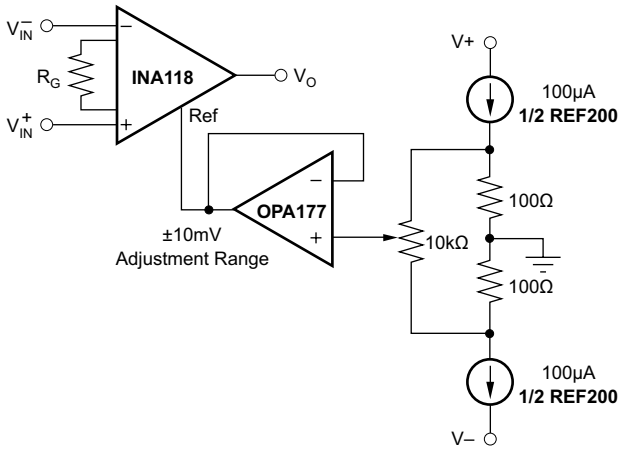


Figure 27. Optional Trimming of Output Offset Voltage

8.2.2.4 Input Bias Current Return Path

The input impedance of the INA118 is extremely high at approximately 10^{10} Ω. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±5 nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 28 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential which exceeds the common-mode range of the INA118, and the input amplifiers saturates.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 28). With higher source impedance, using two equal resistors provides a balanced input, with the possible advantages of lower input offset voltage due to bias current, and better high-frequency common-mode rejection.

Typical Application (continued)

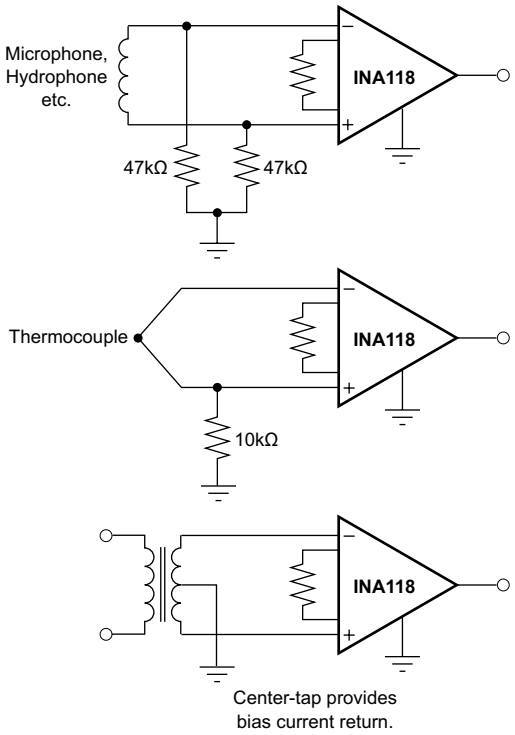
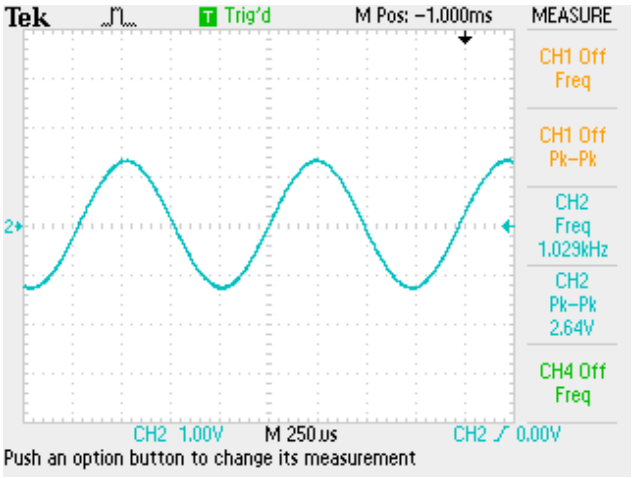


Figure 28. Providing an Input Common-Mode Current Path

8.2.3 Application Curves



1-kHz differential signal is also present but cannot be seen in this waveform.

Figure 29. Input of Typical Application Showing 60-Hz Common-Mode Signal

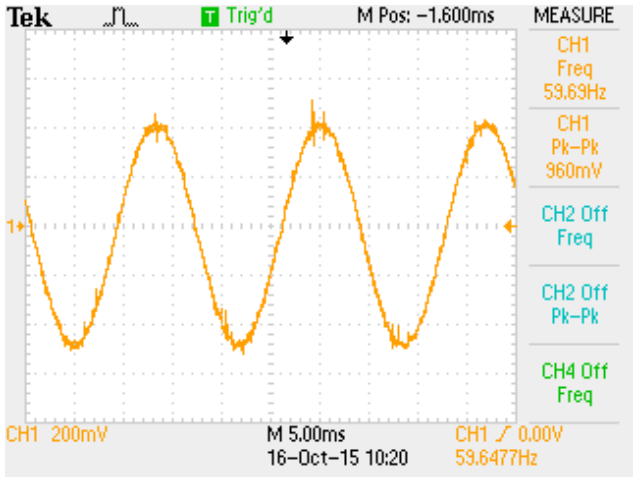


Figure 30. Output of Typical Application Shows Desired 1-kHz Waveform With Common-Mode Interference Rejected

9 Power Supply Recommendations

9.1 Low Voltage Operation

The INA118 can be operated on power supplies as low as ±1.35 V. Performance of the INA118 remains excellent with power supplies ranging from ±1.35 V to ±18 V. Most parameters vary only slightly throughout this supply voltage range; see *Typical Characteristics*. Operation at low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Figure 3 shows the range of linear operation for a various supply voltages and gains.

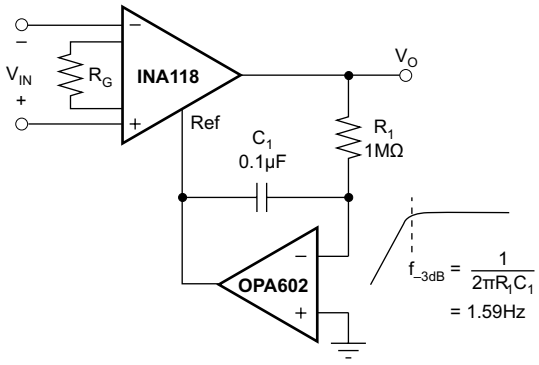
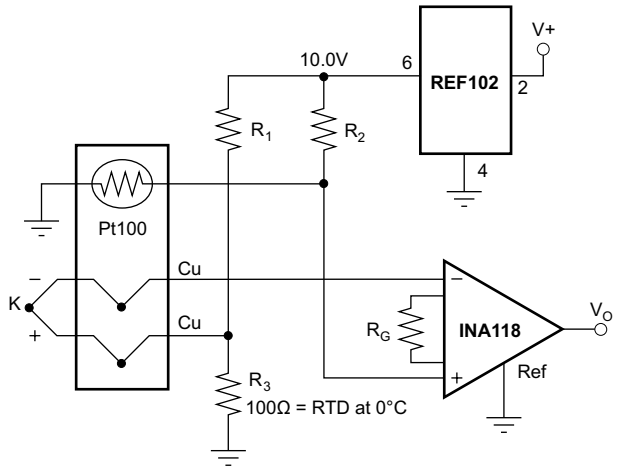


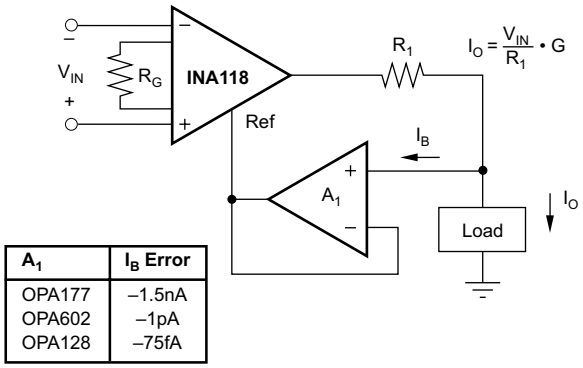
Figure 31. AC-Coupled Instrumentation Amplifier



ISA TYPE	MATERIAL	COEFFICIENT (µV/°C)	R_1, R_2
E	+ Chromel – Constantan	58.5	66.5kΩ
J	+ Iron – Constantan	50.2	76.8kΩ
K	+ Chromel – Alumel	39.4	97.6kΩ
T	+ Copper – Constantan	38.0	102kΩ

Figure 32. Thermocouple Amplifier With Cold Junction Compensation

Low Voltage Operation (continued)



A_1	I_B Error
OPA177	–1.5nA
OPA602	–1pA
OPA128	–75fA

Figure 33. Differential Voltage to Current Converter

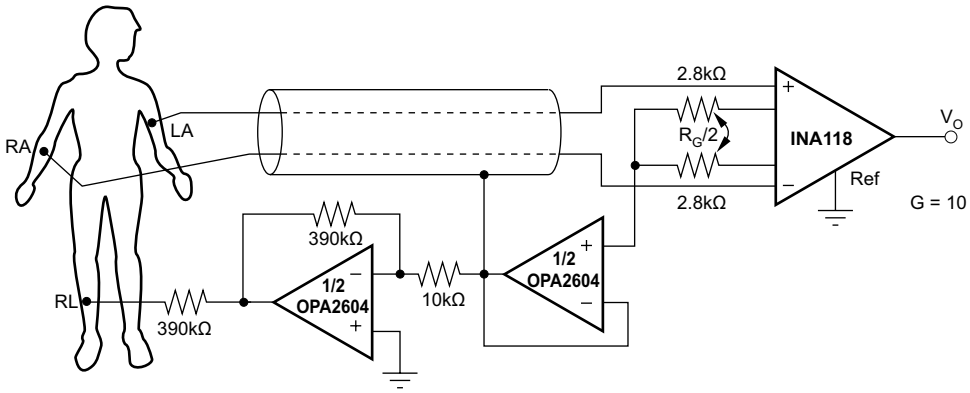


Figure 34. ECG Amplifier With Right-Leg Drive

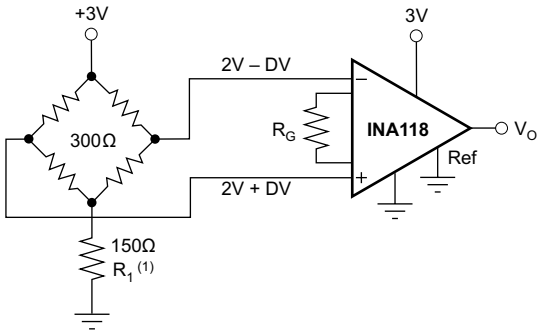
9.2 Single Supply Operation

The INA118 can be used on single power supplies of 2.7 V to 36 V. Figure 35 shows a basic single supply circuit. The output Ref terminal is connected to ground. Zero differential input voltage demands an output voltage of 0 V (ground). Actual output voltage swing is limited to approximately 35-mV above ground, when the load is referred to ground as shown. Figure 15 shows how the output voltage swing varies with output current.

With single supply operation, V^+_{IN} and V^-_{IN} must both be 0.98-V above ground for linear operation. It is not possible, for example, to connect the inverting input to ground and measure a voltage connected to the noninverting input.

To illustrate the issues affecting low voltage operation, consider the circuit in Figure 35, which shows the INA118 operating from a single 3-V supply. A resistor in series with the low side of the bridge assures that the bridge output voltage is within the common-mode range of the amplifier's inputs. See Figure 3 for 3-V single supply operation.

Single Supply Operation (continued)



NOTE: (1) R_1 required to create proper common-mode voltage, only for low voltage operation — see text.

Figure 35. Single-Supply Bridge Amplifier

10 Layout

10.1 Layout Guidelines

TI always recommends paying attention to good layout practices. For best operational performance of the device, use good printed-circuit-board (PCB) layout practices, including:

- Take care to ensure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. In addition, parasitic capacitance at the gain-setting pins can also affect CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS® relays to change the value of RG, select the component so that the switch capacitance is as small as possible.
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, and of the device itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry. Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V^+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques* (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Keep the traces as short as possible.

10.2 Layout Example

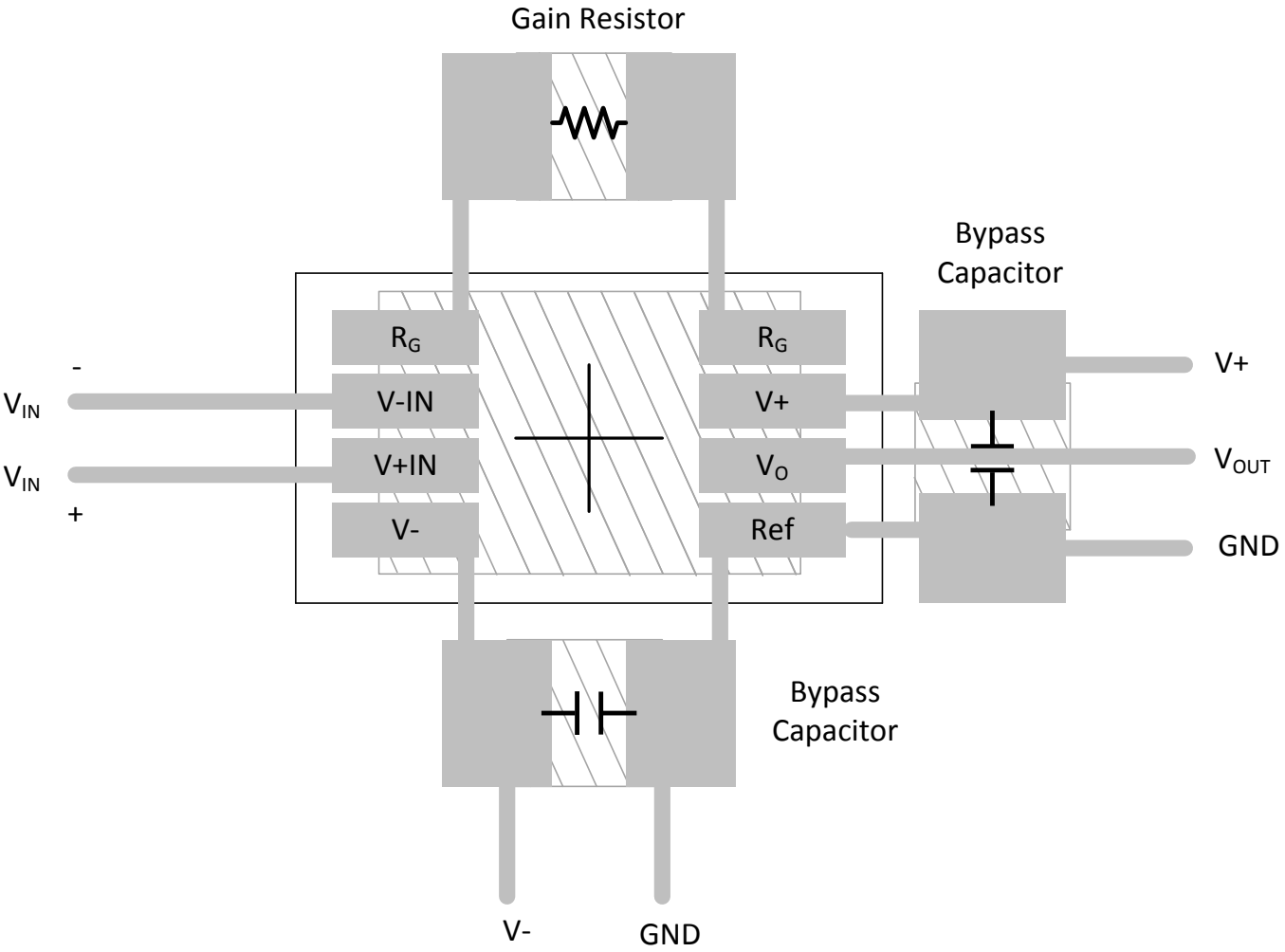


Figure 36. Layout Recommendation

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

Table 1. Design Kits and Evaluation Modules

NAME	PART NUMBER	TYPE
DIP Adapter Evaluation Module	DIP-ADAPTER-EVM	Evaluation Modules and Boards
Universal Instrumentation Amplifier Evaluation Module	INAEVM	Evaluation Modules and Boards

Table 2. Development Tools

NAME	PART NUMBER	TYPE
Calculate Input Common-Mode Range of Instrumentation Amplifiers	INA-CMV-CALC	Calculation Tools
SPICE-Based Analog Simulation Program	TINA-TI	Circuit Design and Simulation

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, refer to the following:

Circuit Board Layout Techniques (SLOA089)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA118P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	INA118P	Samples
INA118PB	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA118P B	Samples
INA118PBG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA118P B	Samples
INA118PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	INA118P	Samples
INA118U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 118U	Samples
INA118U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 118U	Samples
INA118U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 118U	Samples
INA118UB	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 118U B	Samples
INA118UB/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 118U B	Samples
INA118UB/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 118U B	Samples
INA118UBG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 118U B	Samples
INA118UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 118U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

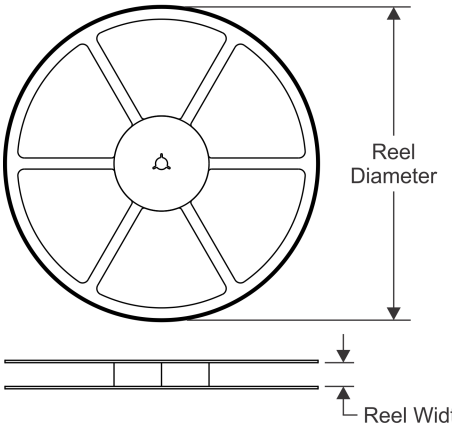
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

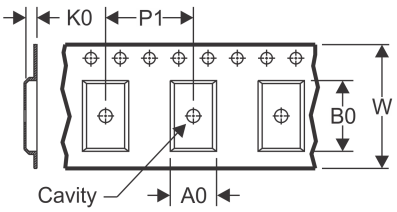
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

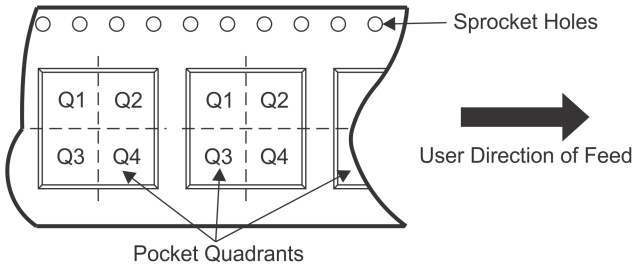


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

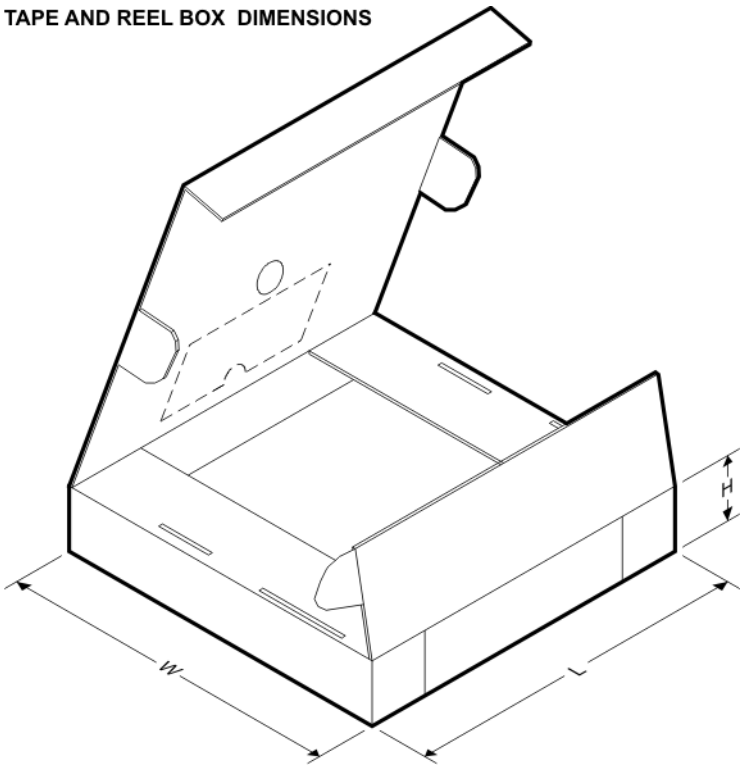
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA118U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA118UB/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

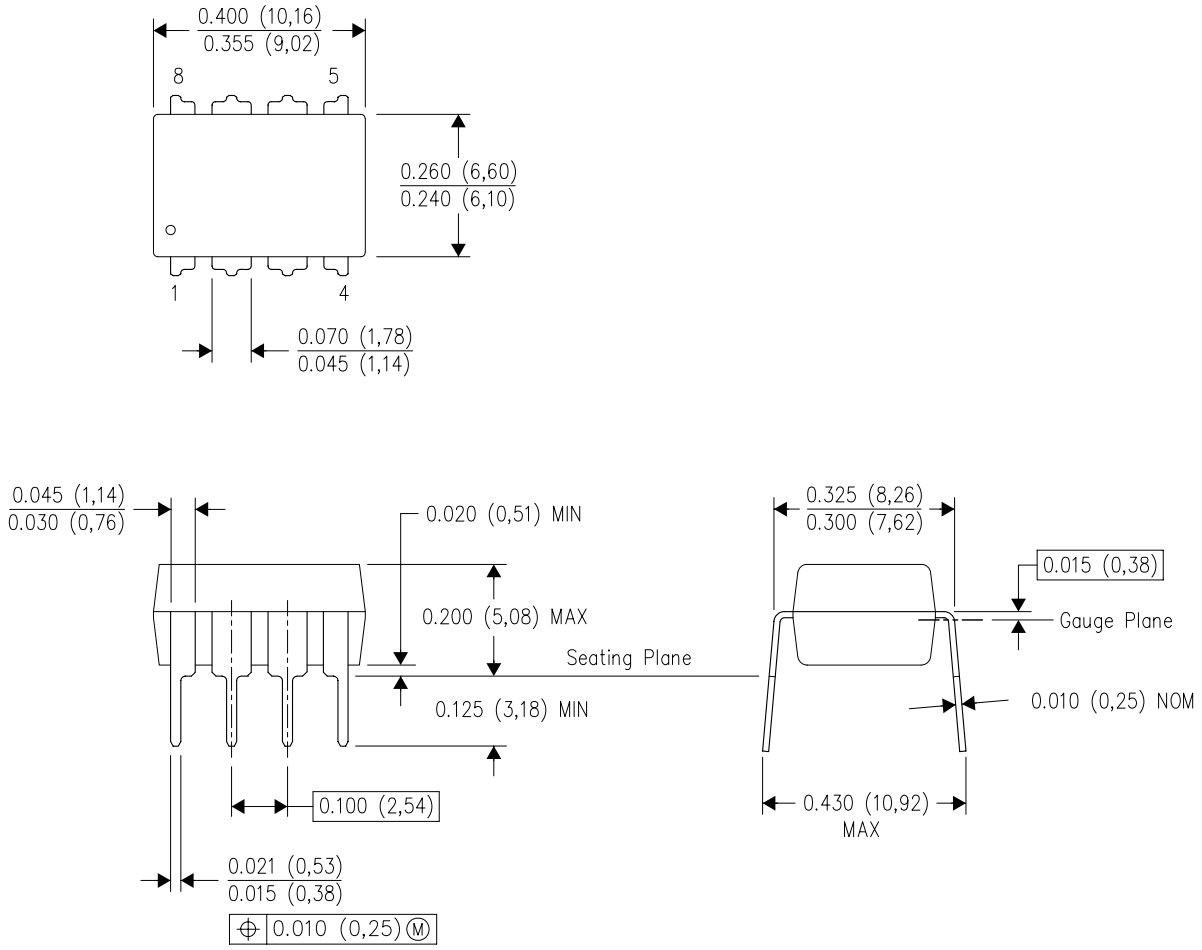
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

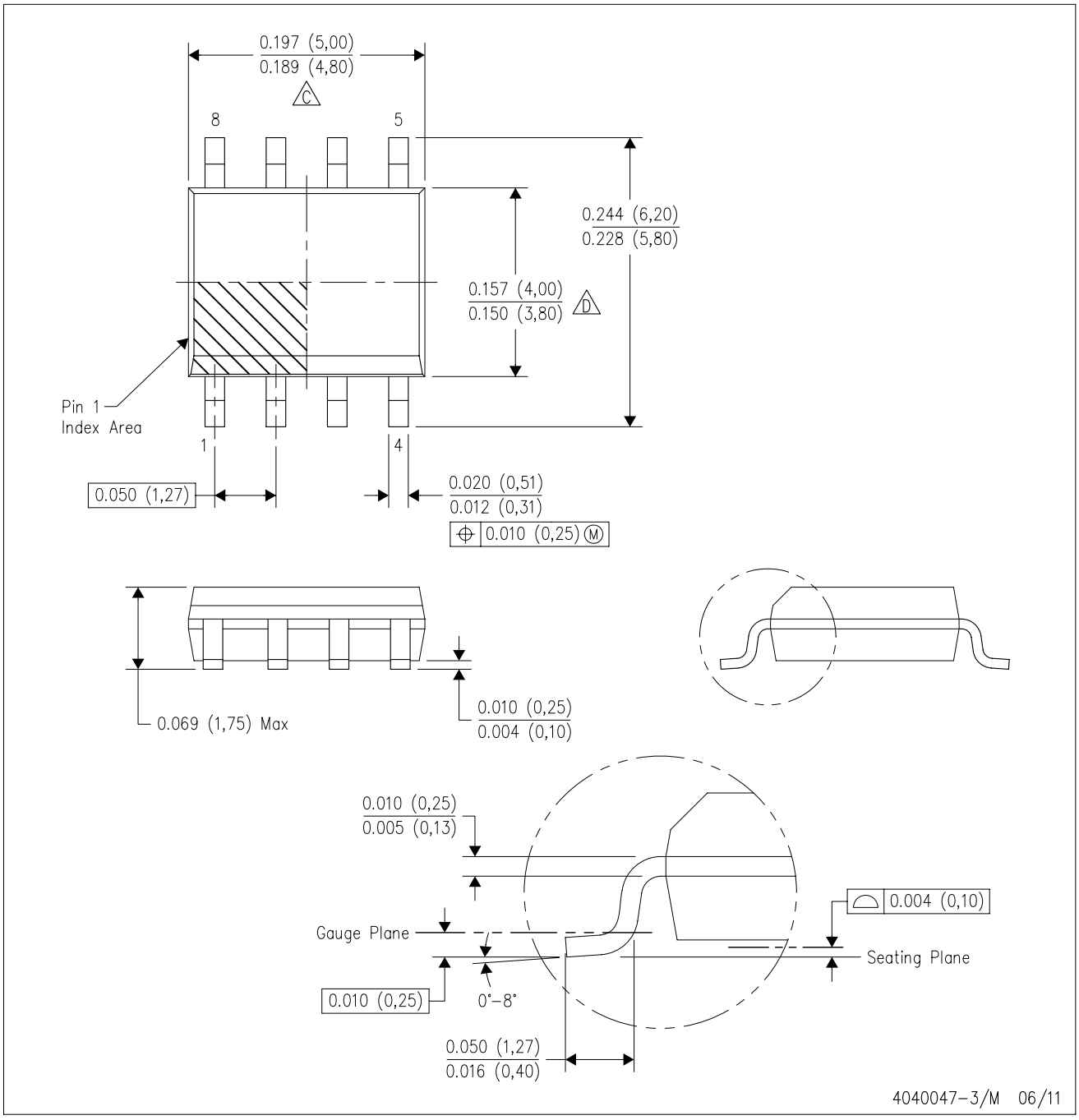
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA118U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA118UB/2K5	SOIC	D	8	2500	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



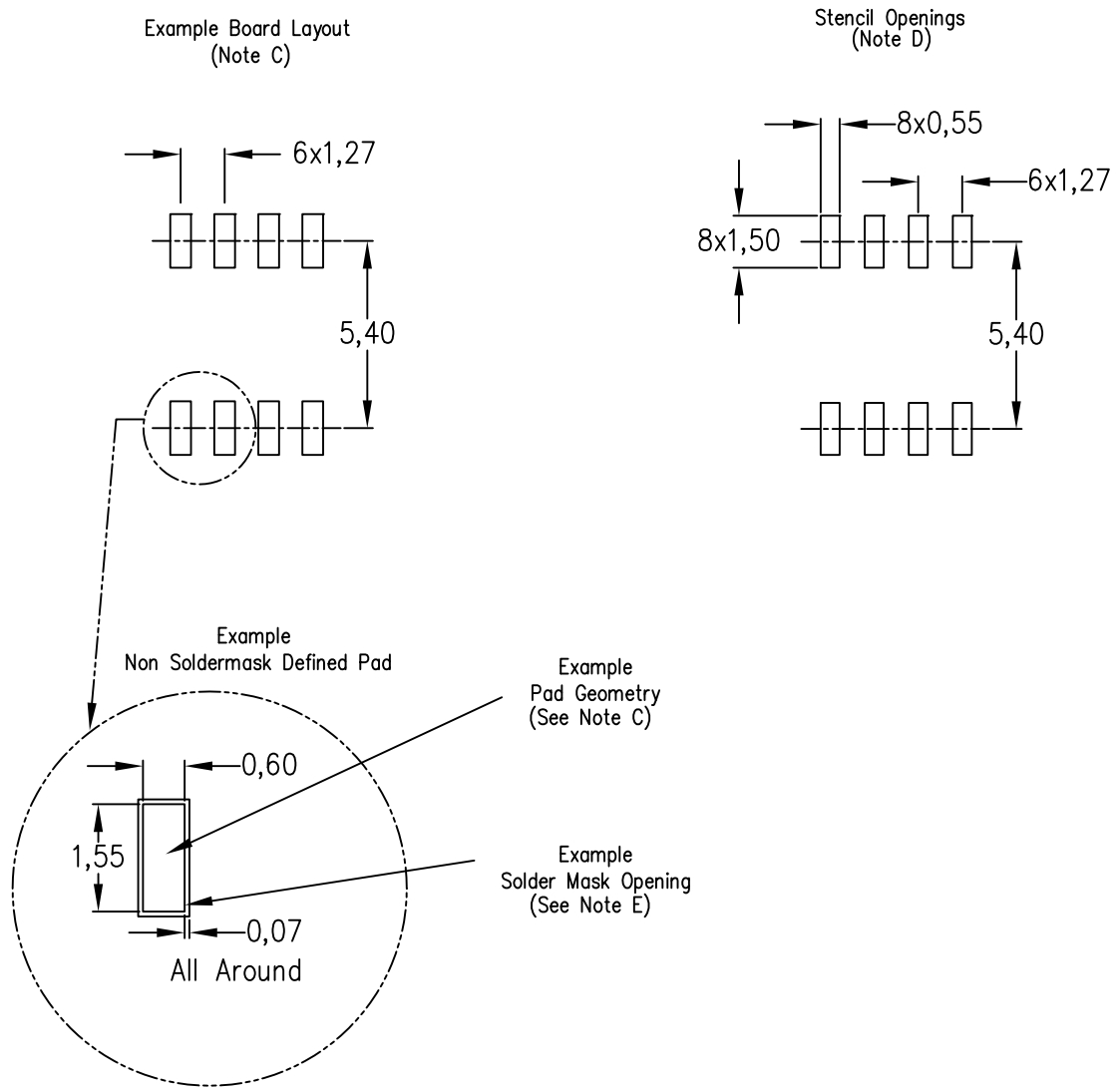
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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