TEXAS INSTRUMENTS

SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244

SDLS144D – APRIL 1985 – REVISED OCTOBER 2016

SNx4LS24x, SNx4S24x Octal Buffers and Line Drivers With 3-State Outputs

1 Features

- Inputs Tolerant Down to 2 V, Compatible With 3.3-V or 2.5-V Logic Inputs
- Maximum t_{pd} of 15 ns at 5 V
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- Hysteresis at Inputs Improves Noise Margins

2 Applications

- Servers
- LED Displays
- Network Switches
- Telecom Infrastructure
- Motor Drivers
- I/O Expanders

3 Description

The SNx4LS24x, SNx4S24x octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and non-inverting outputs, symmetrical, active-low output-control ($\overline{G}$) inputs, and complementary output-control (G and $\overline{G}$) inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise margin. The SN74LS24x and SN74S24x devices can be used to drive terminated lines down to 133 Ω.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN54LS24x, SN54S24x	CDIP (20) – J	24.20 mm × 6.92 mm
	CFP (20) – W	7.02 mm × 13.72 mm
	LCCC (20) – FK	8.89 mm × 8.89 mm
SN74LS240, SN74LS244	SSOP (20) – DB	7.20 mm × 5.30 mm
SN74LS24x, SN74S24x	SOIC (20) – DW	12.80 mm × 7.50 mm
	PDIP (20) – N	24.33 mm × 6.35 mm
SN74LS24x	SOP (20) – NS	7.80 mm × 12.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

'LS240, 'S240

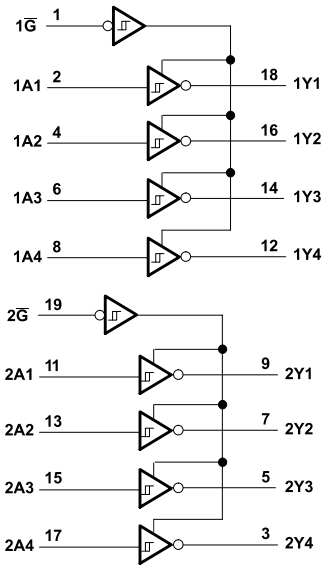


Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 5
6.5 Electrical Characteristics – SNx4LS24x ... 5
6.6 Electrical Characteristics – SNx4S24x ... 5
6.7 Switching Characteristics – SNx4LS24x ... 6
6.8 Switching Characteristics – SNx4S24x ... 6
6.9 Typical Characteristics ... 7
7 Parameter Measurement Information ... 7
7.1 SN54LS24x and SN74LS24x Devices ... 7
7.2 SN54S24x and SN74S24x Devices ... 9
8 Detailed Description ... 11
8.1 Overview ... 11
8.2 Functional Block Diagrams ... 11
8.3 Feature Description ... 12
8.4 Device Functional Modes ... 12
9 Application and Implementation ... 14
9.1 Application Information ... 14
9.2 Typical Application ... 14
9.3 System Examples ... 15
10 Power Supply Recommendations ... 17
11 Layout ... 17
11.1 Layout Guidelines ... 17
11.2 Layout Example ... 17
12 Device and Documentation Support ... 18
12.1 Related Links ... 18
12.2 Receiving Notification of Documentation Updates ... 18
12.3 Community Resource ... 18
12.4 Trademarks ... 18
12.5 Electrostatic Discharge Caution ... 18
12.6 Glossary ... 18
13 Mechanical, Packaging, and Orderable Information ... 19

4 Revision History

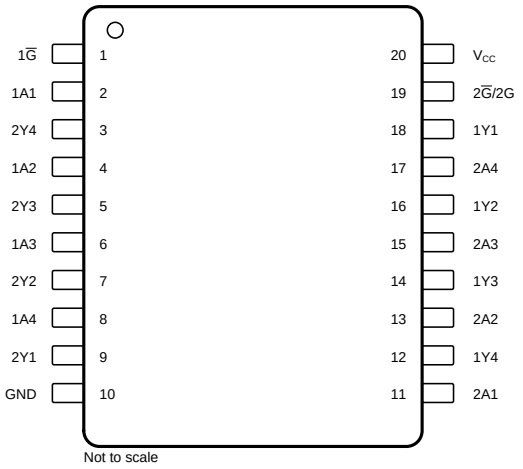
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2010) to Revision D **Page**

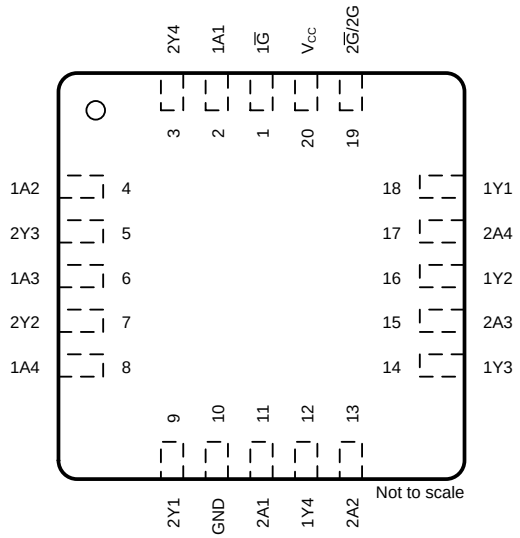
- Added *Applications* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted Ordering Information table; see POA at the end of the data sheet ... 1
- Changed $R\theta_{JA}$ values in the *Thermal Information* table from 70 to 94.3 (DB), from 58 to 90.3 (DW), from 69 to 50.6 (N), and from 60 to 76.6 (NS) ... 5

5 Pin Configuration and Functions

DB, DW, J, N, NS, or W Package
20-Pin SSOP, SOIC, CDIP, PDIP, SOP, or CFP
Top View



FK Package
20-Pin LCCC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$1\overline{G}$	I	Channel 1 output enable
2	1A1	I	Channel 1, A side 1
3	2Y4	O	Channel 2, Y side 4
4	1A2	I	Channel 1, A side 2
5	2Y3	O	Channel 2, Y side 3
6	1A3	I	Channel 1, A side 3
7	2Y2	O	Channel 2, Y side 2
8	1A4	I	Channel 1, A side 4
9	2Y1	O	Channel 2, Y side 1
10	GND	—	Ground
11	2A1	I	Channel 2, A side 1
12	1Y4	O	Channel 1, Y side 4
13	2A2	I	Channel 2, A side 2
14	1Y3	O	Channel 1, Y side 3
15	2A3	I	Channel 2, A side 3
16	1Y2	O	Channel 1, Y side 2
17	2A4	I	Channel 2, A side 4
18	1Y1	O	Channel 1, Y side 1
19	$2\overline{G}/2G$ (1)	I	Channel 2 output enable
20	V_{CC}	—	Power supply

(1) 2G for SNx4LS241 and SNx4S241 or $2\overline{G}$ for all other drivers.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}(2)			7	V
Input voltage, V_I	SNx4LS24x		7	V
	SNx4S24x		5.5	
Off-state output voltage			5.5	V
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
ALL PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	500	V
N PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage(1)	SN54xS24x	4.5	5	5.5	V
		SN74xS24x	4.75	5	5.25	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage	SN54LS24x			0.7	V
		SN54S24x, SN74xS24x			0.8	
I_{OH}	High-level output current	SN54xS24x			–12	mA
		SN74xS24x			–15	
I_{OL}	Low-level output current	SN54LS24x			12	mA
		SN54S24x			48	
		SN74LS24x			24	
		SN74S24x			64	
	External resistance between any input and V_{CC} or ground (SNx4S24x only)				40	kΩ
T_A	Operating free-air temperature(2)	SN54xS24x	–55		125	°C
		SN74xS24x	0		70	

(1) Voltage values are with respect to network ground terminal.
(2) An SN54S241J operating at free-air temperature above 116°C requires a heat sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more that 40°C/W.

6.4 Thermal Information

THERMAL METRIC[1]		SN74LS240, SN74LS244	SN74LS24x, SN74S24x		SN74LS24x	UNIT
		DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2][3]	94.3	90.3	50.6	76.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.9	45.5	37.4	42.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.5	48.1	31.5	44.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	21.3	19.4	24	19.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.1	47.6	31.4	43.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Voltage values are with respect to network ground terminal.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics – SNx4LS24x

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]			MIN	TYP[2]	MAX	UNIT
V_{IK}	V_{CC} = MIN, I_I = –18 mA					–1.5	V
Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN			0.2	0.4		V
V_{OH}	V_{CC} = MIN, I_{OH} = –3 mA, V_{IH} = 2 V, V_{IL} = MAX			2.4	3.4		V
	V_{CC} = MIN, I_{OH} = MAX, V_{IH} = 2 V, V_{IL} = 0.5 V			2			
V_{OL}	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V		I_{OL} = 12 mA, SN54LS24x			0.4	V
			I_{OL} = 24 mA, SN74LS24x			0.5	
I_{OZH}	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V, V_O = 2.7 V					20	µA
I_{OZL}	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V, V_O = 0.4 V					–20	µA
I_I	V_{CC} = MAX, V_I = 7 V					0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V					20	µA
I_{IL}	V_{CC} = MAX, V_{IL} = 0.4 V					–0.2	mA
I_{OS}[3]	V_{CC} = MAX			–40		–225	mA
I_{CC}	V_{CC} = MAX, output open	Outputs high	All		17	27	mA
		Outputs low	SNx4LS240		26	44	
			SNx4LS241, SNx4LS244		27	46	
		Outputs disabled	SNx4LS240		29	50	
			SNx4LS241, SNx4LS244		32	54	

(1) For conditions shown as minimum or maximum, use the appropriate value specified under recommended operating conditions.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) Not more than one output must be shorted at a time, and duration of the short-circuit must not exceed one second.

6.6 Electrical Characteristics – SNx4S24x

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]	MIN	TYP[2]	MAX	UNIT
V_{IK}	V_{CC} = MIN, I_I = –18 mA			–1.2	V
Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN	0.2	0.4		V
V_{OH}	V_{CC} = MIN, I_{OH} = –1 mA, V_{IH} = 2 V, V_{IL} = 0.8 V, SN74S24x only	2.7			V
	V_{CC} = MIN, I_{OH} = –3 mA, V_{IH} = 2 V, V_{IL} = 0.8 V	2.4	3.4		
	V_{CC} = MIN, I_{OH} = MAX, V_{IH} = 2 V, V_{IL} = 0.5 V	2			
V_{OL}	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V, I_{OL} = 0.8 V			0.55	V

(1) For conditions shown as minimum or maximum, use the appropriate value specified under recommended operating conditions.
(2) All typical values are at V_{CC} = 5 V, T_A = 25°C.

Electrical Characteristics – SNx4S24x (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]			MIN	TYP[2]	MAX	UNIT
I_{OZH}	V_{CC} = MAX, V_{IL} = 0.8 V, V_{IH} = 2 V, V_O = 2.4 V					50	µA
I_{OZL}	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V, V_O = 0.5 V					–50	µA
I_I	V_{CC} = MAX, V_I = 5.5 V					1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V					50	µA
I_{IL}	V_{CC} = MAX, V_{IL} = 0.5 V		Any A			–400	µA
			Any G			–2	mA
I_{OS}[3]	V_{CC} = MAX			–50		–225	mA
I_{CC}	V_{CC} = MAX, output open	Outputs high	SN54S240		80	123	mA
			SN74S240		80	135	
			SN54S241, SN54S244		95	147	
			SN74S241, SN74S244		95	160	
		Outputs low	SN54S240		100	145	
			SN74S240		100	150	
			SN54S241, SN54S244		120	170	
			SN74S241, SN74S244		120	180	
		Outputs disabled	SN54S240		100	145	
			SN74S240		100	150	
			SN54S241, SN54S244		120	170	
			SN74S241, SN74S244		120	180	

(3) Not more than one output must be shorted at a time, and duration of the short-circuit must not exceed one second.

6.7 Switching Characteristics – SNx4LS24x

V_{CC} = 5 V, T_A = 25°C (see *SN54LS24x and SN74LS24x Devices*)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	R_L = 667 Ω, C_L = 45 pF	SNx4LS240		9	14	ns
		SNx4LS241, SNx4LS244		12	18	
t_{PHL}	R_L = 667 Ω, C_L = 45 pF			12	18	ns
t_{PZL}	R_L = 667 Ω, C_L = 45 pF			20	30	ns
t_{PZH}	R_L = 667 Ω, C_L = 45 pF			15	23	ns
t_{PLZ}	R_L = 667 Ω, C_L = 5 pF			10	20	ns
t_{PHZ}	R_L = 667 Ω, C_L = 5 pF			15	25	ns

6.8 Switching Characteristics – SNx4S24x

V_{CC} = 5 V and T_A = 25°C (see *SN54S24x and SN74S24x Devices*)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	R_L = 90 Ω, C_L = 50 pF	SNx4S240		4.5	7	ns
		SNx4S241, SNx4S244		6	9	
t_{PHL}	R_L = 90 Ω, C_L = 50 pF	SNx4S240		4.5	7	ns
		SNx4S241, SNx4S244		6	9	
t_{PZL}	R_L = 90 Ω, C_L = 50 pF			10	15	ns
t_{PZH}	R_L = 90 Ω, C_L = 50 pF	SNx4S240		6.5	10	ns
		SNx4S241, SNx4S244		8	12	
t_{PLZ}	R_L = 90 Ω, C_L = 5 pF			10	15	ns
t_{PHZ}	R_L = 90 Ω, C_L = 5 pF			6	9	ns

6.9 Typical Characteristics

V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF, and R_L = 667 Ω (unless otherwise noted)

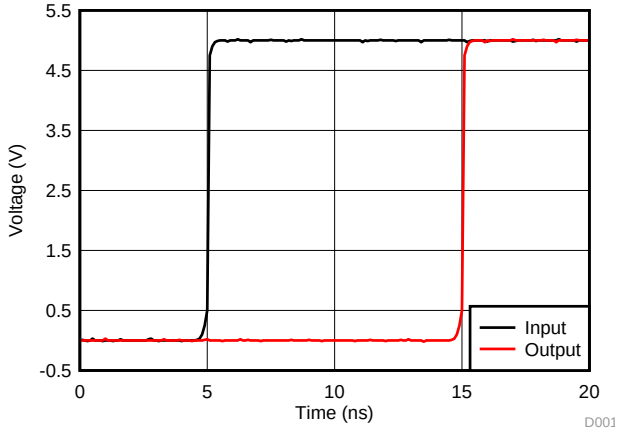


Figure 1. Simulated Propagation Delay From Input to Output

7 Parameter Measurement Information

7.1 SN54LS24x and SN74LS24x Devices

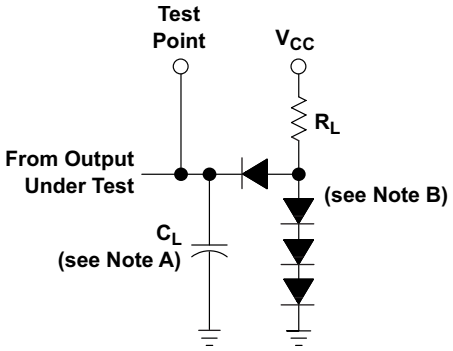


Figure 2. Load Circuit, For 2-State Totem-Pole Outputs

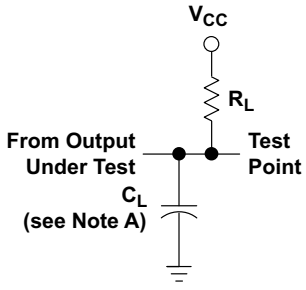


Figure 3. Load Circuit, For Open-Collector Outputs

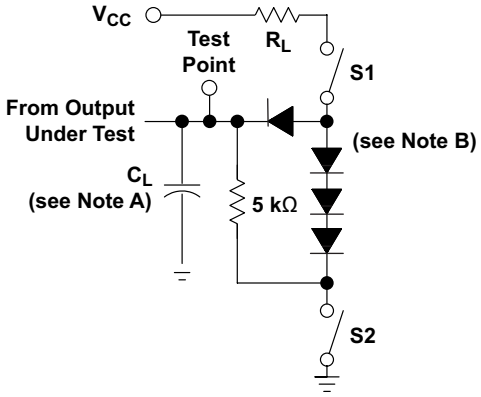


Figure 4. Load Circuit, For 3-State Outputs

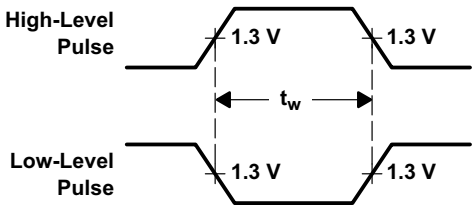


Figure 5. Voltage Waveforms, Pulse Durations

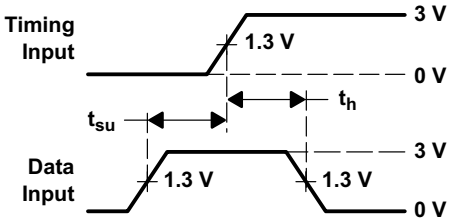


Figure 6. Voltage Waveforms, Setup and Hold Times

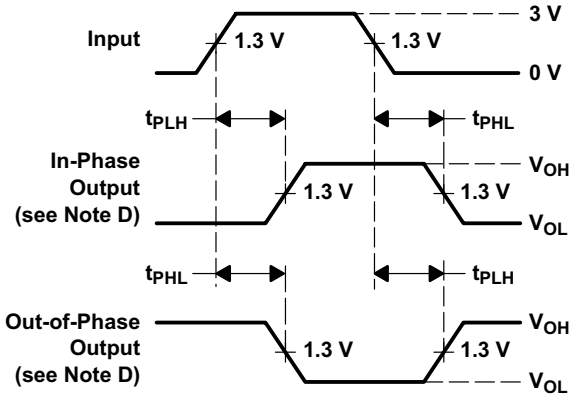
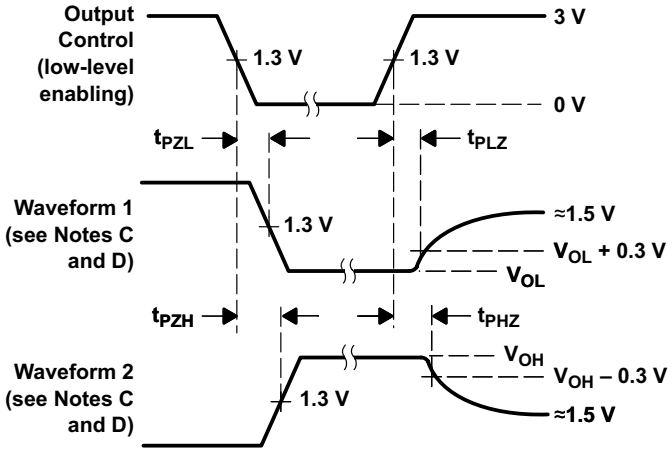


Figure 7. Voltage Waveforms, Propagation Delay Times



A. C_L includes probe and jig capacitance.

B. All diodes are 1N3064 or equivalent.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.

E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O is approximately 50 Ω, t_r ≤ 15 ns, t_f ≤ 6 ns.

G. The outputs are measured one at a time with one input transition per measurement.

Figure 8. Voltage Waveforms, Enable and Disable Times, 3-State Outputs

7.2 SN54S24x and SN74S24x Devices

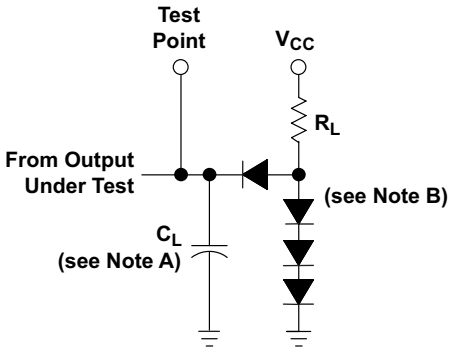


**Figure 9. Load Circuit,
For 2-State Totem-Pole Outputs**

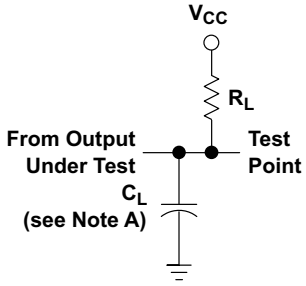


**Figure 10. Load Circuit,
For Open-Collector Outputs**

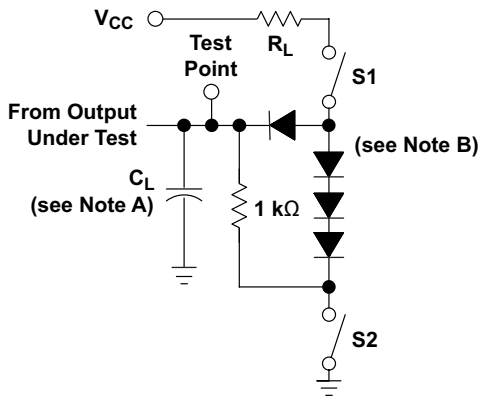


**Figure 11. Load Circuit,
For 3-State Outputs**

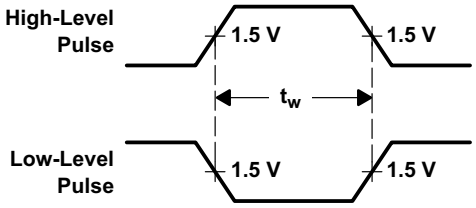


**Figure 12. Voltage Waveforms,
Pulse Durations**

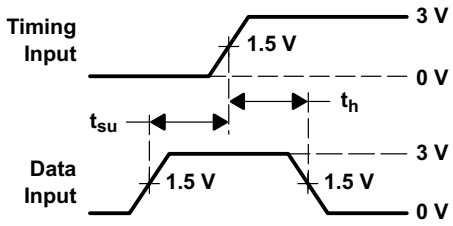


**Figure 13. Voltage Waveforms,
Setup and Hold Times**

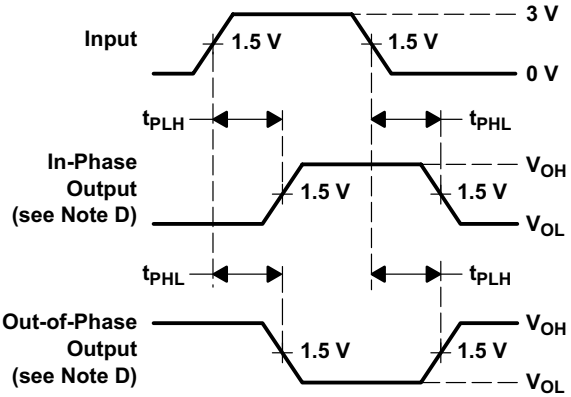
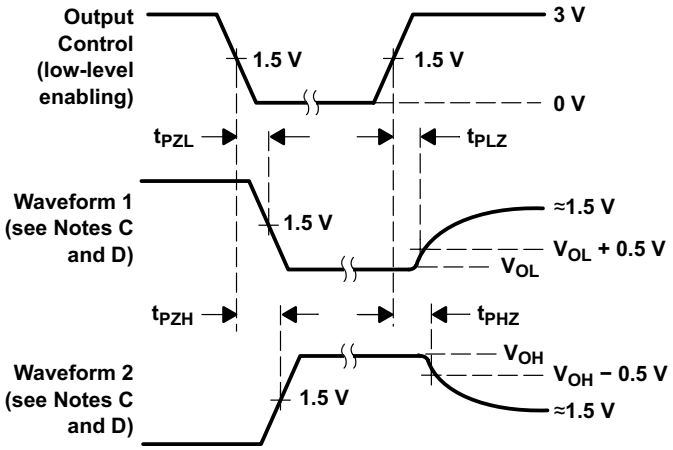


**Figure 14. Voltage Waveforms,
Propagation Delay Times**



A. C_L includes probe and jig capacitance.

B. All diodes are 1N3064 or equivalent.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.

E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O is approximately 50 Ω; t_r and t_f ≤ 7 ns for SN54LS24x and SN74LS24x devices, and t_r and t_f ≤ 2.5 ns for SN54S24x and SN74S24x devices.

F. The outputs are measured one at a time with one input transition per measurement.

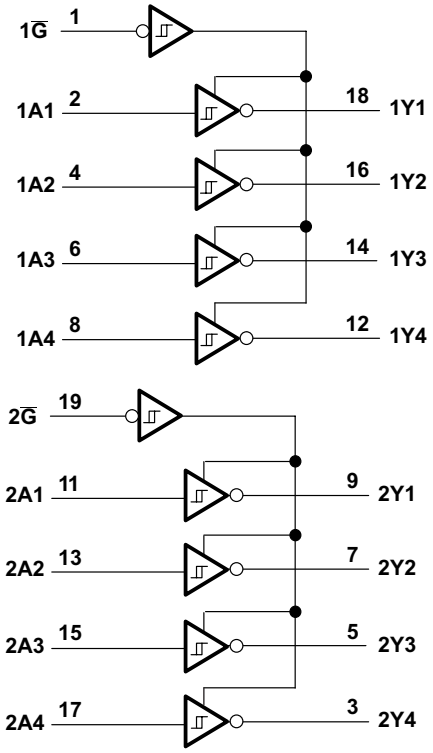
Figure 15. Voltage Waveforms, Enable and Disable Times, 3-State Outputs

8 Detailed Description

8.1 Overview

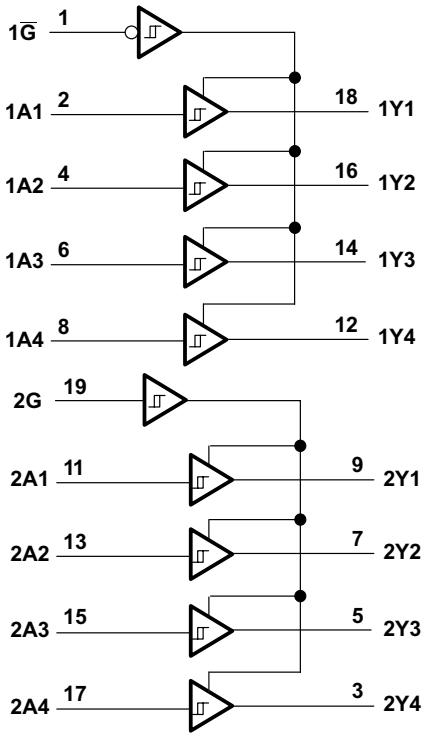
This device is organized as two 4-bit buffers and drivers with separate output-enable ($\overline{G}$) inputs. When $\overline{G}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{G}$ is high, the outputs are in the high impedance state. Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V and 5-V system environment. To ensure the high-impedance state during power up or power down, $\overline{G}$ must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagrams



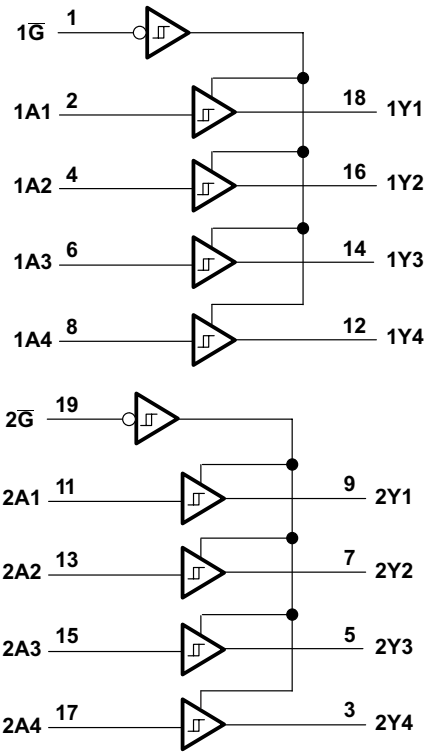
Pin numbers shown are for DB, DW, J, N, NS, and W packages

Figure 16. SNx4LS240 and SNx4S240 Logic Diagram



Pin numbers shown are for DB, DW, J, N, NS, and W packages

Figure 17. SNx4LS241 and SNx4S241 Logic Diagram



Pin numbers shown are for DB, DW, J, N, NS, and W packages

Figure 18. SNx4LS244 and SNx4S244 Logic Diagram

8.3 Feature Description

8.3.1 3-State Outputs

The 3-state outputs can drive bus lines directly. All outputs can be put into high impedance mode through the $\overline{G}$ pin.

8.3.2 PNP Inputs

This device has PNP inputs which reduce dc loading on bus lines.

8.3.3 Hysteresis on Bus Inputs

The bus inputs have built-in hysteresis that improves noise margins.

8.4 Device Functional Modes

The SNx4LS24x and SNx4S24x devices can be used as inverting and non-inverting bus buffers for data line transmission and can isolate input to output by setting the $\overline{G}$ pin HIGH. Table 1, Table 2, and Table 3 list the function tables for all devices.

Table 1. SNx4LS240 and SNx4S240 Function Table

INPUTS		OUTPUTS
$\overline{G}$	A	Y
L	L	H
L	H	L
H	X	Z

Table 2. SNx4LS241 and SNx4S241 Function Table

CHANNEL 1			CHANNEL 2		
INPUTS		OUTPUT	INPUTS		OUTPUT
$1\overline{G}$	1A	1Y	2G	2A	2Y
L	L	L	H	L	L
L	H	H	H	H	H
H	X	Z	L	X	Z

Table 3. SNx4LS244 and SNx4S244 Function Table

INPUTS		OUTPUTS
$\overline{G}$	A	Y
L	L	L
L	H	H
H	X	Z

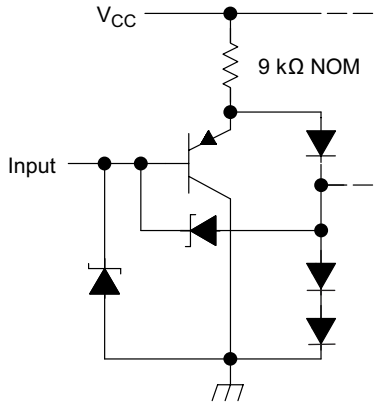
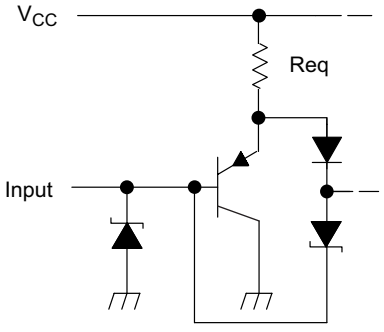


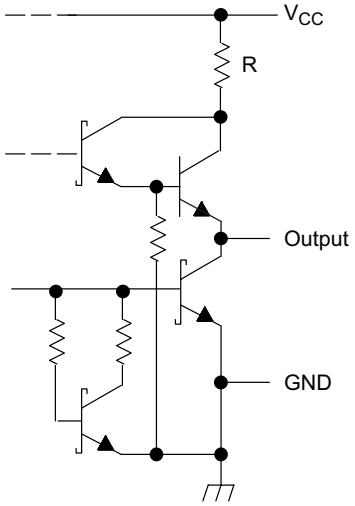
Figure 19. SNx4LS240, SNx4LS241, SNx4LS244 Equivalent of Each Input



G and $\overline{G}$ inputs: R_{eq} = 2 kΩ NOM

A inputs: R_{eq} = 2.8 kΩ NOM

Figure 20. SNx4S240, SNx4S241, SNx4S244 Equivalent of Each Input



SNx4LS240, SNx4LS241, SNx4LS244:
R = 50 Ω NOM

SNx4S240, SNx4S241, SNx4S244:
R = 25 Ω NOM

Figure 21. Typical of All Outputs

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SNx4LS24x, SNx4S24x octal buffers and line drivers are designed to be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

9.2 Typical Application

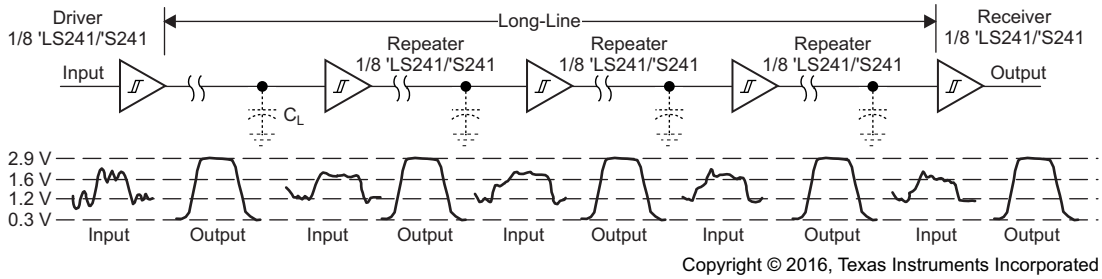


Figure 22. SNx4LS241 and SNx4S241 Used as Repeater or Level Restorer

9.2.1 Design Requirements

This device uses Schottky transistor logic technology. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- Power Supply
  - Each device must maintain a supply voltage between 4.5 V and 5.5 V.
- Inputs
  - Input signals must meet the V_{IH} and V_{IL} specifications in *Electrical Characteristics – SNx4LS24x*.
  - Inputs leakage values (I_I, I_{IH}, I_{IL}) from *Electrical Characteristics – SNx4LS24x* must be considered.
- Outputs
  - Output signals are specified to meet the V_{OH} and V_{OL} specifications in *Electrical Characteristics – SNx4LS24x* as a minimum (the values could be closer to V_{CC} for high signals or GND for low signals).
  - TI recommends maintaining output currents as specified in *Recommended Operating Conditions*.
  - The part can be damaged by sourcing or sinking too much current (see *Electrical Characteristics – SNx4LS24x* for details).

Typical Application (continued)

9.2.3 Application Curve

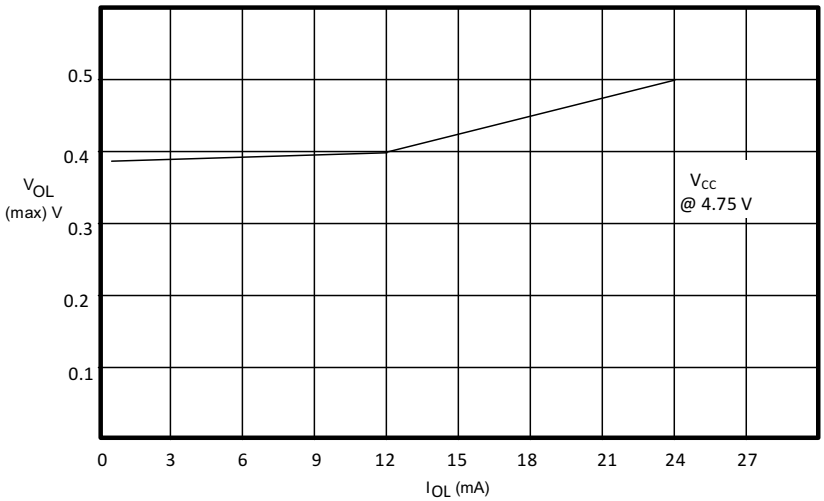
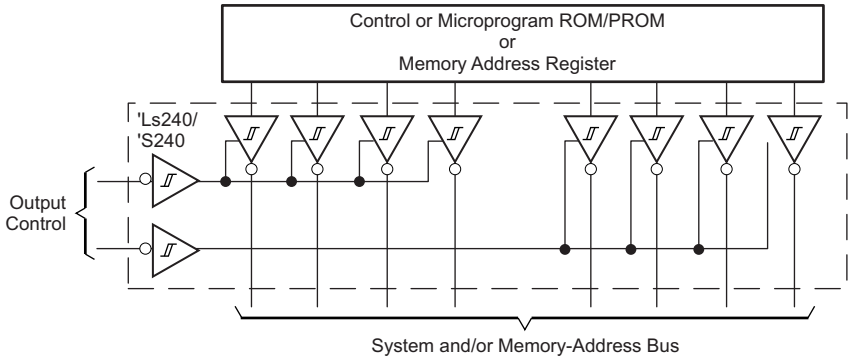


Figure 23. V_{OL} vs I_{OL}

9.3 System Examples

The SNx4LS240 and SNx4S240 devices can be used to buffer signals along a memory bus. The increased output drive helps data transmission reliability. Figure 24 shows a schematic of this example.



4-bit organization can be applied to handle binary or BCD

Figure 24. SNx4LS240 and SNx4S240 Used as System or Memory Bus Driver

The SNx4LS240 and SNx4S240 devices have two independently controlled 4-bit drivers, and can be used to buffer signals in a bidirectional manner along a data bus. Figure 25 shows the SNx4LS240 or SNx4S240 used in this manner.

System Examples (continued)

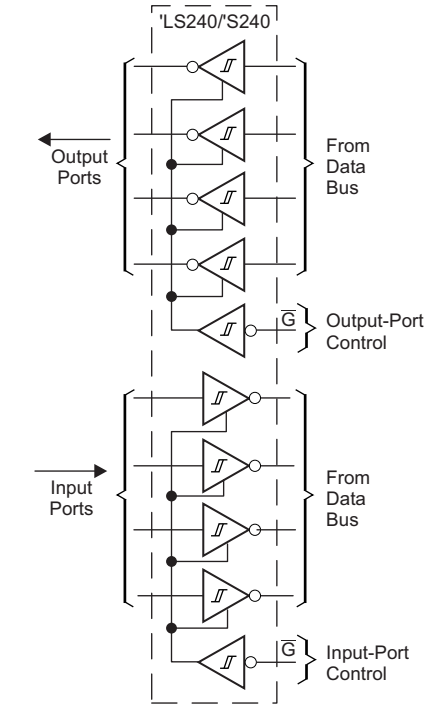


Figure 25. Independent 4-Bit But Drivers/Receivers in a Single Package

The enable pins on the SNx4LS241 and SNx4S241 devices can be used to help direct signals along a shared party-line bus. Figure 26 shows a general configuration of how to implement this structure. Take care to ensure that bus contention does not occur.

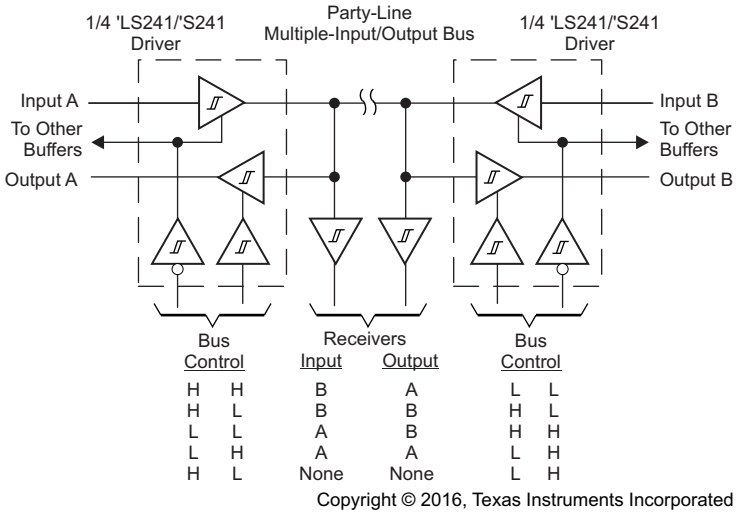


Figure 26. Party-Line Bus System With Multiple Inputs, Outputs, and Receivers

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*. Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF bypass capacitor. If there are multiple V_{CC} pins, TI recommends a 0.01-µF or 0.022-µF bypass capacitors for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. Two bypass capacitors of value 0.1 µF and 1 µF are commonly used in parallel. For best results, install the bypass capacitor(s) as close to the power pin as possible.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs must not be left floating. In many applications, some channels of the SNx4LS24x, SNx4S24x are unused, and thus must be terminated properly. Because each transceiver channel pin can be either an input or an output, they must be treated as both when being terminated. Ground or V_{CC} (whichever is more convenient) can be used to terminate unused inputs; however, each unused channel should be terminated to the same logic level on both the A and Y side. For example, in Figure 27 unused channels are terminated correctly with both sides connected to the same voltage, while channel 8 is terminated incorrectly with each side being tied to a different voltage. The $\overline{G}$ input is also unused in this example, and is terminated directly to ground to permanently enable all outputs.

11.2 Layout Example

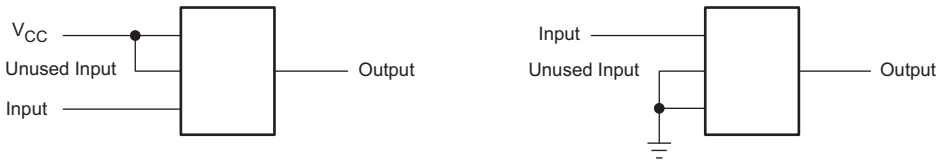


Figure 27. Example Demonstrating How to Terminate Unused Inputs and Channels of a Transceiver

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	SUPPORT & COMMUNITY
SN54LS240	Click here	Click here	Click here	Click here
SN74LS241	Click here	Click here	Click here	Click here
SN74LS244	Click here	Click here	Click here	Click here
SN54S240	Click here	Click here	Click here	Click here
SN54S241	Click here	Click here	Click here	Click here
SN54S244	Click here	Click here	Click here	Click here
SN74LS240	Click here	Click here	Click here	Click here
SN74LS241	Click here	Click here	Click here	Click here
SN74LS244	Click here	Click here	Click here	Click here
SN74S240	Click here	Click here	Click here	Click here
SN74S241	Click here	Click here	Click here	Click here
SN74S241	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-7801201VSA	ACTIVE	CFP	W	20	25	TBD	A42	N / A for Pkg Type	-55 to 125	5962-7801201VS A SNV54LS240W	Samples
7705701RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7705701RA SNJ54LS244J	Samples
7705701SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7705701SA SNJ54LS244W	Samples
78012012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	78012012A SNJ54LS 240FK	Samples
7801201RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7801201RA SNJ54LS240J	Samples
7801201SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7801201SA SNJ54LS240W	Samples
JM38510/32401B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32401B2A	Samples
JM38510/32401BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32401BRA	Samples
JM38510/32401BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32401BSA	Samples
JM38510/32402B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32402B2A	Samples
JM38510/32402BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32402BRA	Samples
JM38510/32402BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32402BSA	Samples
JM38510/32403B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32403B2A	Samples
JM38510/32403BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32403BRA	Samples
JM38510/32403BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32403BSA	Samples
JM38510/32403SRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32403SRA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/32403SSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32403SSA	Samples
M38510/32401B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32401B2A	Samples
M38510/32401BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32401BRA	Samples
M38510/32401BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32401BSA	Samples
M38510/32402B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32402B2A	Samples
M38510/32402BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32402BRA	Samples
M38510/32402BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32402BSA	Samples
M38510/32403B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32403B2A	Samples
M38510/32403BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32403BRA	Samples
M38510/32403BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32403BSA	Samples
M38510/32403SRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32403SRA	Samples
M38510/32403SSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32403SSA	Samples
SN54LS240J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS240J	Samples
SN54LS241J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS241J	Samples
SN54LS244J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS244J	Samples
SN54S240J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S240J	Samples
SN54S241J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S241J	Samples
SN54S244J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S244J	Samples
SN74LS240DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		LS240	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS240DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS240	Samples
SN74LS240DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS240	Samples
SN74LS240DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS240	Samples
SN74LS240DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS240	Samples
SN74LS240N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS240N	Samples
SN74LS240NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS240N	Samples
SN74LS240NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS240	Samples
SN74LS241DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS241	Samples
SN74LS241DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS241	Samples
SN74LS241DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS241	Samples
SN74LS241N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS241N	Samples
SN74LS241NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS241	Samples
SN74LS244DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS244	Samples
SN74LS244DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS244	Samples
SN74LS244DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS244	Samples
SN74LS244DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS244	Samples
SN74LS244DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS244	Samples
SN74LS244DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS244	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS244DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS244	Samples
SN74LS244DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS244	Samples
SN74LS244N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS244N	Samples
SN74LS244NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS244N	Samples
SN74LS244NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS244	Samples
SN74LS244NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS244	Samples
SN74S240DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S240	Samples
SN74S240DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S240	Samples
SN74S240DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S240	Samples
SN74S240N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S240N	Samples
SN74S240NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S240N	Samples
SN74S241DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S241	Samples
SN74S241N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S241N	Samples
SN74S244DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S244	Samples
SN74S244DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S244	Samples
SN74S244DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S244	Samples
SN74S244N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S244N	Samples
SNJ54LS240FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	78012012A SNJ54LS	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										240FK	
SNJ54LS240J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7801201RA SNJ54LS240J	Samples
SNJ54LS240W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7801201SA SNJ54LS240W	Samples
SNJ54LS241FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 241FK	Samples
SNJ54LS241J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS241J	Samples
SNJ54LS241W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS241W	Samples
SNJ54LS244FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 244FK	Samples
SNJ54LS244J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7705701RA SNJ54LS244J	Samples
SNJ54LS244W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7705701SA SNJ54LS244W	Samples
SNJ54S240FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 240FK	Samples
SNJ54S240J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S240J	Samples
SNJ54S240W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S240W	Samples
SNJ54S241FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 241FK	Samples
SNJ54S241J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S241J	Samples
SNJ54S244J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S244J	Samples
SNJ54S244W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S244W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54LS240, SN54LS240-SP, SN54LS241, SN54LS244, SN54LS244-SP, SN54S240, SN54S241, SN54S244, SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 :

- Catalog: SN74LS240, SN54LS240, SN74LS241, SN74LS244, SN54LS244, SN74S240, SN74S241, SN74S244
- Military: SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
- Space: SN54LS240-SP, SN54LS244-SP

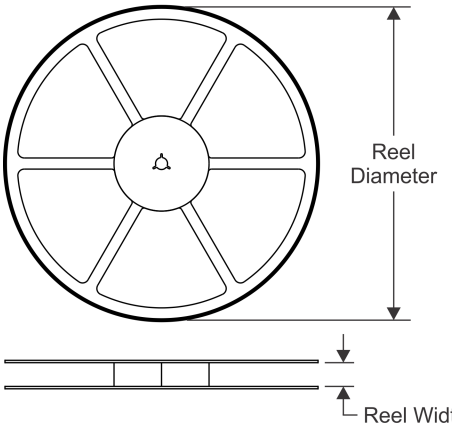
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

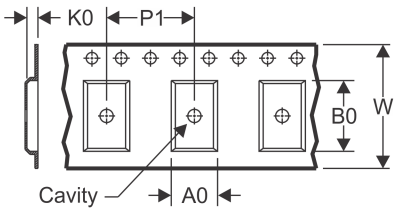
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

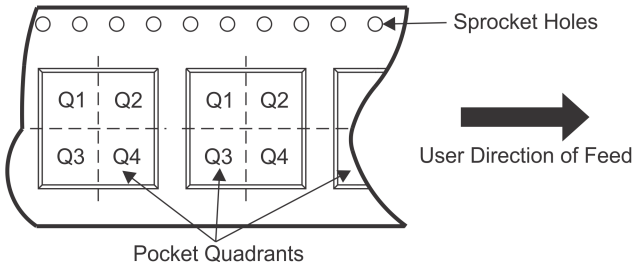


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

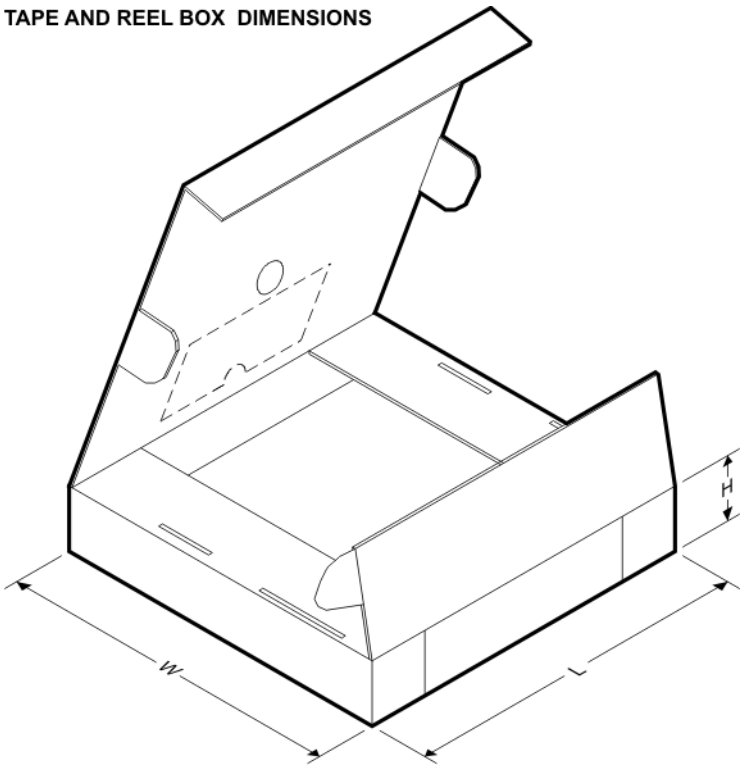
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS240DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LS240DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS240NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	12.0	24.0	Q1
SN74LS241DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS241NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	12.0	24.0	Q1
SN74LS244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LS244DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS244NSR	SO	NS	20	2000	330.0	24.4	9.0	13.0	2.4	12.0	24.0	Q1
SN74S240DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74S244DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

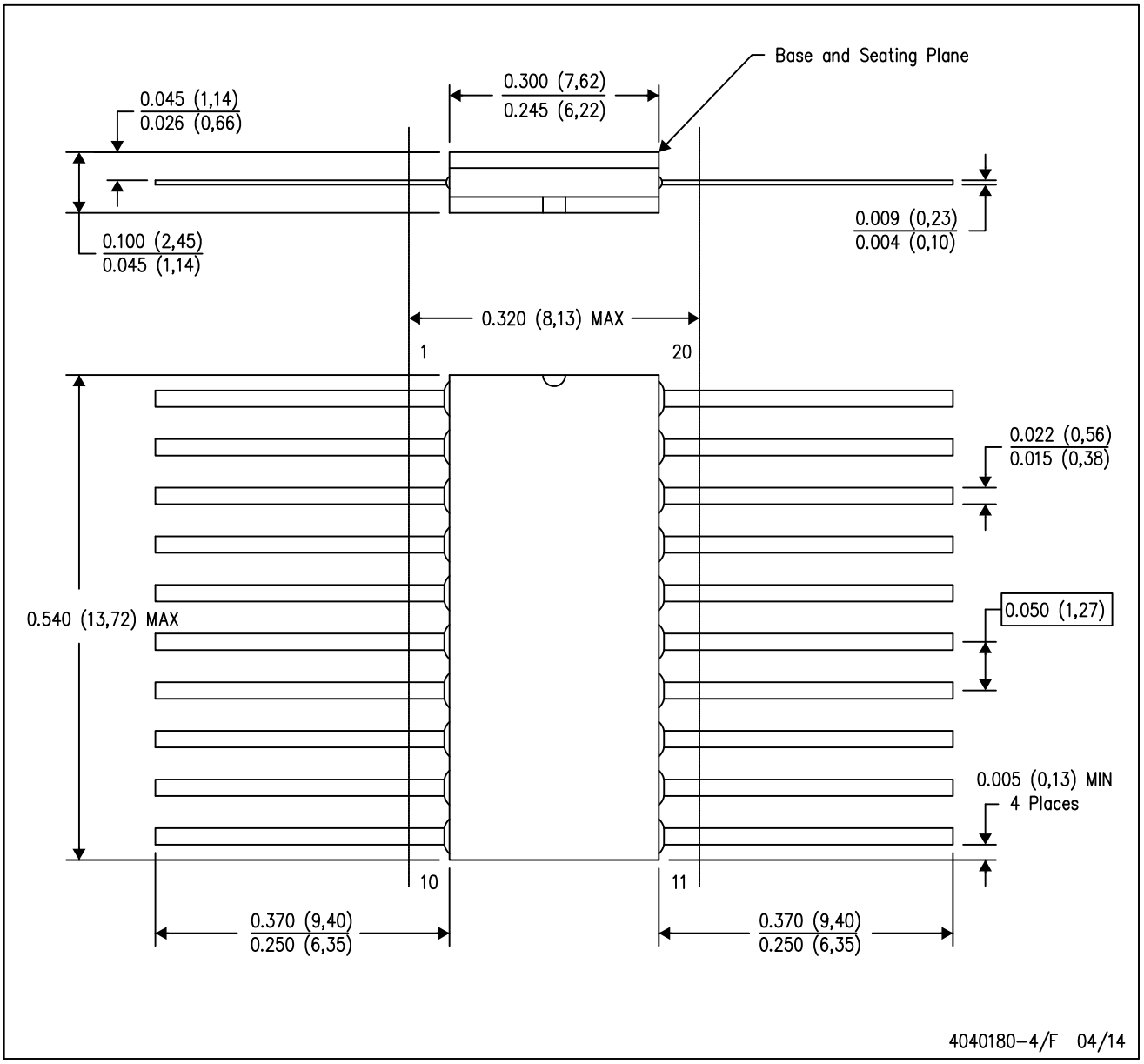
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS240DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LS240DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS240NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LS241DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS241NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LS244DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LS244DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS244NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74S240DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74S244DWR	SOIC	DW	20	2000	367.0	367.0	45.0

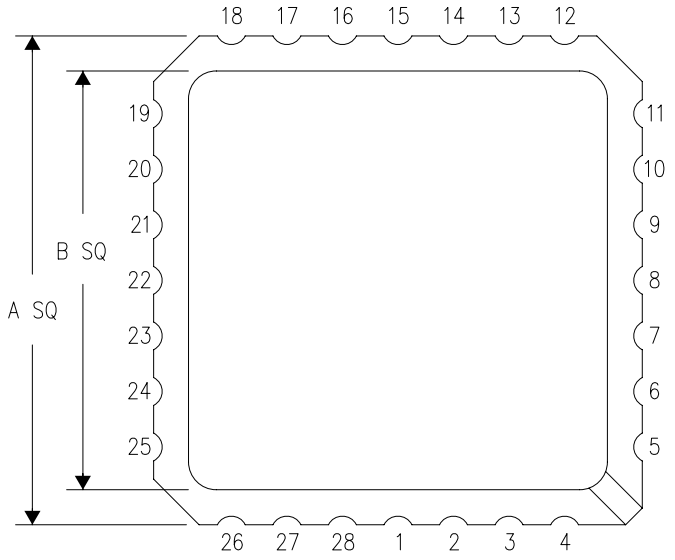
W (R–GDFP–F20) CERAMIC DUAL FLATPACK



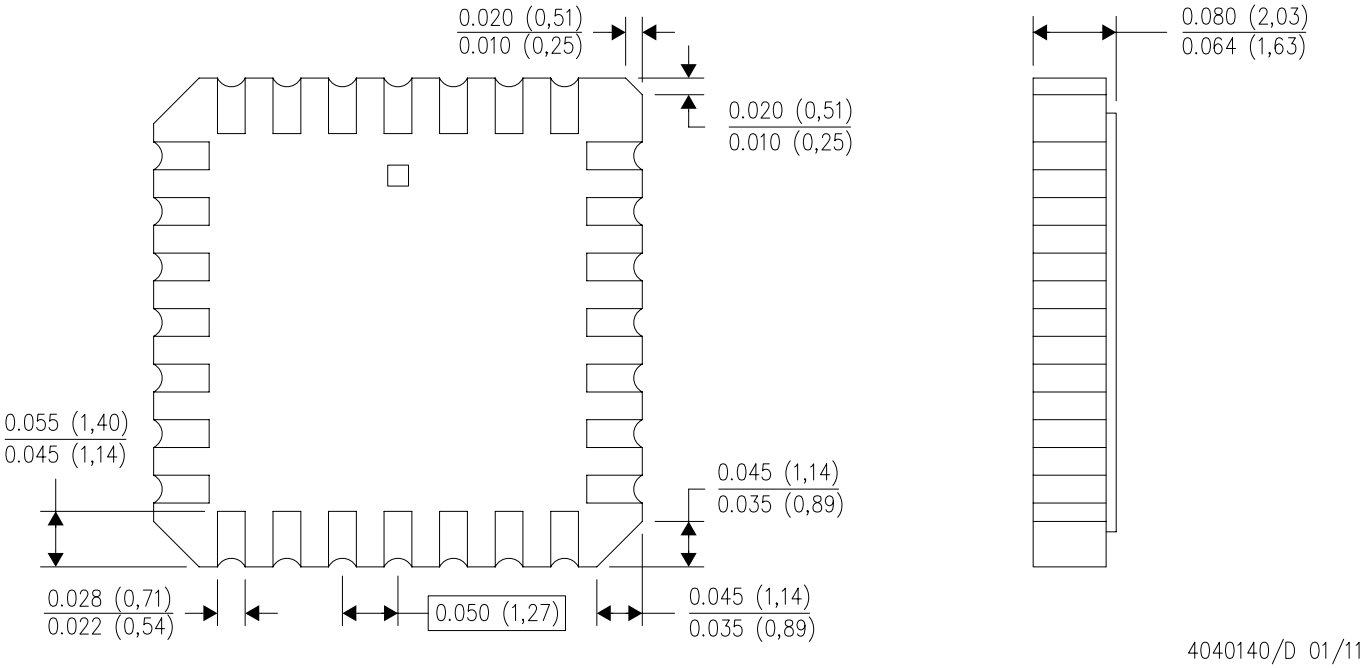
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



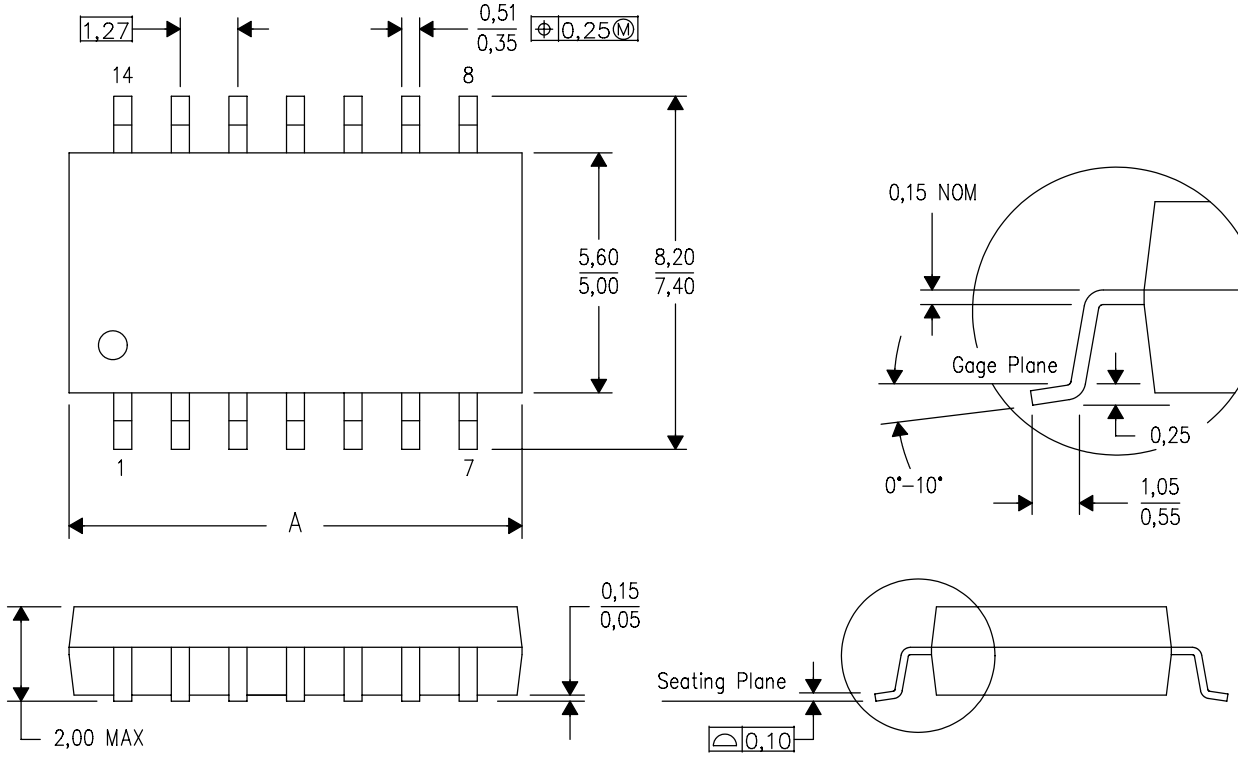
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

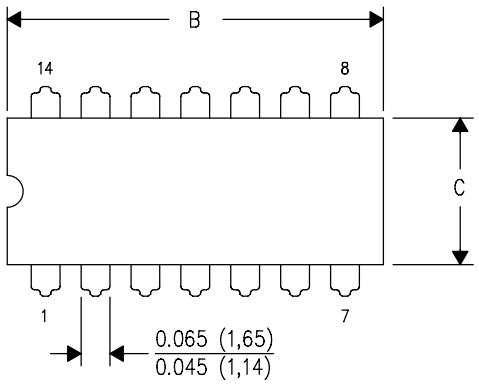
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

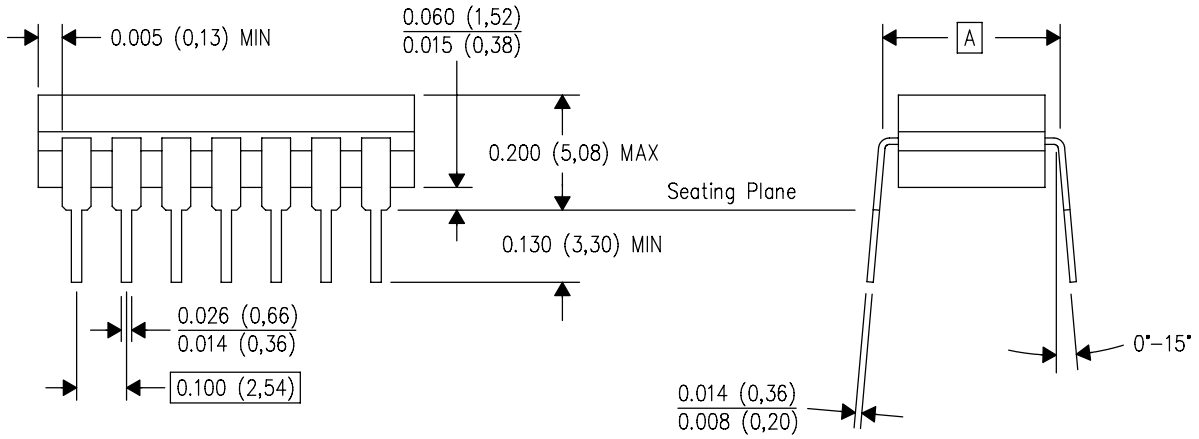
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



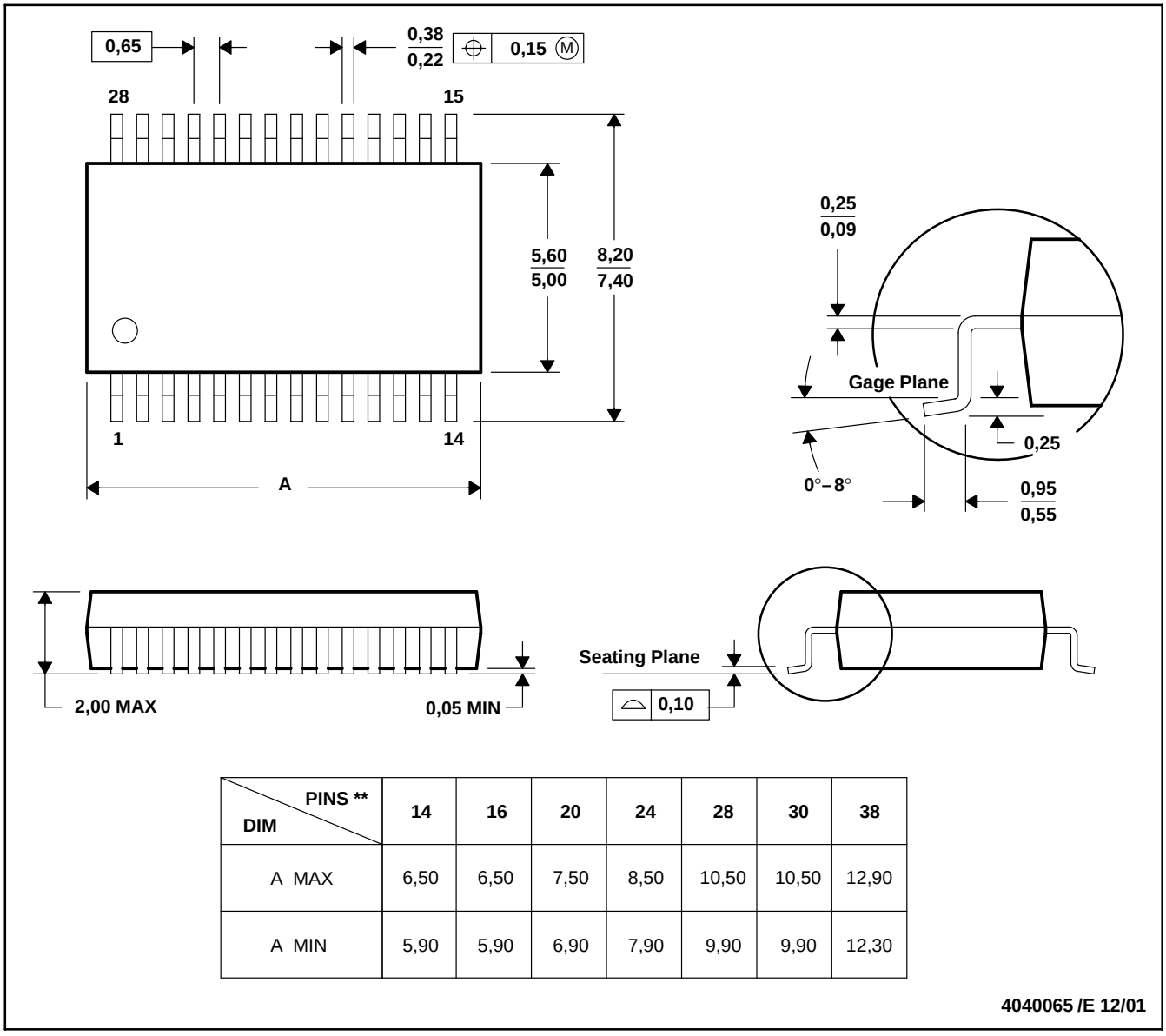
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

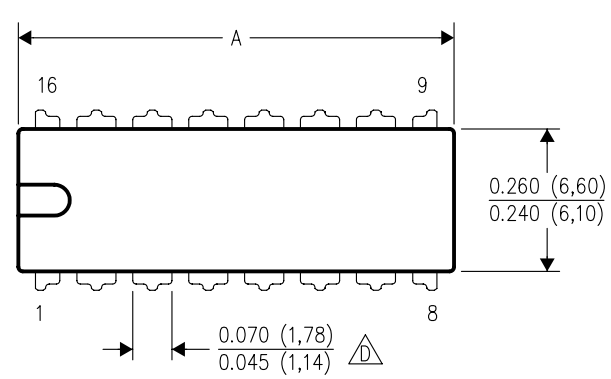
4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

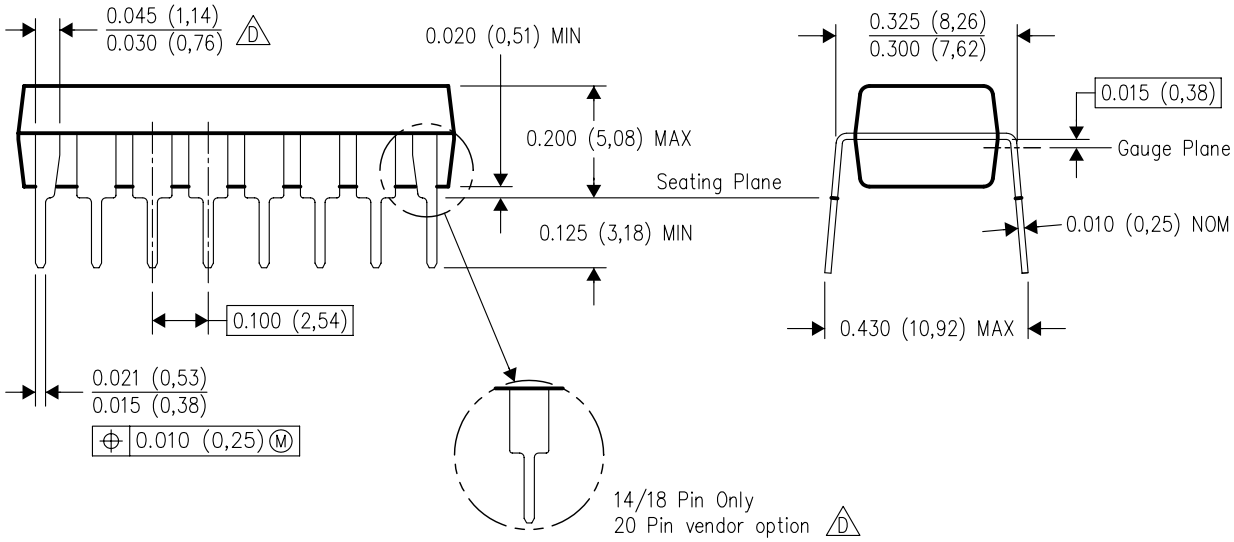
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

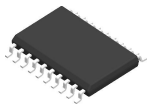


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

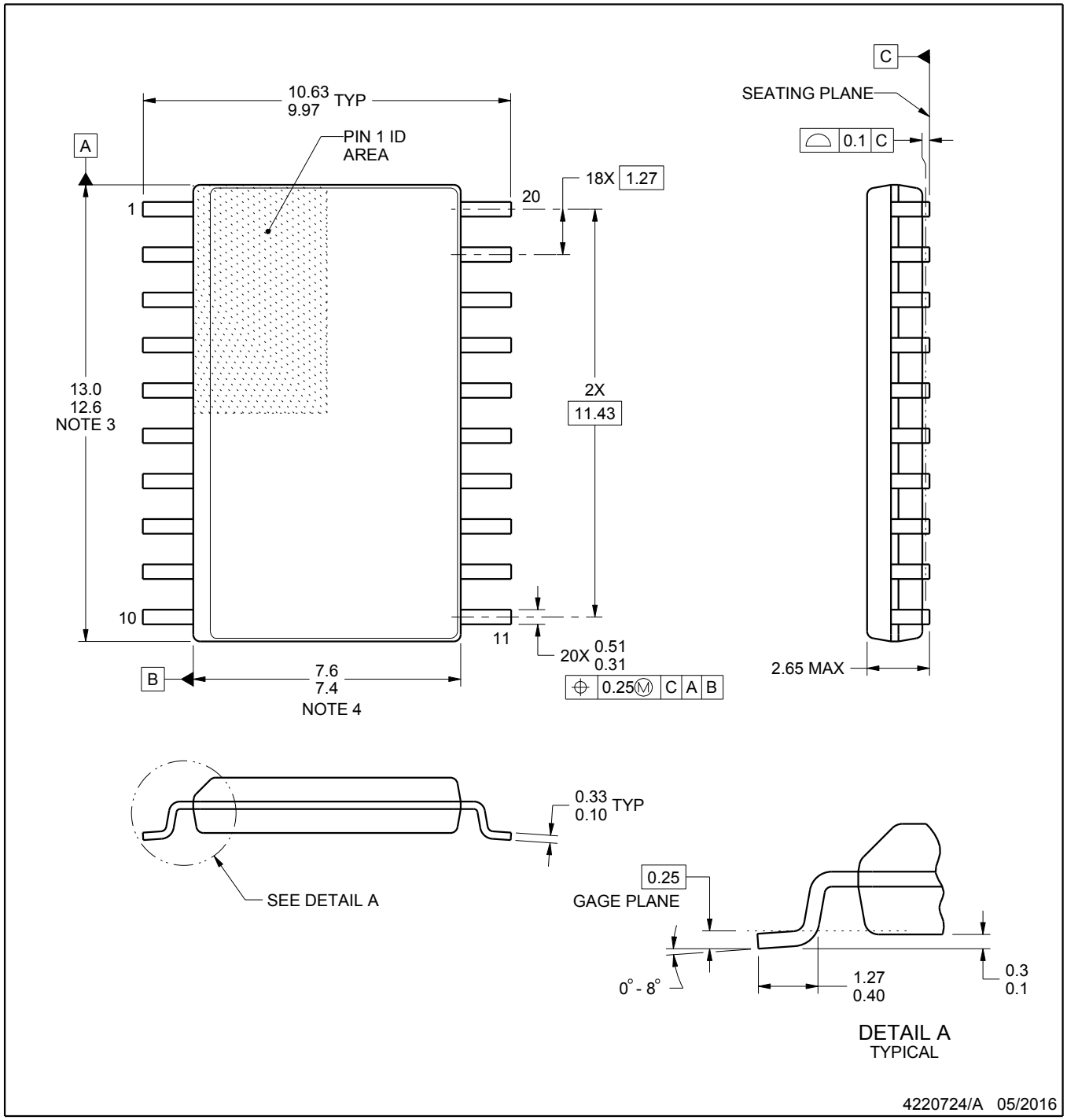


PACKAGE OUTLINE

DW0020A

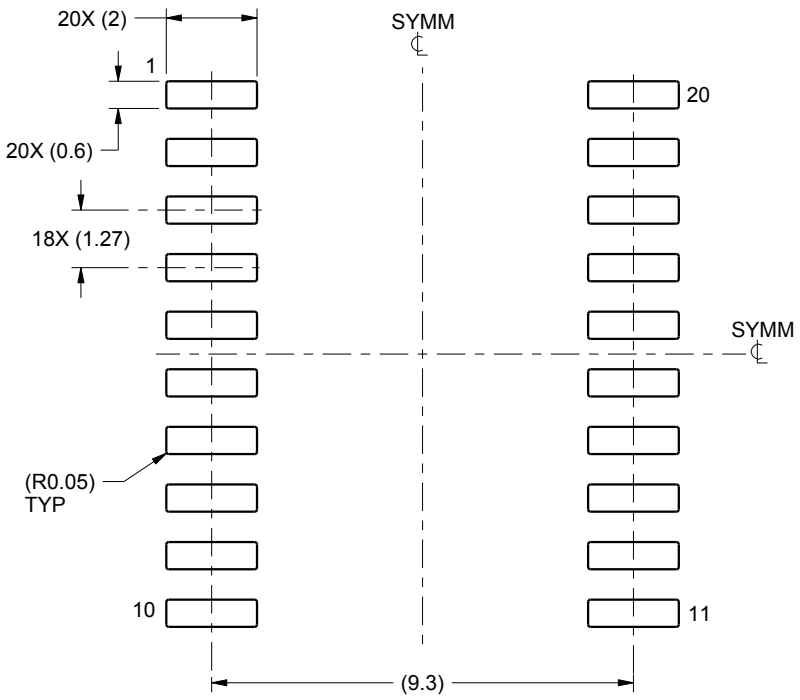
SOIC - 2.65 mm max height

SOIC

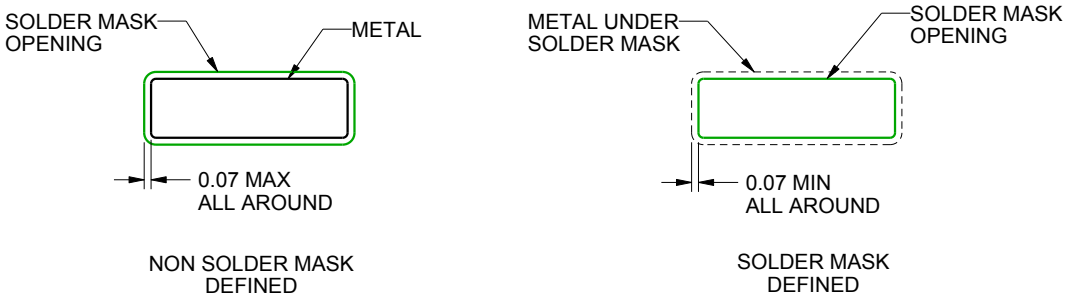


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

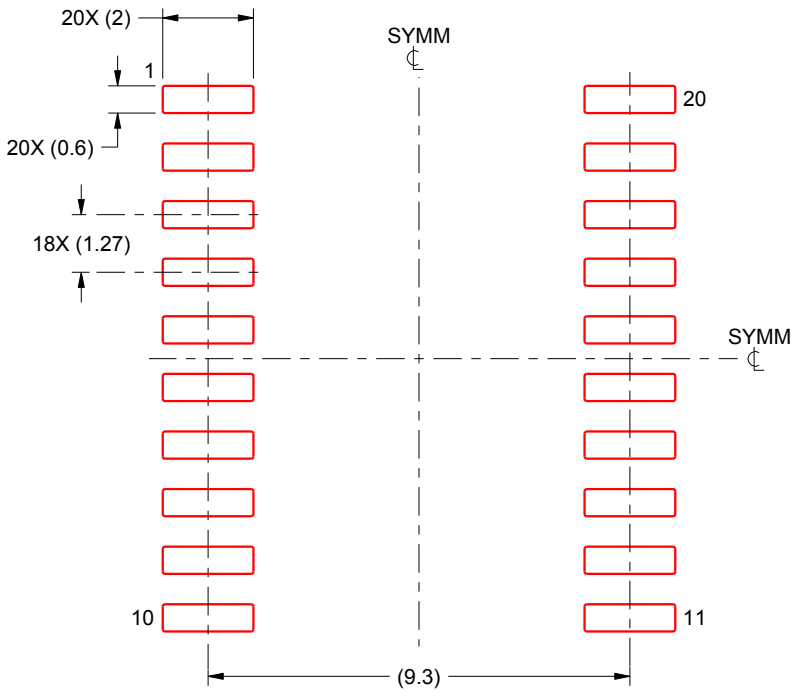


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265