OPAx340 Single-Supply, Rail-to-Rail Operational Amplifiers MicroAmplifier™ Series

1 Features

- Rail-to-Rail Input
- Rail-to-Rail Output (Within 1 mV)
- *Micro*Size Packages
- Wide Bandwidth: 5.5 MHz
- High Slew Rate: 6 V/µs
- Low THD + Noise: 0.0007% (f = 1 kHz)
- Low Quiescent Current: 750 µA/Channel
- Single, Dual, and Quad Versions

2 Applications

- Driving A/D Converters
- PCMCIA Cards
- Data Acquisition
- Process Control
- Audio Processing
- Communications
- Active Filters
- Test Equipment

3 Description

The OPA340 series rail-to-rail CMOS operational amplifiers are optimized for low-voltage, single-supply operation. Rail-to-rail input and output and high-speed operation make them ideal for driving sampling analog-to-digital (A/D) converters. They are also well-suited for general purpose and audio applications as well as providing I/V conversion at the output of digital-to-analog (D/A) converters. Single, dual, and quad versions have identical specifications for design flexibility.

The OPA340 series operate on a single supply as low as 2.5 V with an input common-mode voltage range that extends 500 mV below ground and 500 mV above the positive supply. Output voltage swing is to within 1 mV of the supply rails with a 100-kΩ load. These devices offer excellent dynamic response (BW = 5.5 MHz, SR = 6 V/µs), yet quiescent current is only 750 A. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

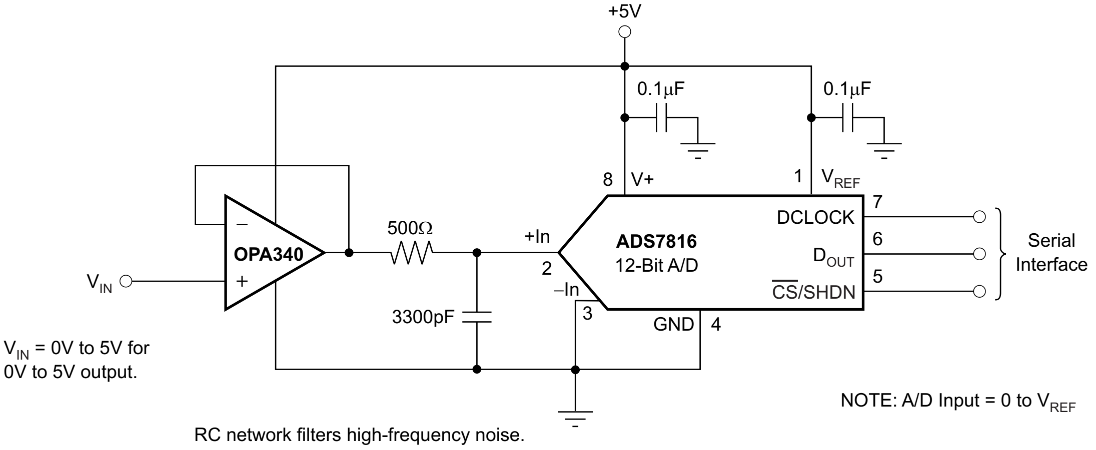
The single (OPA340) packages are the tiny 5-pin SOT-23 surface mount, 8-pin SOIC surface mount, and 8-pin DIP. The dual (OPA2340) comes in the miniature 8-pin VSSOP surface mount, 8-pin SOIC surface mount, and 8-pin PDIP packages. The quad (OPA4340) packages are the space-saving 16-pin SSOP surface mount and 14-pin SOIC surface mount. All are specified from –40°C to 85°C and operate from –55°C to 125°C. A SPICE macromodel is available for design analysis.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA340	SOT-23 (5)	3.00 mm × 3.00 mm
OPA340, OPA2340	PDIP (8)	9.81 mm × 6.35 mm
	SOIC (8)	4.90 mm × 3.91 mm
OPA2340	VSSOP (8)	3.00 mm × 3.00 mm
OPA4340	SOIC (14)	8.65 mm × 3.91 mm
	SSOP (16)	4.90 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

OPA340 in Noninverting Configuration Driving ADS7816



V_{IN} = 0V to 5V for 0V to 5V output.

RC network filters high-frequency noise.

NOTE: A/D Input = 0 to V_{REF}

Table of Contents

---

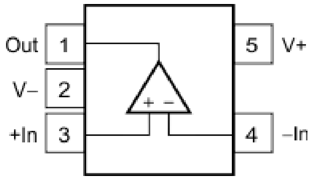
4 Revision History

Changes from Revision B (November 2007) to Revision C **Page**

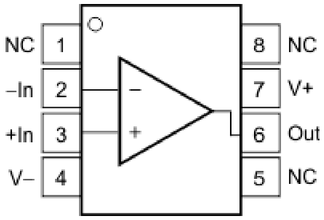
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Deleted *Package/Ordering Information* table, see POA at the end of the data sheet. 1

5 Pin Configuration and Functions

OPA340: DBV Package
5-Pin SOT-23
Top View



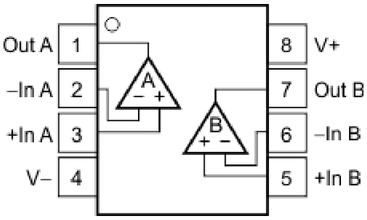
OPA340: P and D Packages
8-Pin PDIP and SOIC
Top View



Pin Functions: OPA340

PIN			I/O	DESCRIPTION
NAME	SOT-23	SOIC, PDIP		
–IN	4	2	I	Negative (inverting) input
+IN	3	3	I	Positive (noninverting) input
NC	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	1	6	O	Output
V–	2	4	—	Negative (lowest) power supply
V+	5	7	—	Positive (highest) power supply

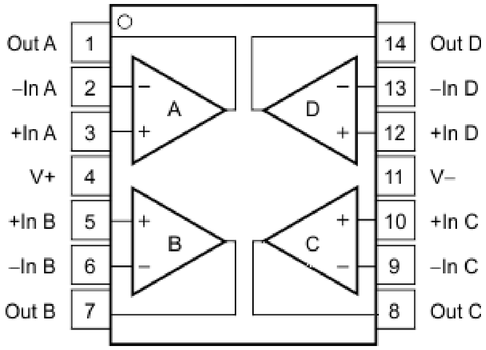
OPA2340: P, D, and DGK Packages
8-Pin PDIP, SOIC, and VSSOP
Top View



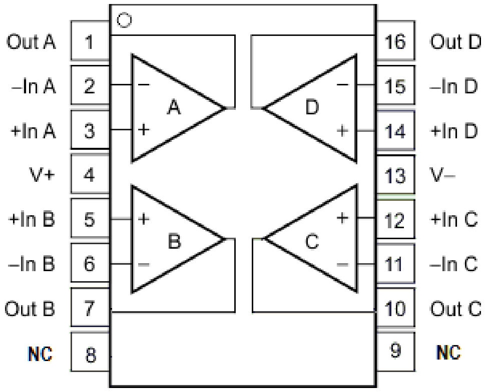
Pin Functions: OPA2340

PIN		I/O	DESCRIPTION
NAME	VSSOP, SOIC, PDIP		
–IN A	2	I	Negative (inverting) input channel A
+IN A	3	I	Positive (noninverting) input channel A
–IN B	6	I	Negative (inverting) input channel B
+IN B	5	I	Positive (noninverting) input channel B
OUT A	1	O	Output channel A
OUT B	7	O	Output channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

OPA4340: D Package
14-Pin SOIC
Top View



OPA4340: DBQ Package
16-Pin SSOP
Top View



Pin Functions: OPA4340

PIN			I/O	DESCRIPTION
NAME	SOIC	SSOP		
–IN A	2	2	I	Negative (inverting) input channel A
–IN B	6	6	I	Negative (inverting) input channel B
–IN C	9	11	I	Negative (inverting) input channel C
–IN D	13	15	I	Negative (inverting) input channel D
+IN A	3	3	I	Positive (noninverting) input channel A
+IN B	5	5	I	Positive (noninverting) input channel B
+IN C	10	12	I	Positive (noninverting) input channel C
+IN D	12	14	I	Positive (noninverting) input channel D
NC	—	8, 9	—	No internal connection (can be left floating)
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	8	10	O	Output, channel C
OUT D	14	16	O	Output, channel D
V–	11	13	—	Negative (lowest) power supply
V+	4	4	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage	Supply voltage		5.5	V
	Signal input terminals[2]	–0.5	0.5	
Current	Signal input terminals[2]		10	mA
	Output short circuit[3]	Continuous		
Temperature	Operating, T_A	–55	125	°C
	Junction, T_J		150	
	Storage, T_{stg}	–55	125	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±600	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage	2.7	5.5	V
Specified temperature	–40	125	°C

6.4 Thermal Information – OPA340

THERMAL METRIC[1]		OPA340				UNIT
		DBV (SOT-23)	P (PDIP)	D (SOIC)	D (SOIC)	
		5 PINS	8 PINS	8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	207.9	53.1	142	83.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.2	42.5	90.2	70.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.0	30.3	82.5	59.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	19.7	39.4	11.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.2	30.2	82	37.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information – OPA2340

THERMAL METRIC[1]		OPA2340		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.4	169.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.5	62.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.6	89.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.9	7.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	78.1	88.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information – OPA4340

THERMAL METRIC[1]		OPA4340	UNIT
		DBQ (SSOP)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics

At T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage		V_S = 5 V		±150	±500	µV
dV_{OS}/dt	Input offset voltage vs temperature		T_A = –40°C to 85°C, V_S = 5 V		±2.5		µV/°C
PSRR	Input offset voltage vs power supply		V_S = 2.7 V to 5.5 V, V_{CM} = 0 V		30	120	µV/V
		Over temperature	V_S = 2.7 V to 5.5 V, V_{CM} = 0 V, T_A = –40°C to 85°C, V_S = 5 V			120	µV/°C
	Channel separation, DC				0.2		µV/V
INPUT BIAS CURRENT							
I_S	Input bias current				±0.2	±10	pA
		Over temperature	T_A = –40°C to 85°C, V_S = 5 V			±60	
I_{OS}	Input offset current				±0.2	±10	pA
NOISE							
	Input voltage noise		f = 0.1 kHz to 50 kHz		8		μV_{RMS}
e_n	Input voltage noise density		f = 1 kHz		25		nV/√Hz
i_n	Current noise density		f = 1 kHz		3		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			–0.3		(V+) + 0.3	V
CMRR	Common-mode rejection ratio		–0.3 V < V_{CM} < (V+) – 1.8 V	80	92		dB
			V_S = 5 V, –0.3 V < V_{CM} < 5.3 V	70	84		
			V_S = 2.7 V, –0.3 V < V_{CM} < 3 V	66	80		

(1) V_S = 5 V.

Electrical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, and V_{OUT} = $V_S/2$, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
INPUT IMPEDANCE							
	Differential				10^{13} || 3		Ω || pF
	Common-mode				10^{13} || 6		Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain		R_L = 100 kΩ, 5 mV < V_O < (V+) – 5 mV	106	124		dB
			R_L = 10 kΩ, 5 mV < V_O < (V+) – 50 mV	100	120		
			R_L = 2 kΩ, 200 mV < V_O < (V+) – 200 mV	94	114		
		Over temperature	R_L = 100 kΩ, 5 mV < V_O < (V+) – 5 mV, T_A = –40°C to 85°C, V_S = 5 V	106			
			R_L = 10 kΩ, 5 mV < V_O < (V+) – 50 mV, T_A = –40°C to 85°C, V_S = 5 V	100			
			R_L = 2 kΩ, 200 mV < V_O < (V+) – 200 mV, T_A = –40°C to 85°C, V_S = 5 V	94			
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product		G = 1		5.5		MHz
SR	Slew rate		V_S = 5 V, G = 1, C_L = 100 pF		6		V/µs
	Settling time, 0.1%		V_S = 5 V, 2-V step, C_L = 100 pF		1		µs
	Settling time, 0.01%		V_S = 5 V, 2-V step, C_L = 100 pF		1.6		µs
	Overload recovery time		V_{IN} × G = V_S		0.2		µs
THD+N	Total harmonic distortion + noise		V_S = 5 V, V_O = $3V_{PP}$ (2), G = 1, f = 1 kHz		0.0007%		
OUTPUT							
	Voltage output swing from rail (2)		R_L = 100 kΩ, A_{OL} ≥ 106 dB		1	5	mV
			R_L = 10 kΩ, A_{OL} ≥ 106 dB		10		
			R_L = 2 kΩ, A_{OL} ≥ 106 dB		40		
		Over temperature	R_L = 100 kΩ, A_{OL} ≥ 106 dB, T_A = –40°C to 85°C, V_S = 5 V			5	
			R_L = 10 kΩ, A_{OL} ≥ 106 dB, T_A = –40°C to 85°C, V_S = 5 V			50	
			R_L = 2 kΩ, A_{OL} ≥ 106 dB, T_A = –40°C to 85°C, V_S = 5 V			200	
I_{SC}	Short-circuit current				±50		mA
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		
POWER SUPPLY							
V_S	Specified voltage range			2.7		5	V
	Operating voltage range		Lower end		2.5		V
			Higher end		5.5		
I_Q	Quiescent current (per amplifier)		I_O = 0, V_S = 5 V		750	950	µA
		Over temperature	I_O = 0, V_S = 5 V, T_A = –40°C to 85°C			100	
TEMPERATURE RANGE							
	Specified range			–40		85	°C
	Operating range			–55		125	°C
	Storage range			–55		125	°C

(2) Output voltage swings are measured between the output and power-supply rails.

6.8 Typical Characteristics

At T_A = 25°C, V_S = 5 V, and R_L = 10 kΩ connected to V_S/2, unless otherwise noted.

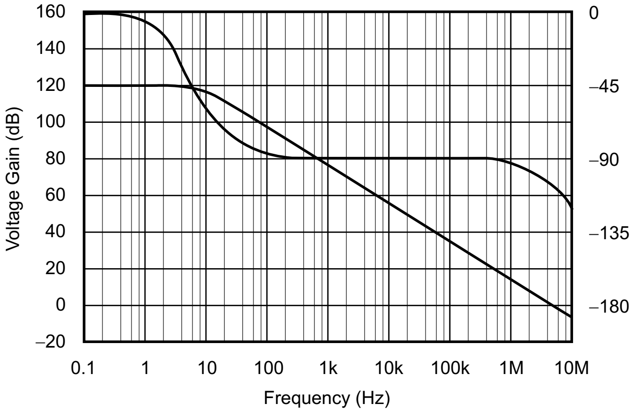


Figure 1. Open-Loop Gain/Phase vs Frequency

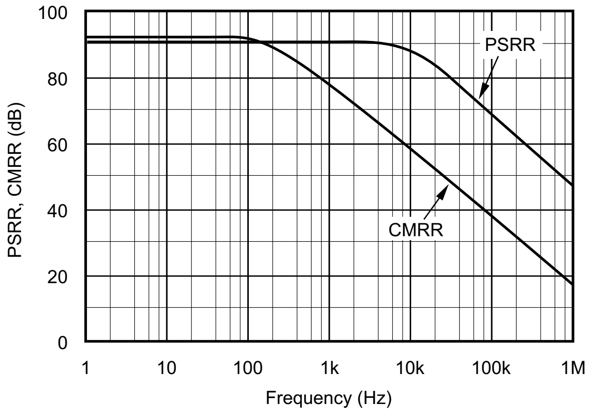


Figure 2. Power-Supply and Common-Mode Rejection vs Frequency

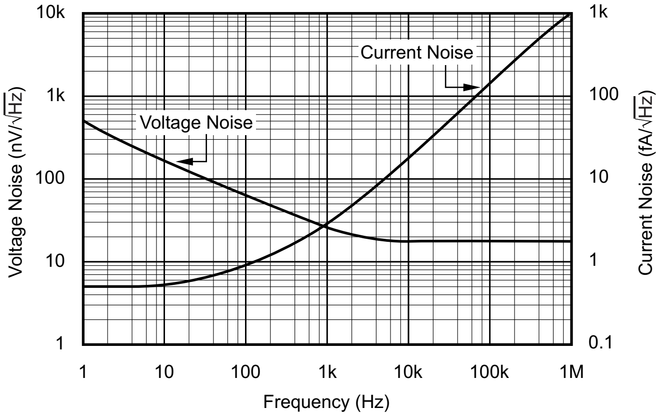


Figure 3. Input Voltage and Current Noise Spectral Density vs Frequency

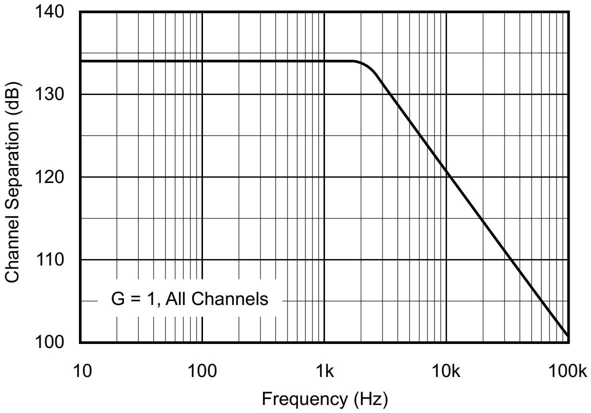


Figure 4. Channel Separation vs Frequency

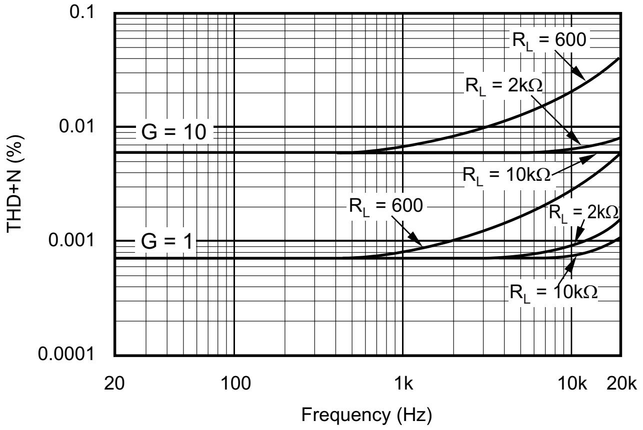


Figure 5. Total Harmonic Distortion + Noise vs Frequency

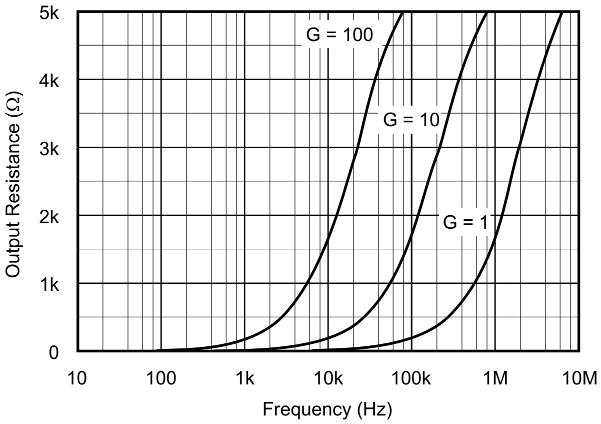


Figure 6. Closed-Loop Output Impedance vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, and R_L = 10 kΩ connected to $V_S/2$, unless otherwise noted.

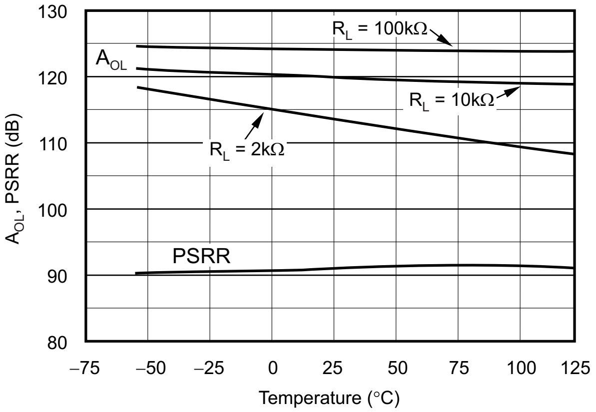


Figure 7. Open-Loop Gain and Power-Supply Rejection vs Temperature

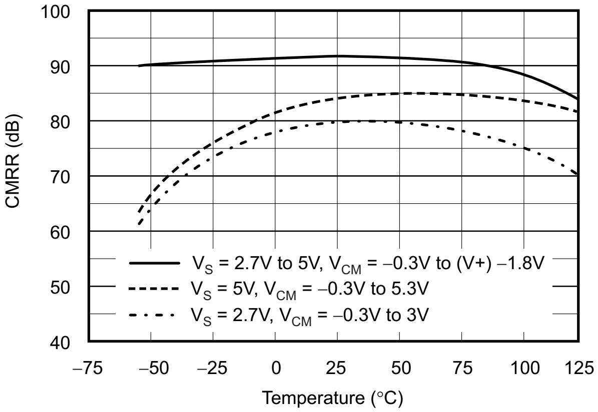


Figure 8. Common-Mode Rejection vs Temperature

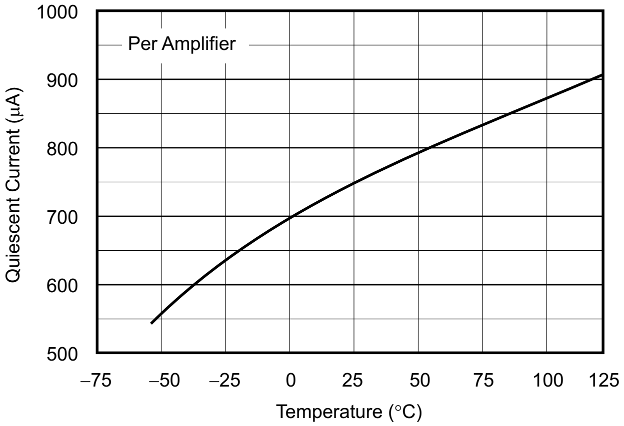


Figure 9. Quiescent Current vs Temperature

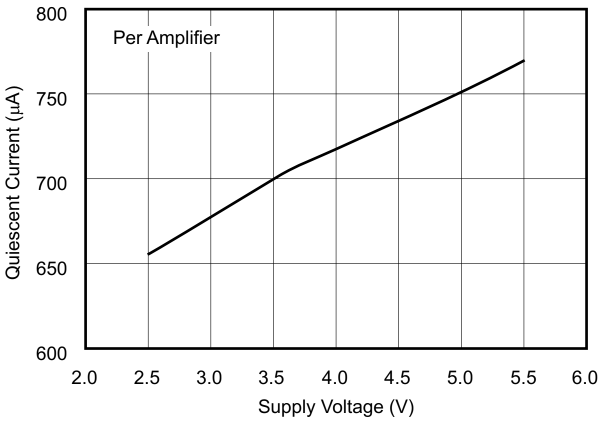


Figure 10. Quiescent Current vs Supply Voltage

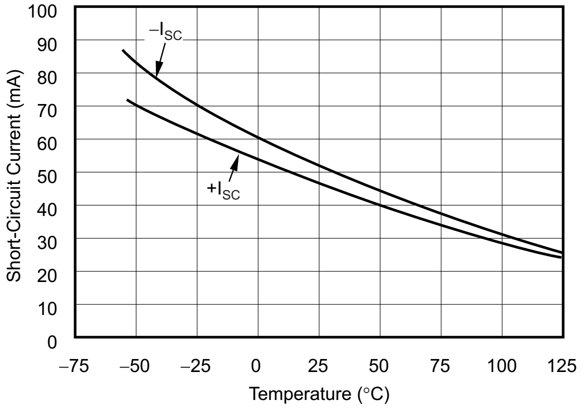


Figure 11. Short-Circuit Current vs Temperature

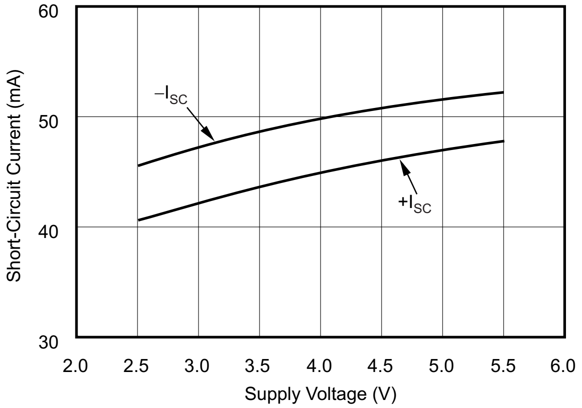


Figure 12. Short-Circuit Current vs Supply Voltage

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, and R_L = 10 kΩ connected to $V_S/2$, unless otherwise noted.

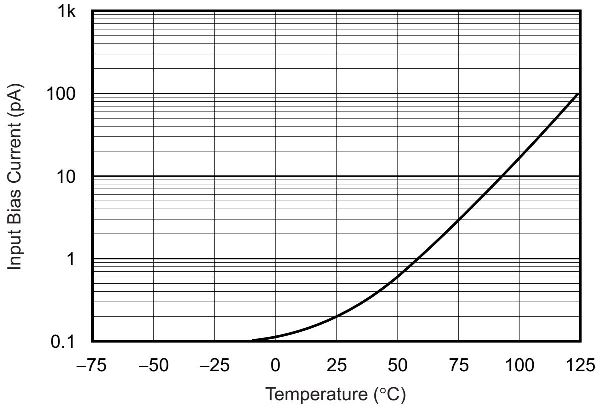


Figure 13. Input Bias Current vs Temperature

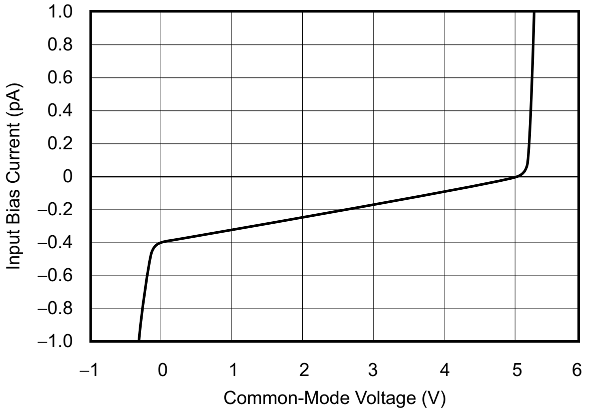


Figure 14. Input Bias Current vs Input Common-Mode Voltage

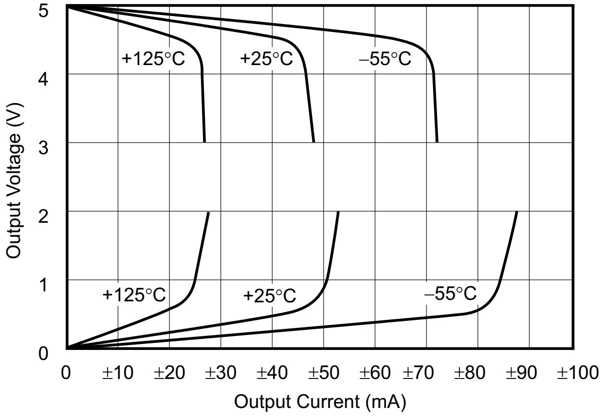


Figure 15. Output Voltage Swing vs Output Current

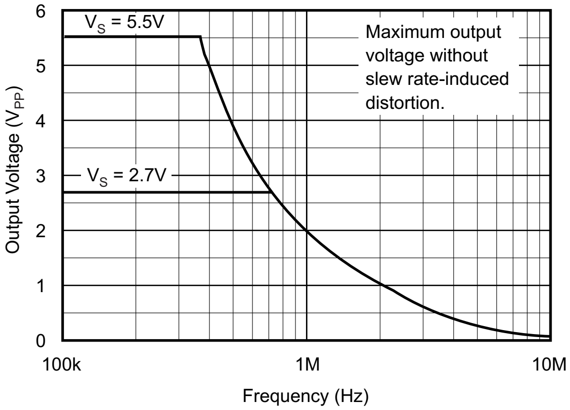


Figure 16. Maximum Output Voltage vs Frequency

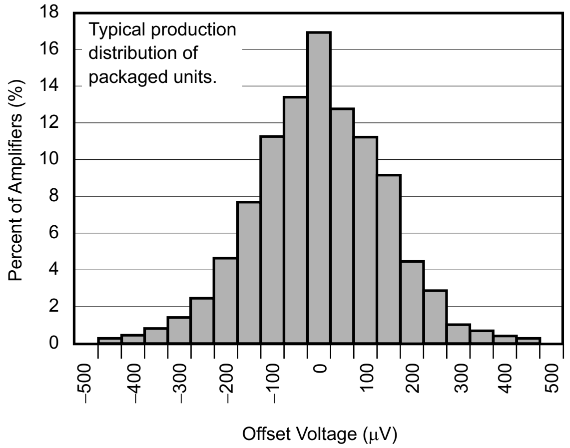


Figure 17. Offset Voltage Production Distribution

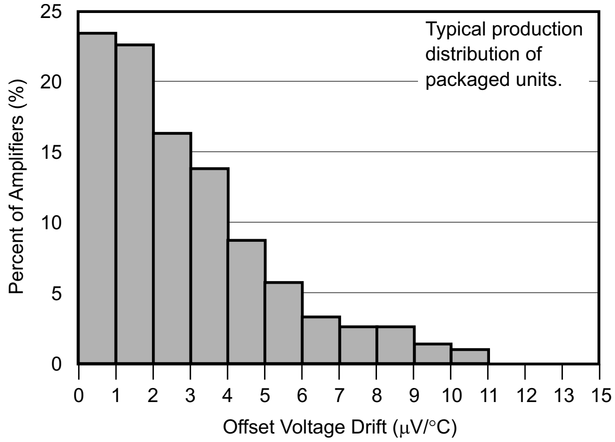
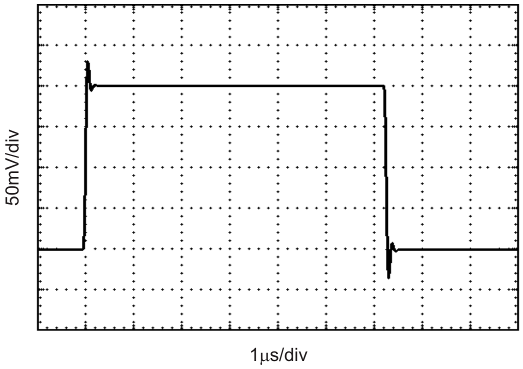


Figure 18. Offset Voltage Drift Magnitude Production Distribution

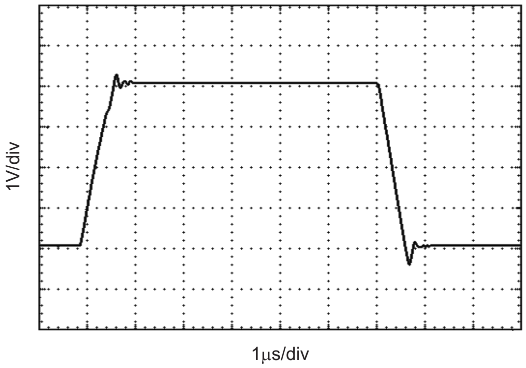
Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, and R_L = 10 kΩ connected to $V_S/2$, unless otherwise noted.



C_L = 100 pF

Figure 19. Small-Signal Step Response



C_L = 100 pF

Figure 20. Large-Signal Step Response

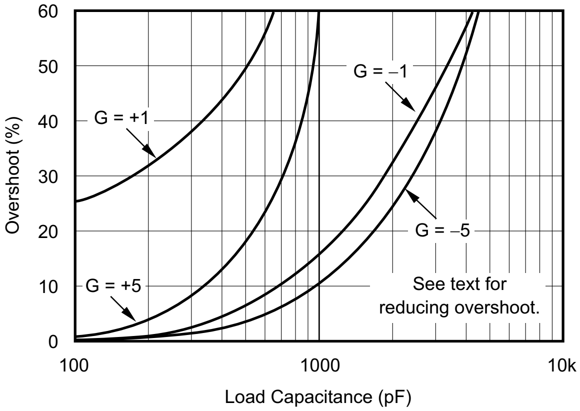


Figure 21. Small-Signal Overshoot vs Load Capacitance

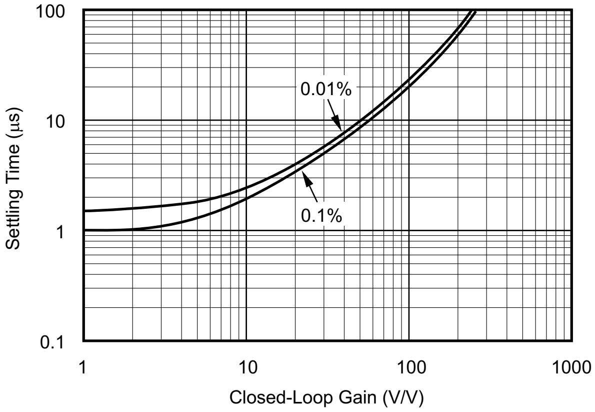


Figure 22. Settling Time vs Closed-Loop Gain

7 Detailed Description

7.1 Overview

The OPA340 series operational amplifiers are fabricated on a state-of-the-art, 0.6-micron CMOS process. These devices are unity-gain stable and suitable for a wide range of general-purpose applications. Rail-to-rail input and output make them ideal for driving sampling A/D converters. In addition, excellent AC performance makes them well-suited for audio applications. The class AB output stage is capable of driving 600-Ω loads series and extends 500 mV beyond the supply. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. Figure 23 shows the input and output waveforms for the OPA340 in unity-gain configuration. Operation is from a single 5-V supply with a 10-kΩ load connected to V/2. The input is a 5-V_{PP} sinusoid. Output voltage is approximately 4.98 V_{PP}. Power-supply pins must be bypassed with 0.01-µF ceramic capacitors.

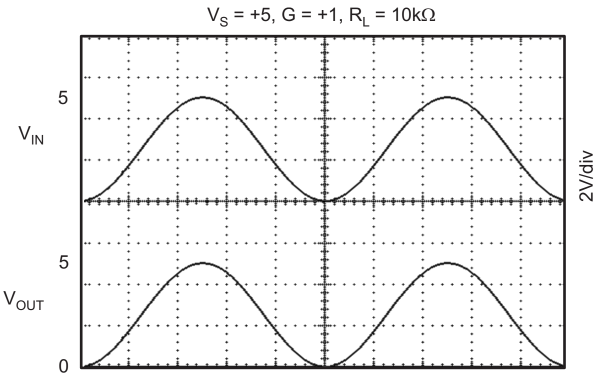
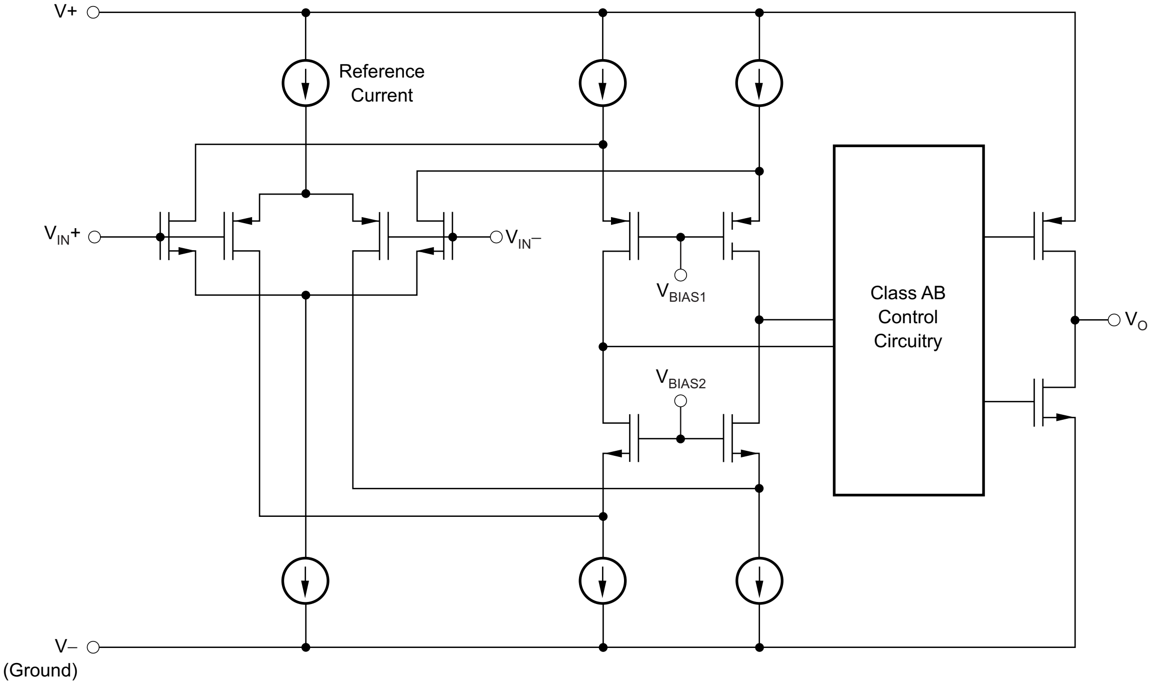


Figure 23. Rail-to-Rail Input and Output

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

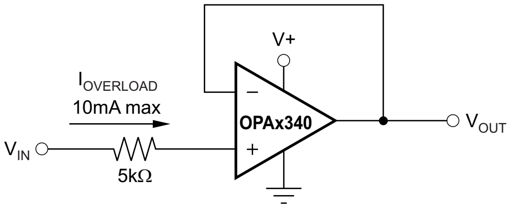
The OPA340 series operational amplifiers are fully specified from 2.7 V to 5 V. However, supply voltage may range from 2.5 V to 5.5 V. Parameters are ensured over the specified supply range—a unique feature of the OPA340 series. In addition, many specifications apply from –40°C to 85°C. Most behavior remains virtually unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltages or temperature are shown in the *Typical Characteristics*.

7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the OPA340 series extends 500 mV beyond the supply rails. This extended range is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.3 V to 500 mV above the positive supply, while the P-channel pair is on for inputs from 500 mV below the negative supply to approximately (V+) – 1.3 V. There is a small transition region, typically (V+) – 1.5 V to (V+) – 1.1 V, in which both pairs are on. This 400-mV transition region can vary ±300 mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1.8 V to (V+) – 1.4 V on the low end, up to (V+) – 1.2 V to (V+) – 0.8 V on the high end.

OPA340 series operational amplifiers are laser-trimmed to the reduce offset voltage difference between the N-channel and P-channel input stages, resulting in improved common-mode rejection and a smooth transition between the N-channel pair and the P-channel pair. However, within the 400-mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region.

A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class AB output stage. Normally, input bias current is approximately 200 fA; however, input voltages exceeding the power supplies by more than 500 mV can cause excessive current to flow in or out of the input pins. Momentary voltages greater than 500 mV beyond the power supply can be tolerated if the current on the input pins is limited to 10 mA. This current limiting is easily accomplished with an input resistor, as shown in Figure 24. Many input signals are inherently current-limited to less than 10 mA; therefore, a limiting resistor is not required.



Copyright © 2016, Texas Instruments Incorporated

Figure 24. Input Current Protection for Voltages Exceeding the Supply Voltage

7.3.3 Rail-to-Rail Output

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For light resistive loads (> 50 kΩ), the output voltage is typically a few millivolts from the supply rails. With moderate resistive loads (2 kΩ to 50 kΩ), the output can swing to within a few tens of millivolts from the supply rails and maintain high open-loop gain (see Figure 15).

7.3.4 Capacitive Load and Stability

OPA340 series operational amplifiers can drive a wide range of capacitive loads. However, all operational amplifiers under certain conditions can become unstable. operational amplifier configuration, gain, and load value are some of the factors to consider when determining stability. An operational amplifier in unity-gain configuration is most susceptible to the effects of capacitive load. The capacitive load reacts with the output resistance of the operational amplifier, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin. In unity-gain configuration, the OPA340 series operational amplifiers perform well, with a pure capacitive load up to approximately 1000 pF. Increasing gain enhances the amplifier ability to drive more capacitance (see Figure 21).

Feature Description (continued)

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10-Ω to 20-Ω resistor in series with the output, as shown in Figure 25. This resistor significantly reduces ringing with large capacitive loads. However, if there is a resistive load in parallel with the capacitive load, it creates a voltage divider introducing a DC error at the output and slightly reduces output swing. This error can be insignificant. For instance, with R_L = 10 kΩ and R_S = 20 Ω, there is only an approximate 0.2% error at the output.

When used with the miniature package options of the OPA340 series, the combination is ideal for space-limited and low-power applications. For further information, consult the ADS7816 data sheet, *12-Bit High Speed Micro Power Sampling Analog-To-Digital Converter* (SBAS061). With the OPA340 in a noninverting configuration, an RC network at the output of the amplifier can be used to filter high-frequency noise in the signal (see Figure 26). In the inverting configuration, filtering may be accomplished with a capacitor across the feedback resistor (see Figure 27).

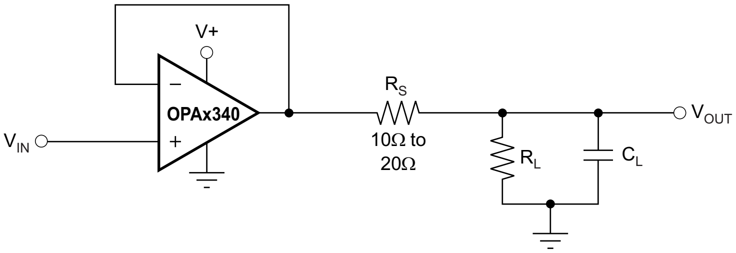


Figure 25. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive

7.3.5 Driving A/D Converters

The OPA340 series operational amplifiers are optimized for driving medium-speed (up to 100 kHz) sampling A/D converters. However, they also offer excellent performance for higher speed converters. The OPA340 series provides an effective means of buffering the converter input capacitance and resulting charge injection while providing signal gain. Figure 26 and Figure 27 show the OPA340 driving an ADS7816. The ADS7816 is a 12-bit, micro-power sampling converter in the tiny 8-pin VSSOP package.

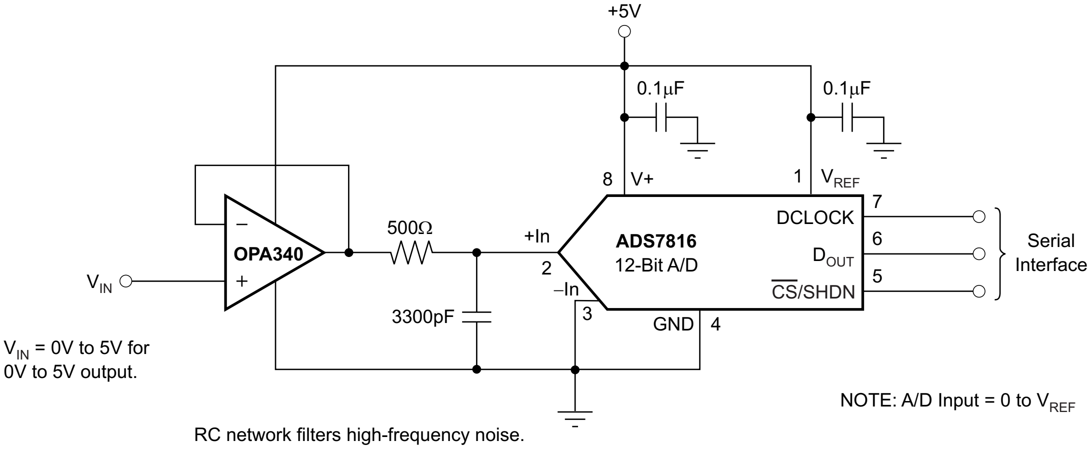
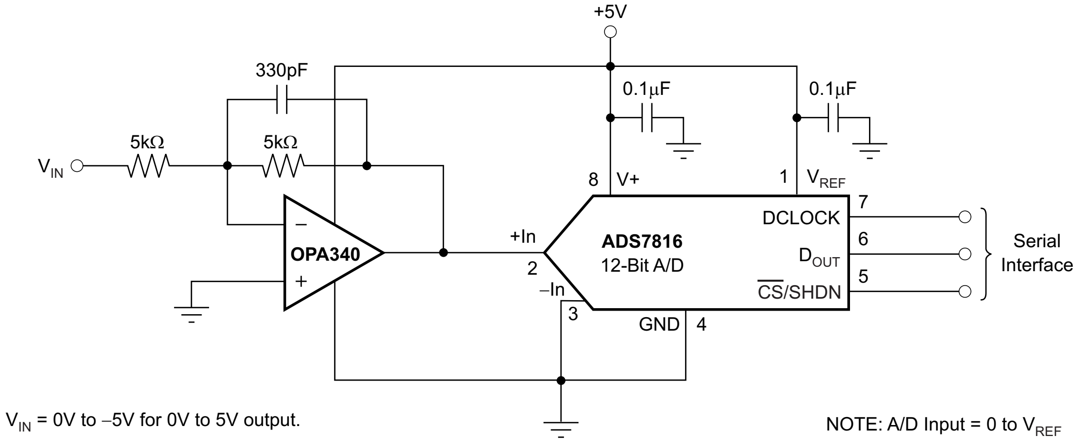


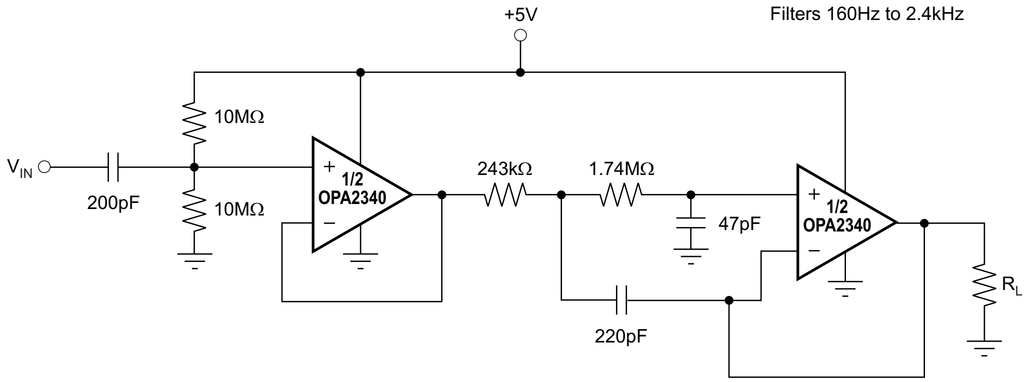
Figure 26. OPA340 in Noninverting Configuration Driving ADS7816

Feature Description (continued)



Copyright © 2016, Texas Instruments Incorporated

Figure 27. OPA340 in Inverting Configuration Driving ADS7816



Copyright © 2016, Texas Instruments Incorporated

Figure 28. Speech Bandpass Filter

7.4 Device Functional Modes

The OPAx340 has a single functional mode and is operational when the power-supply voltage is greater than 2.7 V (±1.35 V). The maximum power supply voltage for the OPAx340 is 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

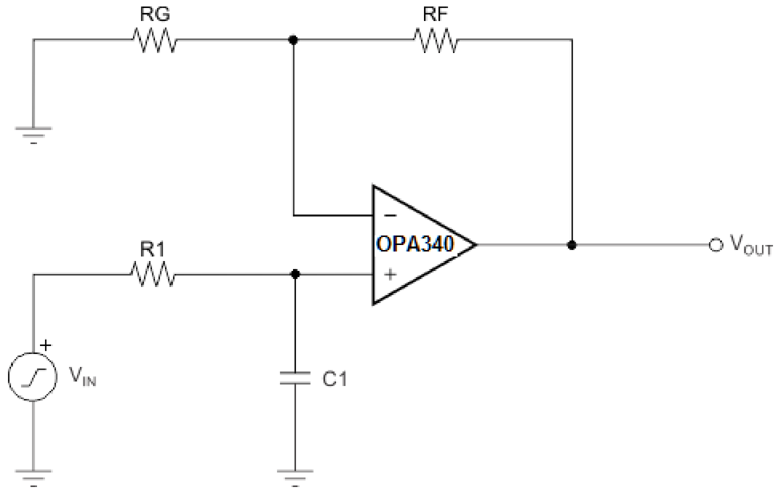
8.1 Application Information

The OPAx340 amplifier is a single-supply, CMOS operational amplifier with 5.5-MHz unity-gain bandwidth and supply current of 950 µA. Its performance is optimized for low-voltage (2.7 V to 5.5 V), single-supply applications, with its input common-mode voltage linear range extending 300 mV beyond the rails and the output voltage swing within 5 mV of either rail. The OPAx340 series features wide bandwidth and unity-gain stability with rail-to-rail input and output for increased dynamic range. Power-supply pins must be bypassed with 0.01-µF ceramic capacitors.

8.2 Typical Applications

8.2.1 Single-Pole, Low-Pass Filter

Figure 29 shows the OPA340 in a typical noninverting application with the input signal bandwidth limited by the input lowpass filter.



Copyright © 2016, Texas Instruments Incorporated

Figure 29. Single-Pole, Low-Pass Filter

Equation 1 through Equation 2 show calculations for corner frequency and gain:

$$f_{-3\,dB} = \frac{1}{2\pi R_1 C_1} \tag{1}$$

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right) \tag{2}$$

Typical Applications (continued)

8.2.1.1 Design Requirements

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting terminal of the amplifier, as shown in Figure 29. If a steeper attenuation level is required, a two-pole or higher-order filter may be used.

8.2.1.2 Detailed Design Procedure

The design goals for this circuit include these parameters:

- A noninverting gain of 10 V/V (20 dB)
- Design a single-pole response circuit with –3-dB rolloff at 15.9 kHz and 159 Hz
- Modify the design to increase attenuation level to –40 dB/decade (Sallen-Key Filter)

Use these design values:

- C_1 = 0 nF, 10 nF, 1 µF
- R_1 = 1 kΩ
- R_G = 10 kΩ
- R_F = 90 kΩ

Figure 30 shows how the output voltage of OPA340 changes over frequency depending on the value of C_1 with a constant R_1 of 1 kΩ. Without any filtering of the input signal (C_1 = 0), the –3-dB effective bandwidth is a function of the OPA340 unity-gain bandwidth and closed-loop gain, $f_{(-3dB)}$ = UGBW/A_{CL}, where A_{CL} is closed-loop gain and UGBW denotes unity-gain bandwidth. Thus, for a closed-loop gain = 10, $f_{(-3dB)}$ = 1 MHz/10 =100 kHz; see Figure 30.

To further limit the output bandwidth, an appropriate choice of C_1 must be made: for C_1 = 10 nF, $f_C = \frac{1}{2\pi \times R_1C_1} = \frac{1}{2\pi \times 1^{3} \times 1^{-8}}$ = 15.9 kHz.

To further limit the bandwidth, a larger C_1 must be used: choosing C_1 = 1 µF,

$f_C = \frac{1}{2\pi \times R_1C_1} = \frac{1}{2\pi \times 1^{3} \times 1^{-6}}$ = 159 Hz (see Figure 30).

8.2.1.3 Application Curve

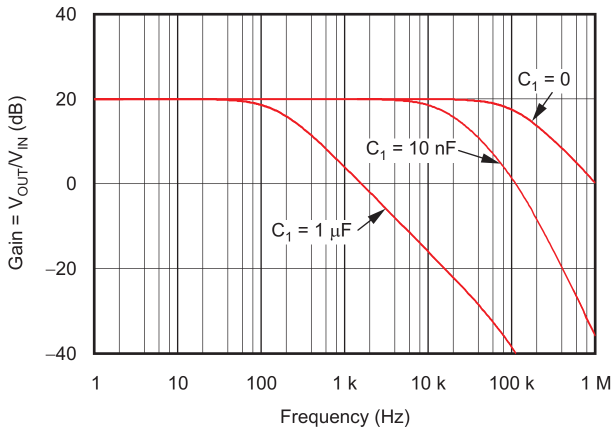
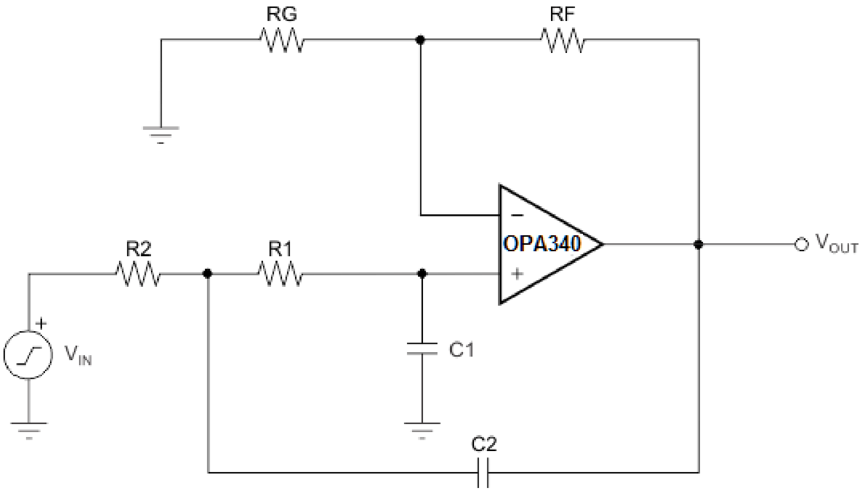


Figure 30. OPA340 Single-Pole AC Gain vs Frequency Response

Typical Applications (continued)

8.2.2 Two-Pole, Low-Pass Filter

If even more attenuation is required, a multiple pole filter is required. The Sallen-Key filter may be used for this task, as shown in Figure 31. For best results, the amplifier must have effective bandwidth that is at least 10 times higher than the filter cutoff frequency. Failure to follow this guideline results in a phase shift of the amplifier, which in turn leads to lower precision of the filter bandwidth. Additionally, to minimize the loading effect between multiple RC pairs on overall the filter cutoff frequency, choose R = 10 × R_1 and C_2 = C1/10; see Figure 32.



Copyright © 2016, Texas Instruments Incorporated

Figure 31. Two-Pole, Lowpass Filter

Equation 3 through Equation 5 show calculations for corner frequency and gain:

$$f_C = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}} \tag{3}$$

$$\frac{V_{OUT(s)}}{V_{IN(s)}} = \frac{G(2\pi f_c)^2}{s^2 + 2\zeta(2\pi f_c)s + (2\pi f_c)^2} \tag{4}$$

$$G = \frac{R_G + R_F}{R_G} \tag{5}$$

8.2.2.1 Detailed Design Procedure

Use these design values:

- C_1 = 10 nF and C_2 = 1 nF
- R_1 = 1 kΩ and R_2= 10 kΩ
- R_G = 10 kΩ
- R_F = 90 kΩ

Figure 32 shows the Sallen-Key filter second-order response for different RC values: for R and C values above, $f_C = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}} = \frac{1}{2\pi\sqrt{1^3 \times 1^{-8} \times 1^4 \times 1^{-9}}}$ = 15.9 kHz.

To further limit the bandwidth, a larger RC value must be used: increasing C values 100 times, such as C_1 = 1 µF and C_2 = 0.1 µF, with unchanged resistors, results in the second-order rolloff at $f_C = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}} = \frac{1}{2\pi\sqrt{1^3 \times 1^{-6} \times 1^4 \times 1^{-7}}}$ = 159 Hz. See Figure 32.

Typical Applications (continued)

8.2.2.2 Application Curve

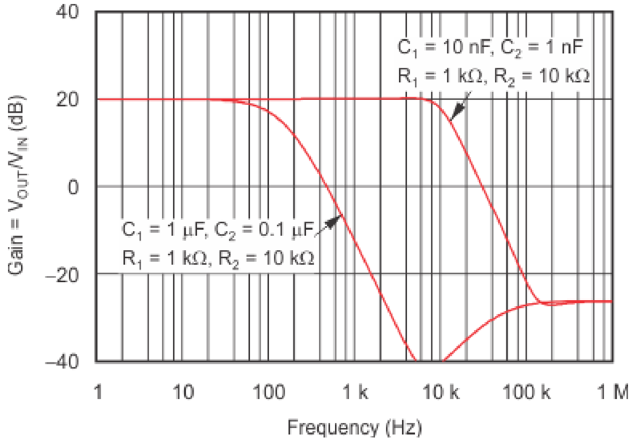


Figure 32. OPA340 Two-Pole, Lowpass Sallen-Key AC Gain vs Frequency Response

9 Power Supply Recommendations

The OPAx340 is specified for operation from 2.7 V to 5.5 V (±1.35 V to ±2.75 V).

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings*).

TI recommends placing 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

10 Layout

10.1 Layout Guidelines

Pay attention to good layout practices. Keep traces short and when possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Operational amplifiers vary in susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or DC signal levels with changes in the interfering RF signal. The OPA340 is specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields can still cause varying offset levels.

10.2 Layout Example

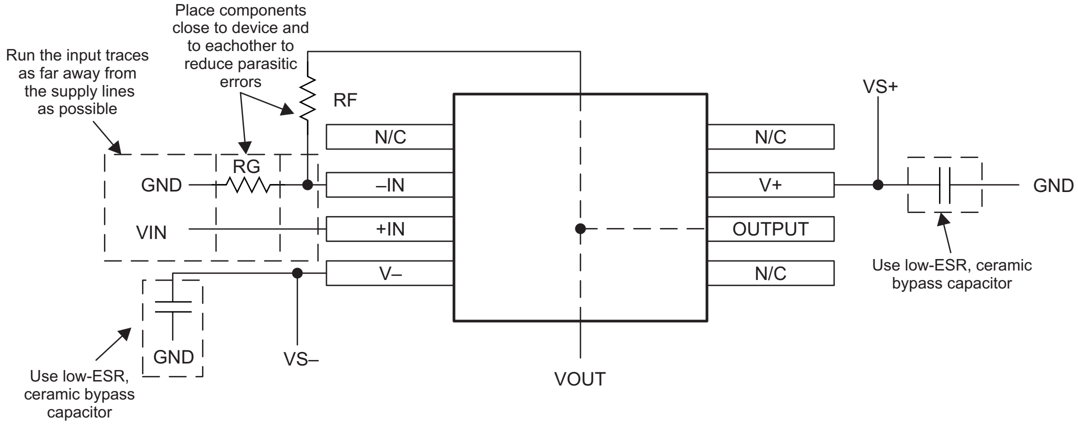


Figure 33. Layout Recommendation

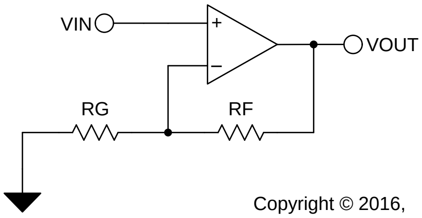


Figure 34. Schematic Representation

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 DIP Adapter EVM

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (MSOP-8), DBV (SOT23-6, SOT23-5 and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

11.1.1.3 Universal Operational Amplifier EVM

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, MSOP, TSSOP and SOT23 packages are all supported.

NOTE

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several operational amplifier device samples when ordering the Universal Op Amp EVM.

11.1.1.4 TI Precision Designs

TI Precision Designs are analog solutions created by TI’s precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

11.1.1.5 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following application reports and publications (available for download from www.ti.com):

- *12-Bit High Speed Micro Power Sampling Analog-To-Digital Converter* (SBAS061)
- *A Dual-Polarity, Bidirectional Current-Shunt Monitor* (SLYT311)
- *OPA340, OPA2340, OPA4340 EMI Immunity Performance* (SBOZ010)
- *Getting the Full Potential from your ADC* (SBAA069)
- *Feedback Plots Define Op Amp AC Performance* (SBOA015)
- *Capacitive Load Drive Solution Using an Isolation Resistor* (TIPD128)
- *Circuit Board Layout Techniques* (SLOA089)

11.3 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA340	Click here	Click here	Click here	Click here	Click here
OPA2340	Click here	Click here	Click here	Click here	Click here
OPA4340	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

MicroAmplifier, TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2340EA/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		A40A	Samples
OPA2340EA/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		A40A	Samples
OPA2340EA/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		A40A	Samples
OPA2340EA/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		A40A	Samples
OPA2340PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2340PA	Samples
OPA2340PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2340PA	Samples
OPA2340UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2340UA	Samples
OPA2340UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 2340UA	Samples
OPA2340UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 2340UA	Samples
OPA2340UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2340UA	Samples
OPA340NA/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A40	Samples
OPA340NA/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A40	Samples
OPA340NA/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A40	Samples
OPA340NA/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A40	Samples
OPA340PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	OPA340PA	Samples
OPA340PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	OPA340PA	Samples
OPA340UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 340UA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA340UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 340UA	Samples
OPA340UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 340UA	Samples
OPA340UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 340UA	Samples
OPA4340EA/250	ACTIVE	SSOP	DBQ	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4340EA	Samples
OPA4340EA/250G4	ACTIVE	SSOP	DBQ	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4340EA	Samples
OPA4340EA/2K5	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4340EA	Samples
OPA4340EA/2K5G4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4340EA	Samples
OPA4340UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4340UA	Samples
OPA4340UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4340UA	Samples
OPA4340UA/2K5G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4340UA	Samples
OPA4340UAG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4340UA	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA340 :

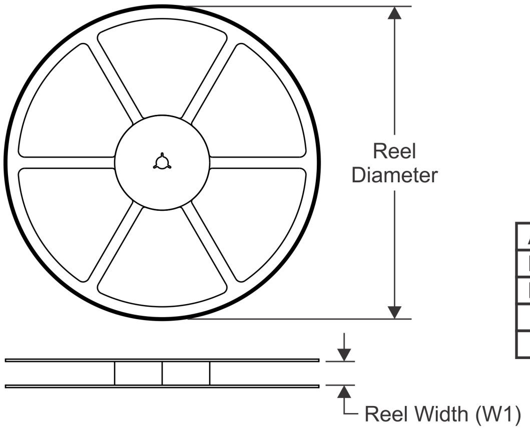
- Enhanced Product: OPA340-EP

NOTE: Qualified Version Definitions:

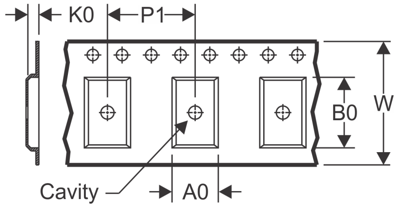
  - Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

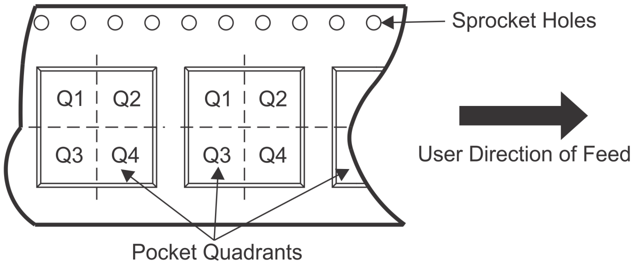


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

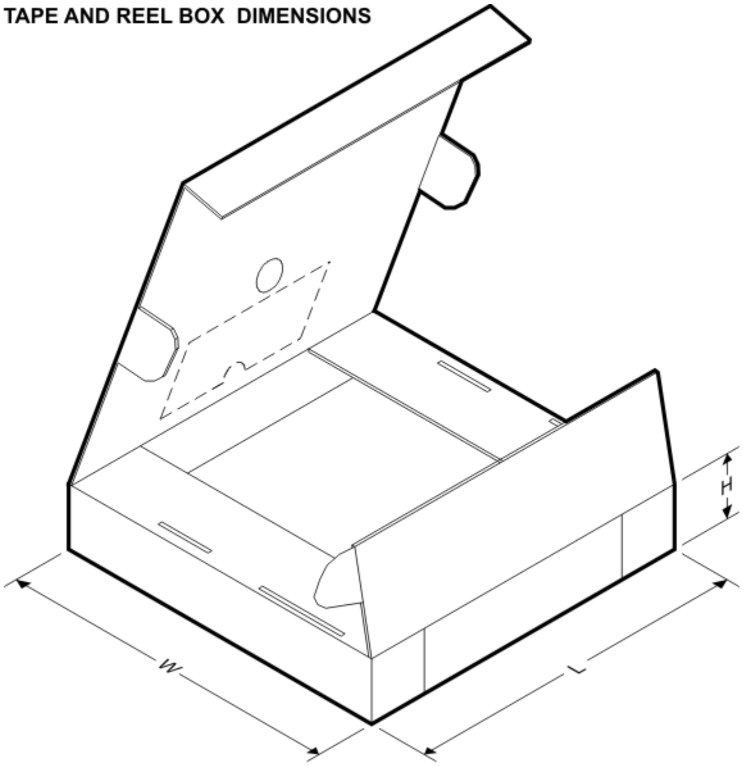
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2340EA/250	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2340EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA340NA/250	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA340NA/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA340NA/3K	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA340NA/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA4340EA/250	SSOP	DBQ	16	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4340EA/2K5	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4340UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

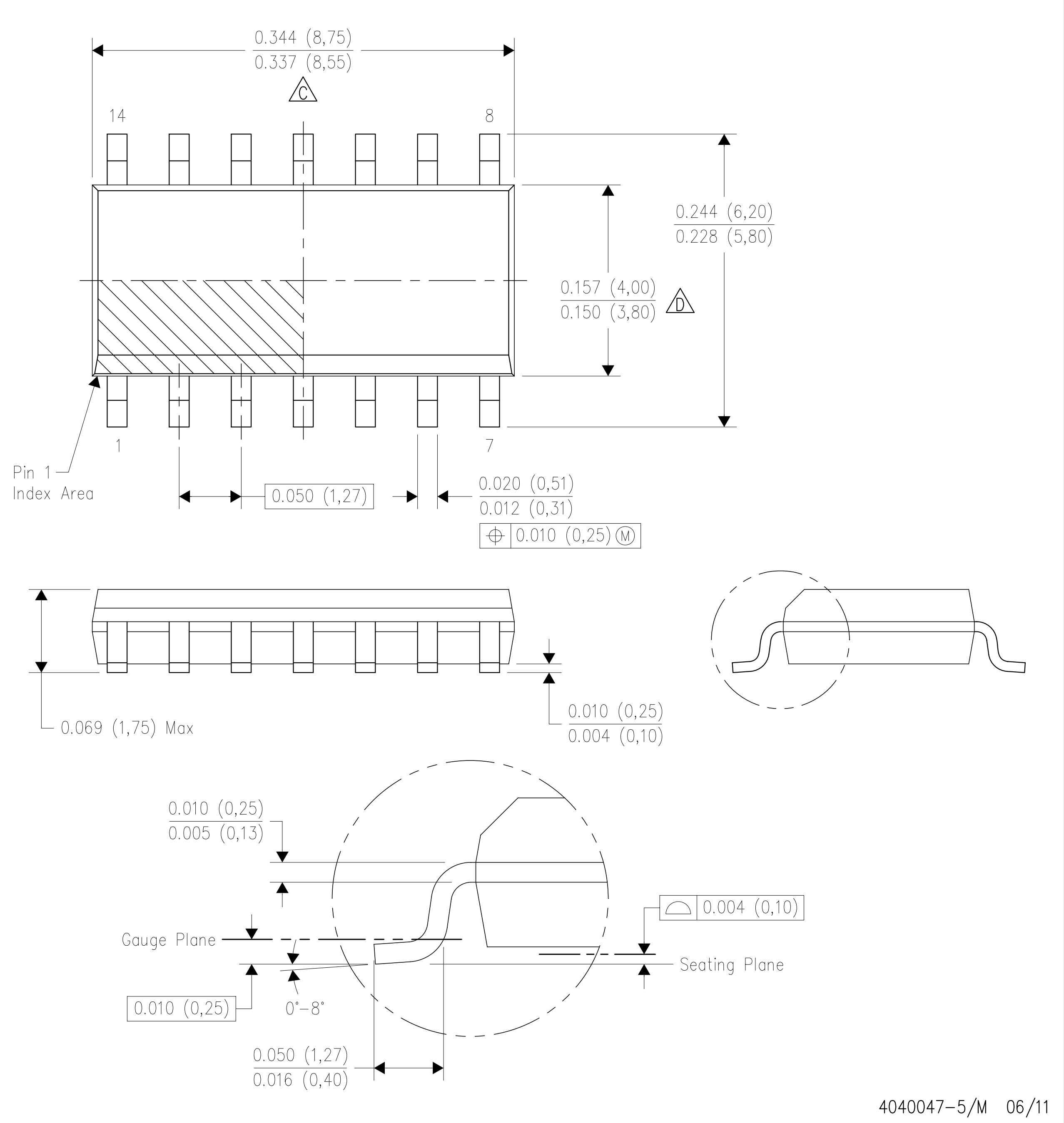
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

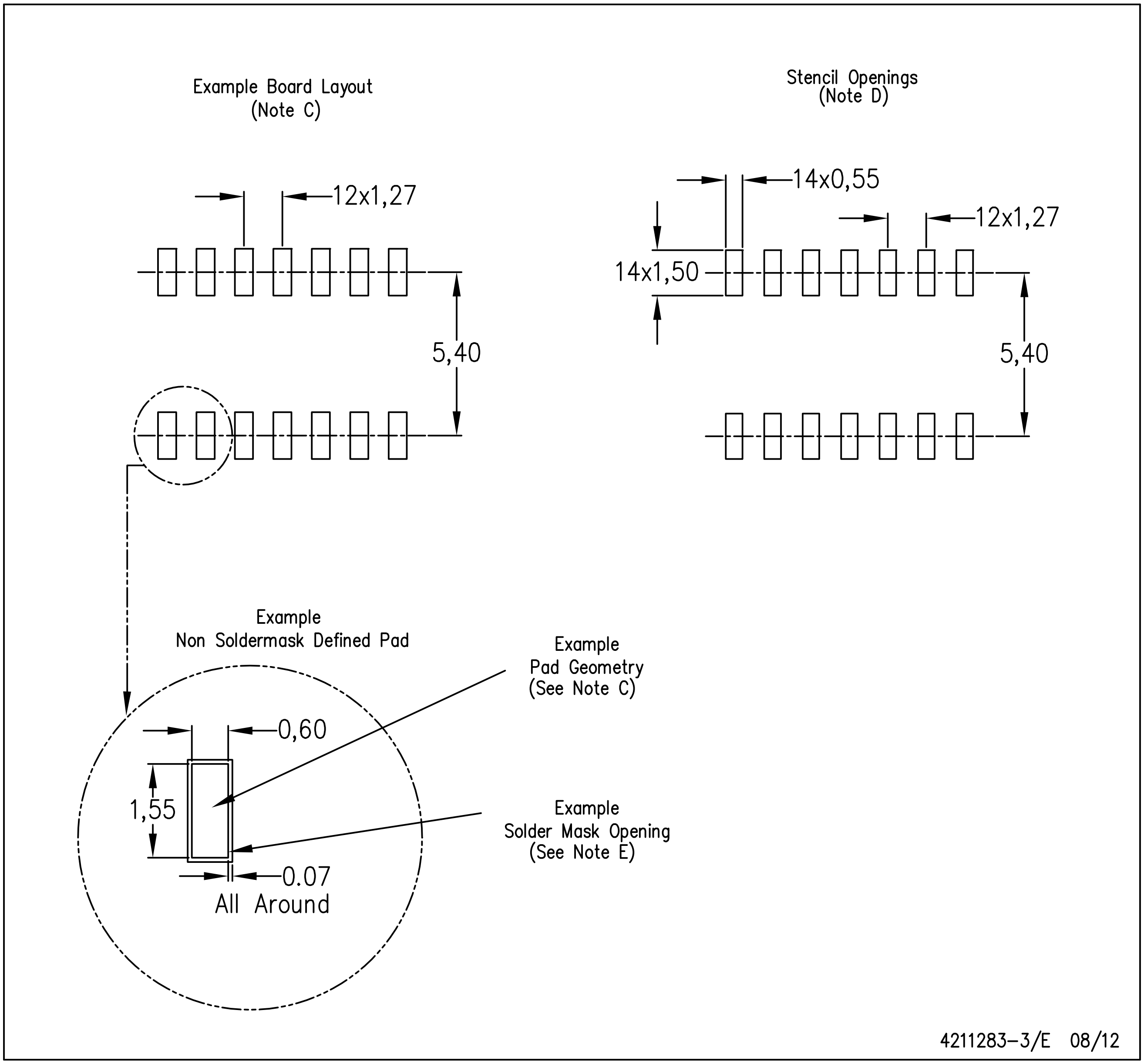
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2340EA/250	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2340EA/2K5	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA340NA/250	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA340NA/250	SOT-23	DBV	5	250	195.0	200.0	45.0
OPA340NA/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA340NA/3K	SOT-23	DBV	5	3000	195.0	200.0	45.0
OPA4340EA/250	SSOP	DBQ	16	250	210.0	185.0	35.0
OPA4340EA/2K5	SSOP	DBQ	16	2500	367.0	367.0	35.0
OPA4340UA/2K5	SOIC	D	14	2500	367.0	367.0	38.0

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



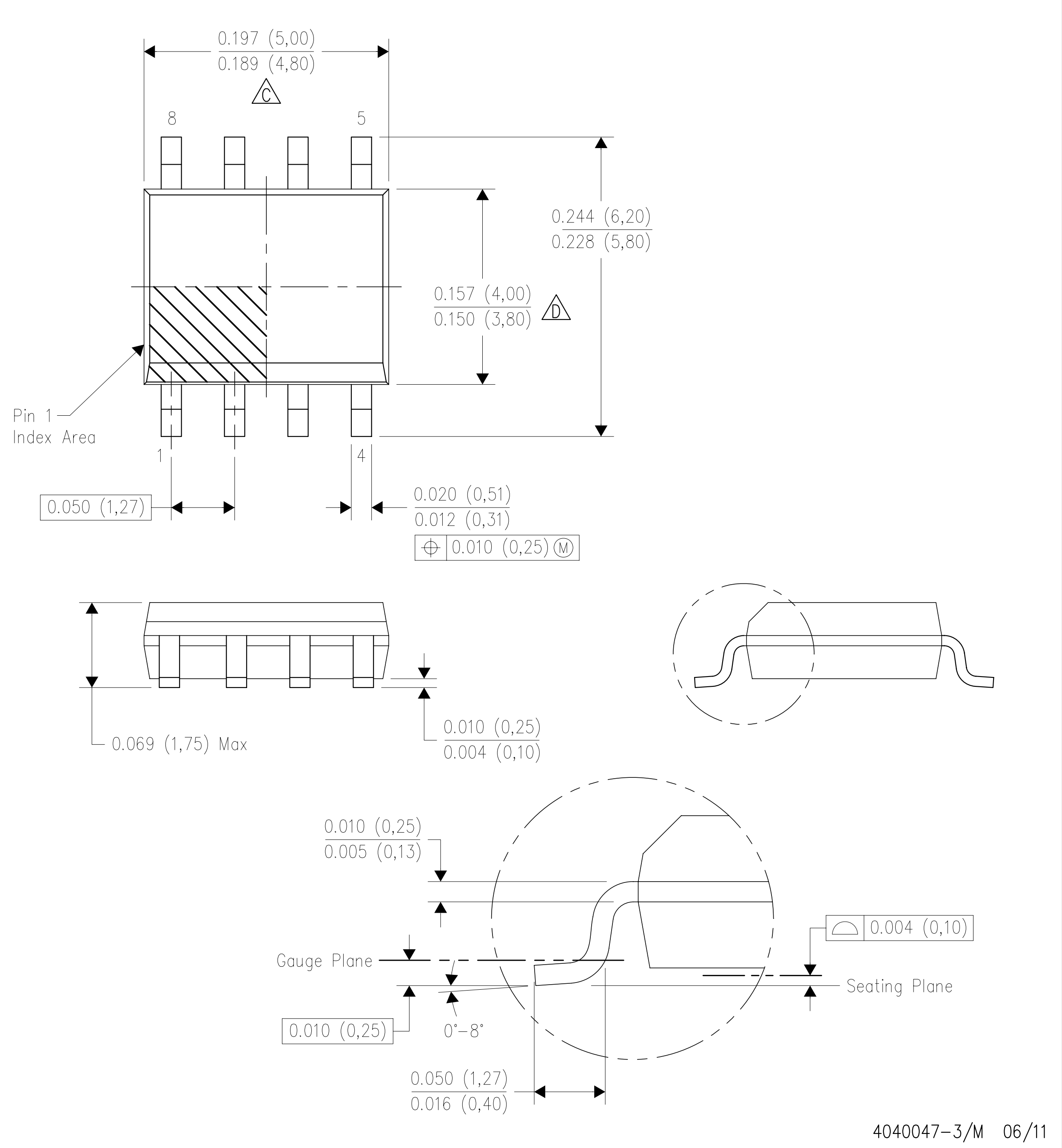
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



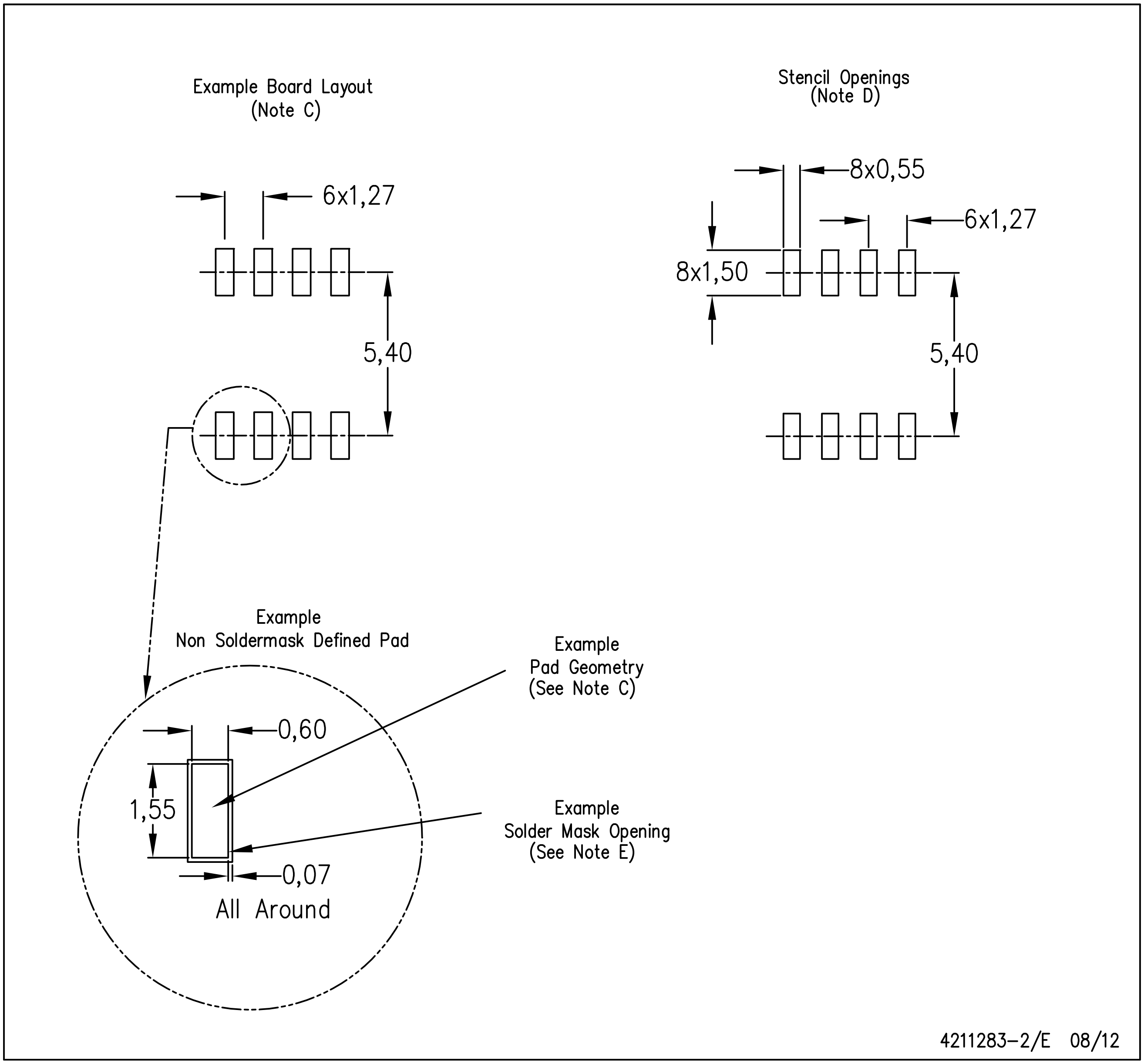
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE

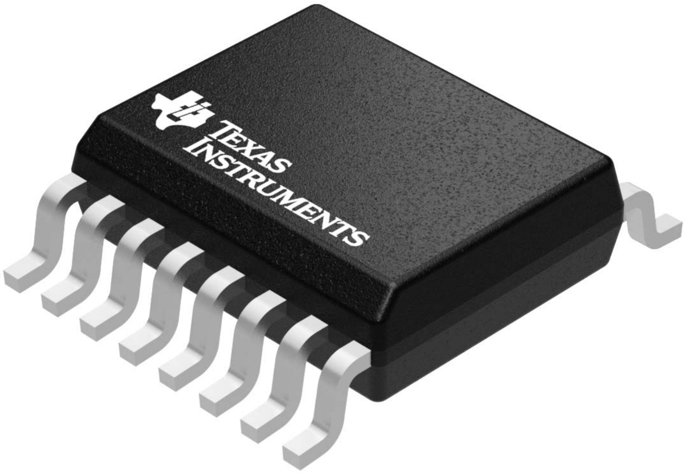


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

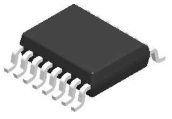
DBQ 16 **SSOP - 1.75 mm max height**

SHRINK SMALL-OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4073301-2/I

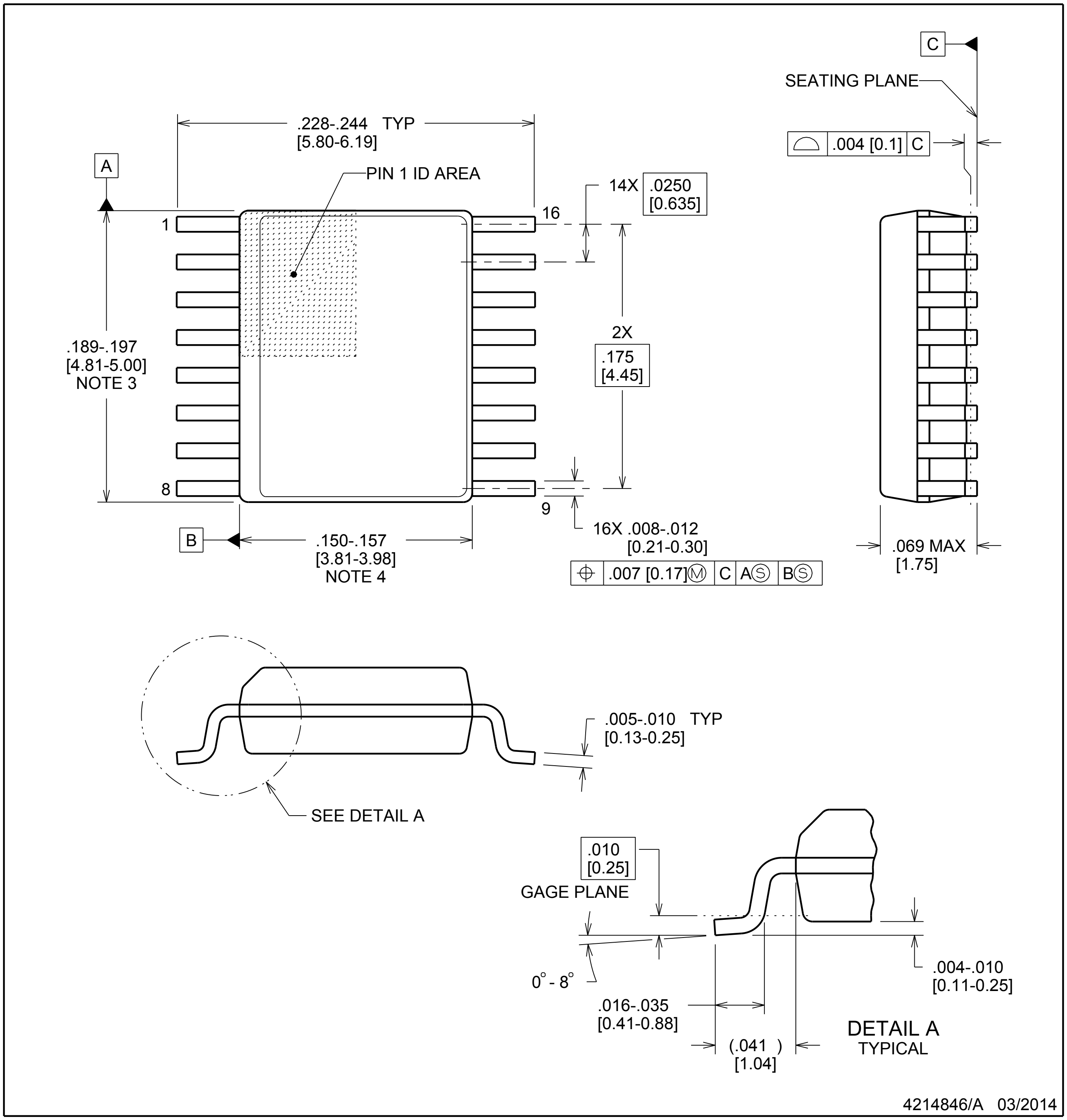


PACKAGE OUTLINE

DBQ0016A

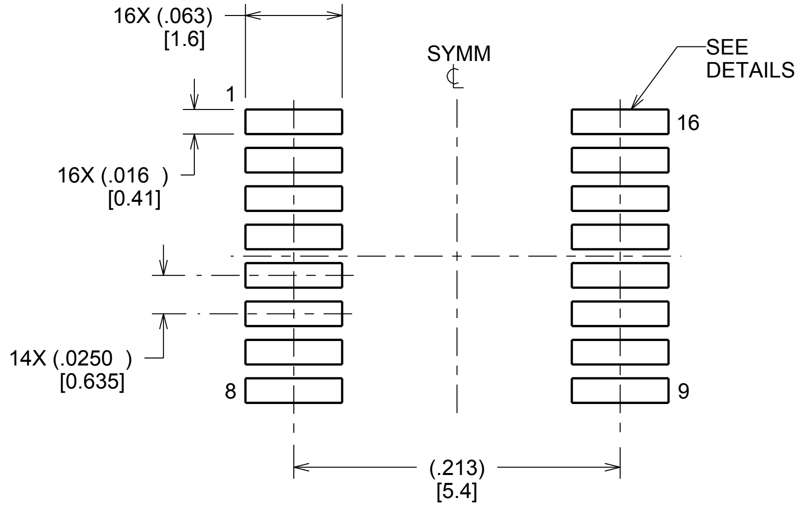
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

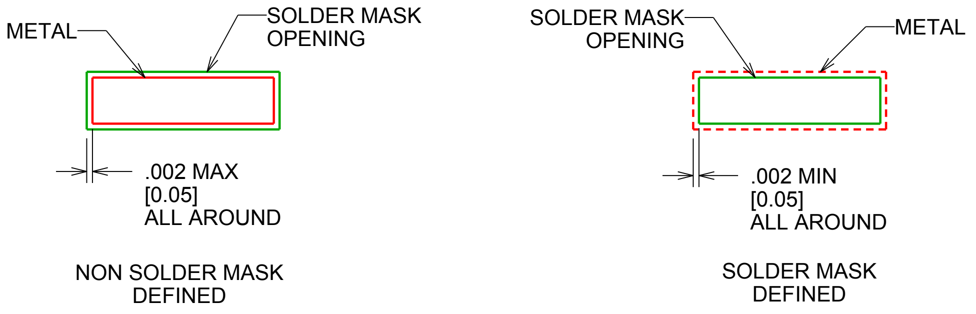


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

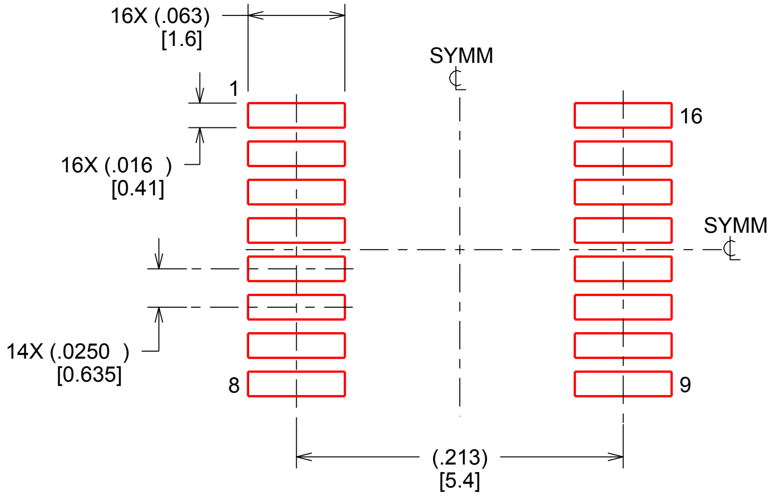


SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

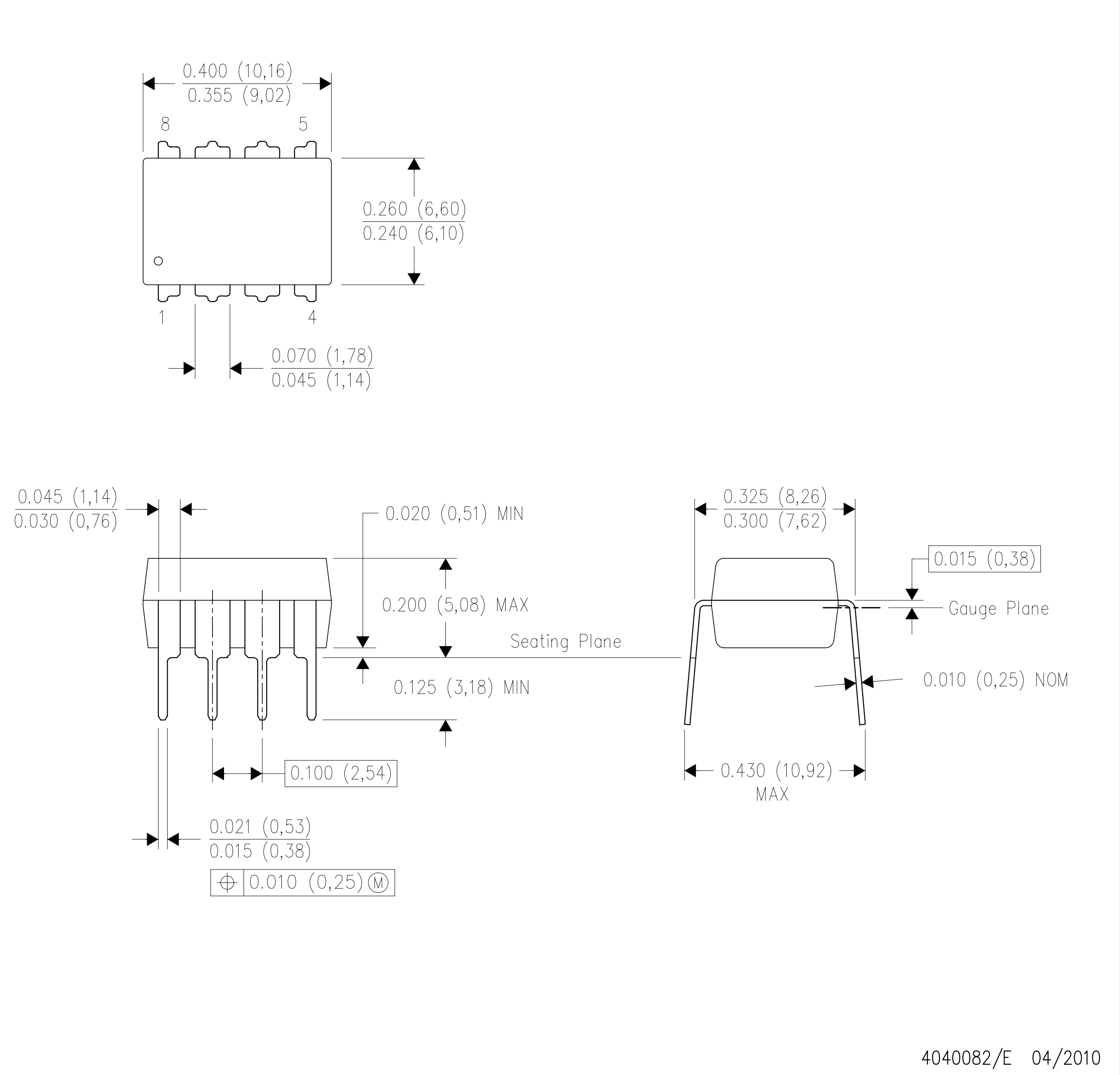


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

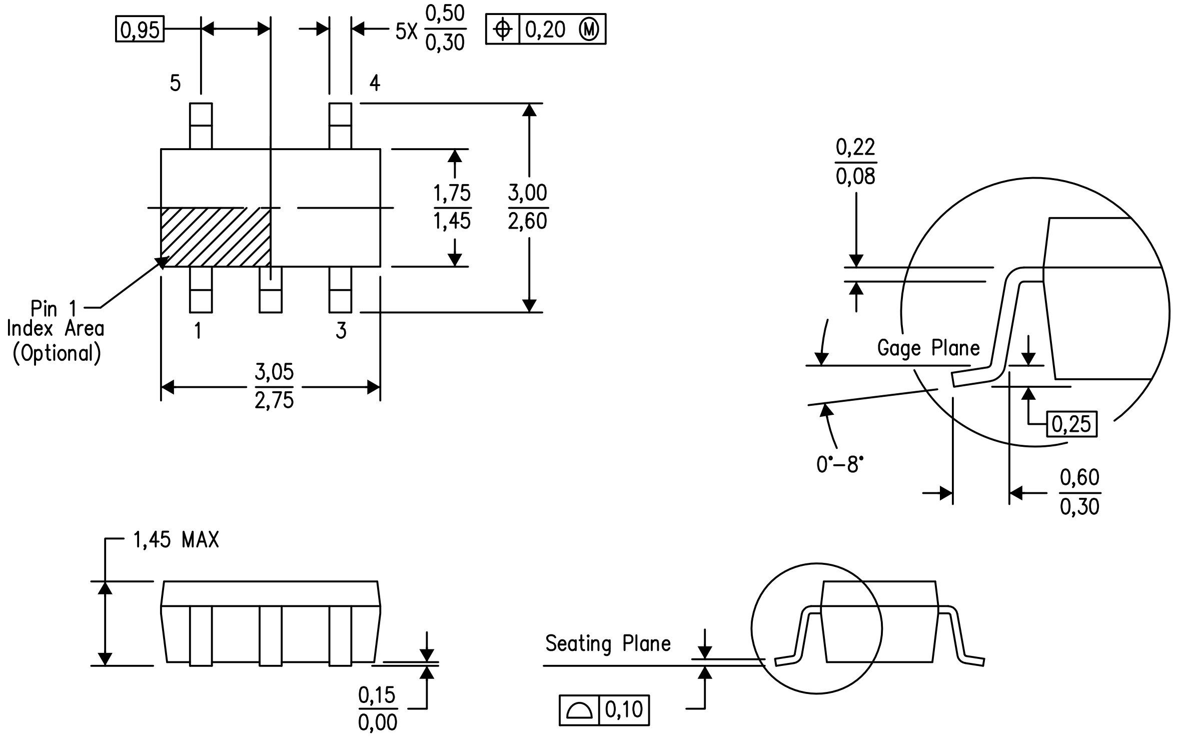
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

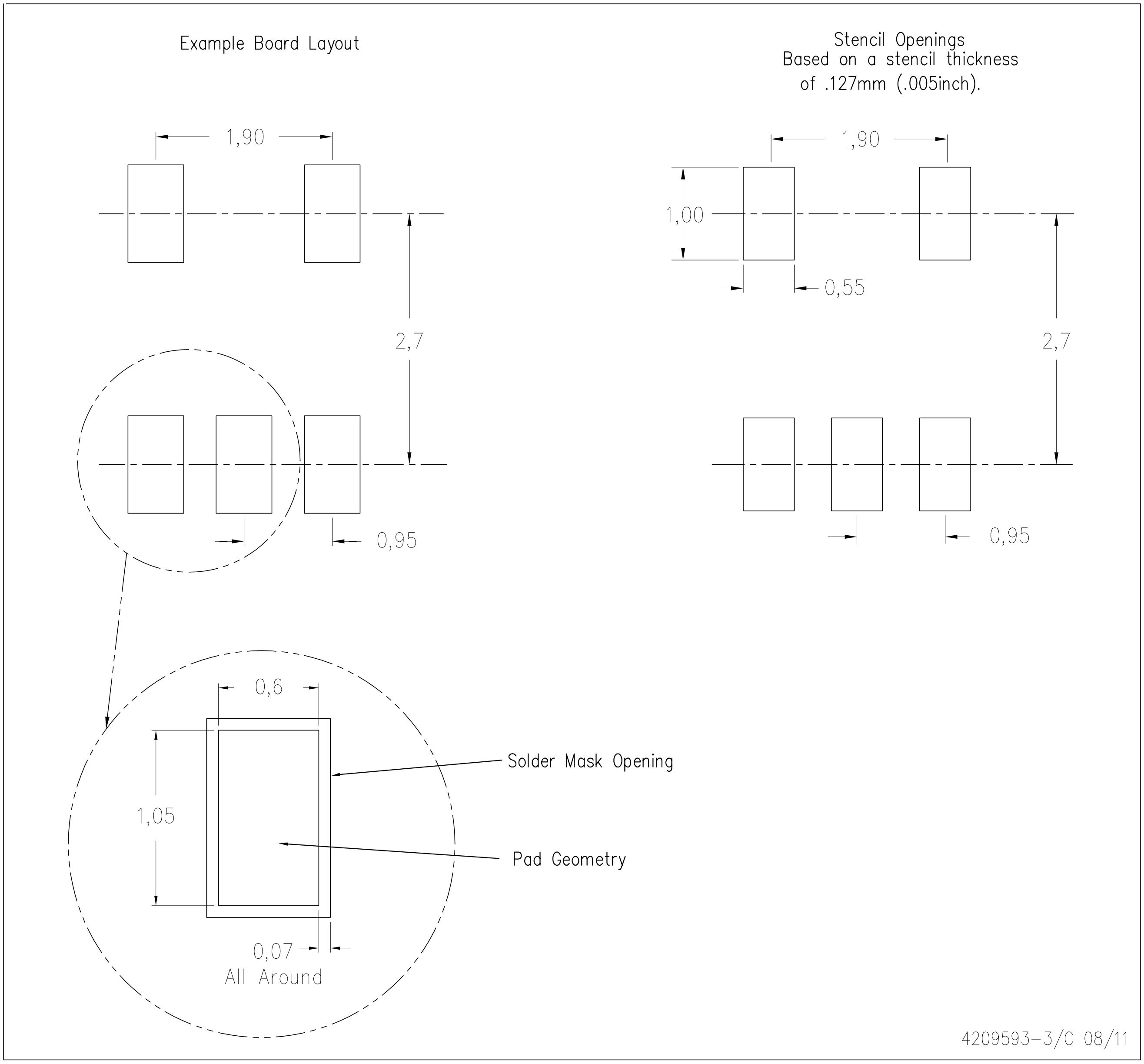
DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/N 12/14

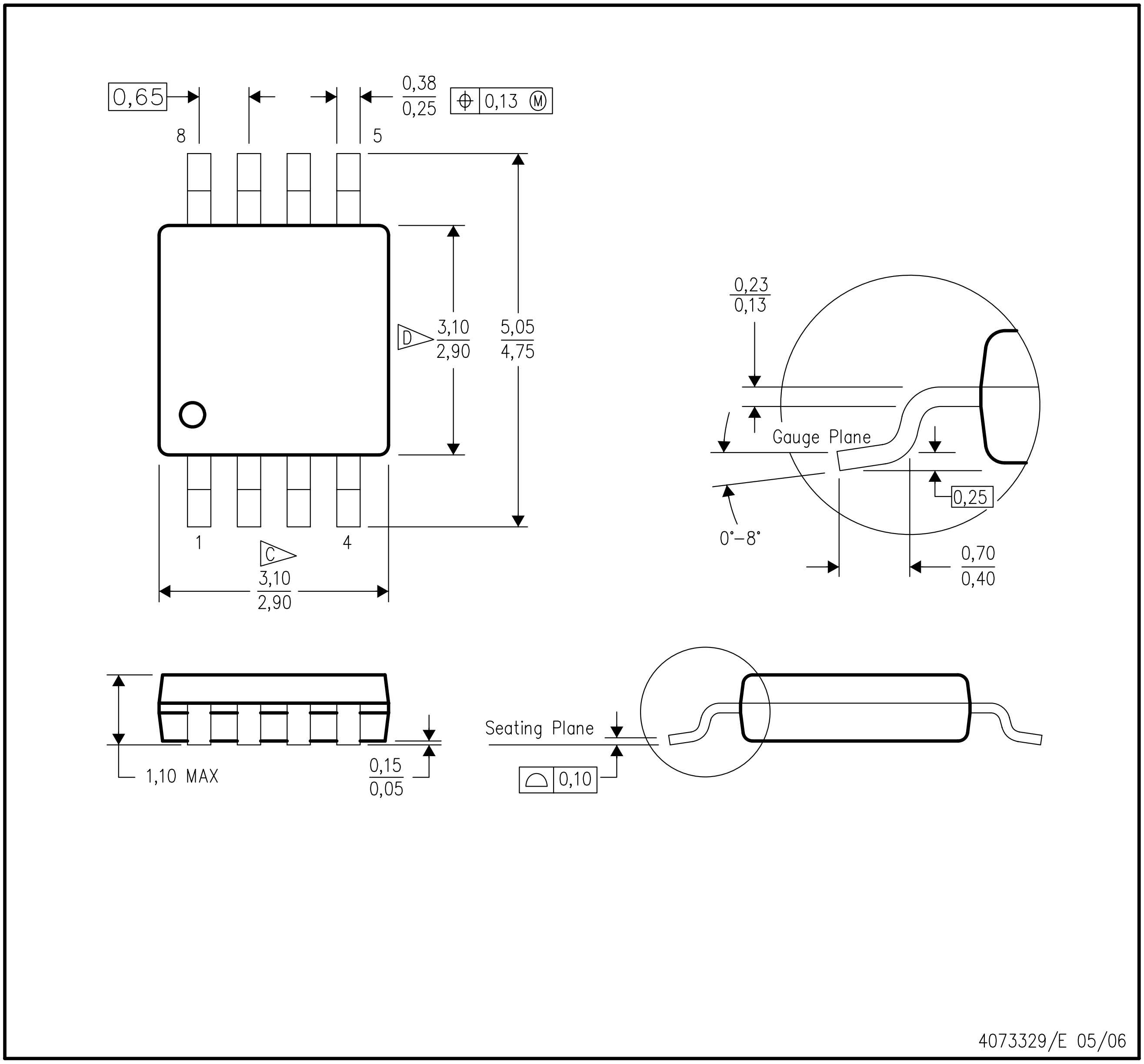
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



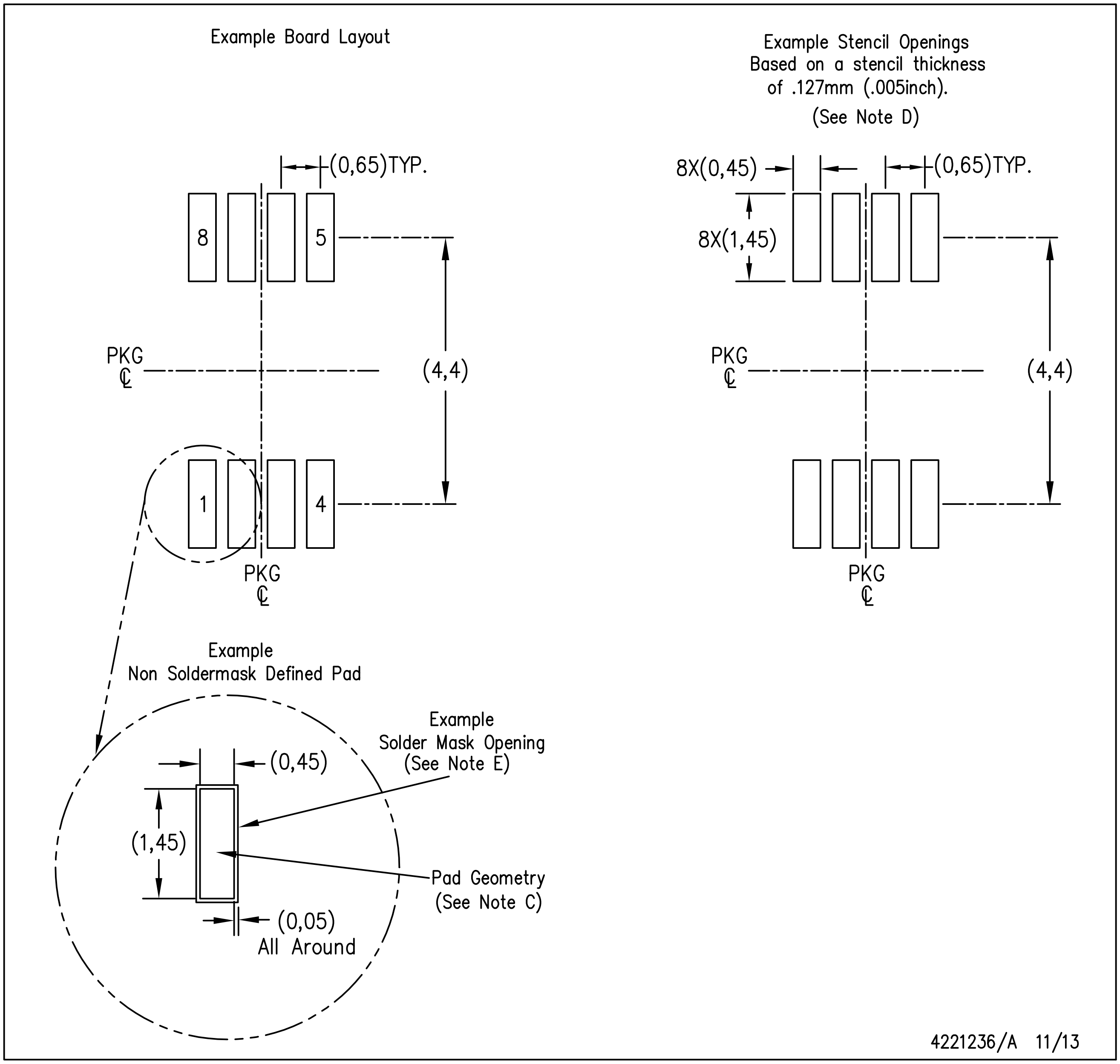
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8)   PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, “Designers”) understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers’ applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI’s provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, “TI Resources”) are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer’s company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI’s provision of TI Resources does not expand or otherwise alter TI’s applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED “AS IS” AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers’ own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer’s non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2017, Texas Instruments Incorporated