CC1350 SimpleLink™ Wireless MCU Silicon Errata

This document describes known exceptions to the functional specifications for the CC1350 SimpleLink™ device.

1 Known Design Exceptions to Functional Specifications

Advisory List

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Advisory	***Frequency Bands Not Yet Supported***

Description   The supported frequency ranges are 431 MHz to 527 MHz, 861 MHz to 1054 MHz, and 2152 MHz to 2635 MHz. Support for the 315-MHz and 779-MHz frequency bands may be added to the CC1350 at a later time.

Suggested Workaround   Functional testing at 315-MHz and 779-MHz frequency bands has been performed, but full characterization is not yet completed. Support for these frequency bands may be added when they are ready. Contact TI for more information through the Sub-1 GHz – Proprietary and 15.4 Star networks Forum on E2E.

Advisory	***Data Rates Not Yet Supported***

Description   The supported data rates at product release are 2.4 kbps to 100 kbps, and LRM 625 bps for Sub-1 GHz operation, and BLE 1 Mbps for 2.4 GHz operation. Support for other data rates will be added to the CC1350 at a later time.

Suggested Workaround   Functional testing of data rates outside the 2.4-kbps to 100-kbps range for Sub-1 GHz operation has been performed, but full characterization is not yet completed. Contact TI for more information through the Sub-1 GHz – Proprietary and 15.4 Star networks Forum on E2E.

Advisory	***Modulation Formats Not Yet Supported***

Description   4-FSK is not yet supported.

Suggested Workaround   Functional testing of 4-FSK has been performed, but full characterization is not yet completed. Support for 4-FSK will be added through a firmware or software upgrade when ready. Contact TI for more information through the Sub-1 GHz – Proprietary and 15.4 Star networks Forum on E2E.

Advisory	***Synthesizer Calibration Might Fail on Rare Occasions***

Description   The synthesizer (synth) calibration has been observed to fail on rare occasions. This will cause any radio command that requires a calibrated synth to fail.

Suggested Workaround   The workaround for a failed synth calibration is to calibrate again. For applications that use TI-RTOS or CC13xx Ware, but not the TI provided software stacks, it is recommended that proper run-time error handling is performed when executing a radio command. See the TI-RTOS documentation for error codes. For applications that use the software stacks delivered by Texas Instruments™ (BLE-Stack or TIMAC), no action is required because error handling is implemented by the stacks.

Advisory	***Reading From Flash While Performing Clock Switching of the High Speed Oscillators (XOSC_HF and RCOSC_HF) Will Cause the System to Hang***

Description

The CC1350 device contains five modules that can read from flash independently of each other. These five modules are:

- ARM® Cortex®-M3
- RF Core
- I2S
- DMA
- Crypto

Clock switching between XOSC_HF and RCOSC_HF can only be initiated by the Cortex-M3. While the Cortex-M3 performs clock switching, no other modules are allowed to read from the flash. The system will hang if any of the other four modules (RF core, I2S, DMA, Crypto) read from flash during this period.

Suggested Workaround

The user must make sure that the Cortex-M3 does not perform clock switching while any of the other four modules (RF core, I2S, DMA, Crypto) read from flash.

TI-RTOS

Clock switching from RCOSC_HF to XOSC_HF is done by calling Power_setDependency (XOSC_HF). The user must register a notification to be notified when the clock switching is completed. When the notification function is called by the power driver, the clock switching is completed and it is safe for all modules to read from flash again.

Clock switching from XOSC_HF to RCOSC_HF is done by calling Power_releaseDependency (XOSC_HF). When this function returns, the clock switching is completed and it is safe for all modules to read from flash again. The TI-RTOS radio driver never reads from flash, so it is safe to perform clock switching at all times when using this driver. However, it is up to the user to make sure that no clock switching is performed if the I2S, DMA, or Crypto modules read from flash.

Non-TI-RTOS

Clock switching is performed by calling the driverlib function OSCHfSourceSwitch(). When this function returns, it is safe for all modules to read from flash again. It is up to the user to make sure that no clock switching is performed if the RF core, I2S, DMA, or Crypto modules are read from flash.

Advisory	***Slave Mode can Sample New TX Data From SYSBUS Clock Domain Using SSPCLK With no Synchronization***

Description

When the SSI is programmed to operate in slave mode, the data written to the SSI data register in the SYSBUS clock domain can be sampled in the SSPCLK domain or without any synchronization. This condition occurs when the SSI Transmit FIFO is empty and the SSI Data register [TOP:SSI0/SSI1:DR : 0x4000_0008] write access occurs as a new SPI master transfer starts and the SSI slave-state machine samples data to transmit. This issue causes written data to be lost.

Suggested Workaround There is no software workaround to fix this issue.

Advisory	***Motorola® SPI Format Slave Mode Writes to Transmit FIFO can Lose Data***

Description

If the SSI is configured to operate in Motorola® SPI slave mode, it is possible to lose write data because of the following two conditions:

(i)   A write to the SSI data register [TOP:SSI0/SSI1:DR: 0x4000_0008] occurs between a new SPI master transfer starting and the end of the first bit of incoming data

(ii) A write to the SSI data register [TOP: SSI0/SSI1: DR: 0x4000_0008] occurs during the first bit of new incoming data in a back-to-back transfer sequence

Suggested Workaround There is no software workaround to fix this issue.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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