

## OPA167x Low-Distortion Audio Operational Amplifiers

### 1 Features

- Low Noise:  $4.5 \text{ nV}/\sqrt{\text{Hz}}$  at 1 kHz
- Low Distortion: 0.0001% at 1 kHz
- High Open-Loop Gain: 114dB
- High Common-Mode Rejection: 110 dB
- Low Quiescent Current:  
2 mA Per Channel
- Low Input Bias Current: 10 pA (Typical)
- Slew Rate:  $9 \text{ V}/\mu\text{s}$
- Wide Gain Bandwidth: 16 MHz ( $G = 1$ )
- Unity-Gain Stable
- Rail-to-Rail Output
- Wide Supply Range:  
 $\pm 2.25 \text{ V}$  to  $\pm 18 \text{ V}$ , or  $4.5 \text{ V}$  to  $36 \text{ V}$
- Dual-Channel and Quad-Channel Versions
- Small Package Sizes:  
Dual-Channel: SO-8 and MSOP-8  
Quad-Channel: SO-14 and TSSOP-14

### 2 Applications

- Analog Signal Conditioning
- Analog and Digital Mixers
- Audio Effects Pedals
- A/V Receivers
- Car Audio Systems

### 3 Description

The OPA1678 (dual-channel) and OPA1679 (quad-channel) operational amplifiers offer higher system-level performance over legacy op amps commonly used in audio circuitry. The OPA167x amplifiers achieve a low  $4.5\text{-nV}/\sqrt{\text{Hz}}$  noise density and low distortion of 0.0001% at 1 kHz which improves audio signal fidelity. They also offer rail-to-rail output swing to within 800 mV with a 2-k $\Omega$  load, which increases headroom and maximizes dynamic range.

The OPA1678 and OPA1679 operate over a very wide supply range of  $\pm 2.25 \text{ V}$  to  $\pm 18 \text{ V}$  or ( $4.5 \text{ V}$  to  $36 \text{ V}$ ) on only 2 mA of supply current to accommodate the power supply constraints of many types of audio products. These op amps are unity-gain stable and provide excellent dynamic behavior over a wide range of load conditions allowing them to be used in many audio circuits.

The OPA167x amplifiers use completely independent internal circuitry for lowest crosstalk and freedom from interactions between channels, even when overdriven or overloaded.

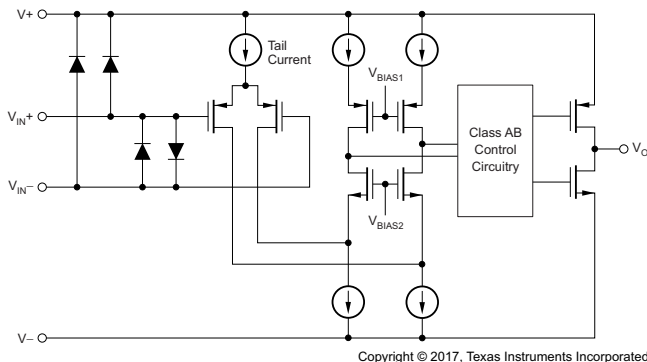
The OPA167x temperature ranges are specified from  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

#### Device Information<sup>(1)</sup>

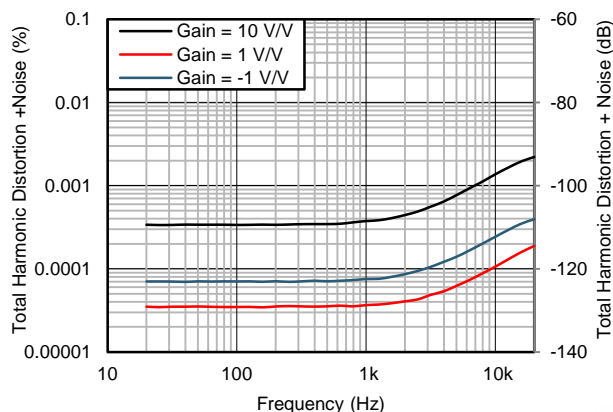
PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA1678	SOIC (8)	4.90 mm x 3.91 mm
	VSSOP (8)	3.00 mm x 3.00 mm
OPA1679	SOIC (14)	8.65 mm x 3.91 mm
	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified Internal Schematic



#### THD+N vs Frequency (2-k $\Omega$ Load)



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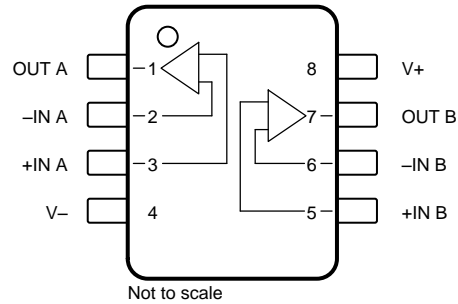
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2017	SBOS855	Initial release.

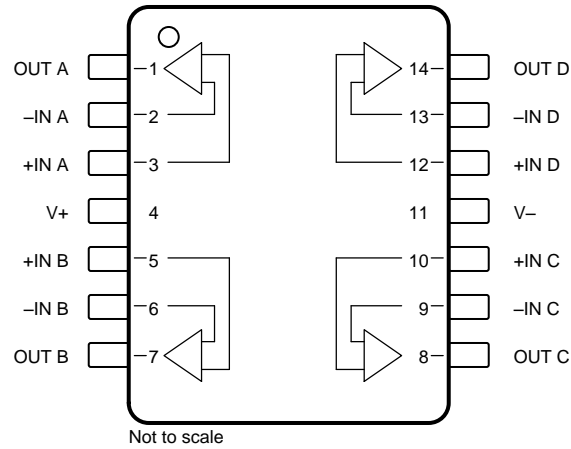
## 5 Pin Configuration and Functions

**OPA1678 D and DGK Packages  
8-Pin SOIC and VSSOP  
Top View**



**Pin Functions: OPA1678**

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
-IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V-	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

**OPA1679 D and PW Packages  
14-Pin SOIC and TSSOP  
Top View**

**Pin Functions: OPA1679**

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
-IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
-IN C	9	I	Inverting input, channel C
+IN D	10	I	Noninverting input, channel C
-IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V+	4	—	Positive (highest) power supply
V-	11	—	Negative (lowest) power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	Supply voltage, $V_S = (V+) - (V-)$		40	V
	Input	$(V-) - 0.5$	$(V+) + 0.5$	V
Current	Input (all pins except power-supply pins)	-10	10	mA
	Output short-circuit <sup>(2)</sup>	Continuous		
Temperature	Operating, $T_A$	-55	125	°C
	Junction, $T_J$		200	°C
	Storage, $T_{stg}$	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Short-circuit to  $V_S / 2$  (ground in symmetrical dual-supply setups), one amplifier per package.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000
		Machine model (MM)	±200

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Supply voltage	4.5 (±2.25)		36 (±18)	V
$T_A$	Operating temperature	-40		85	°C

#### 6.4 Thermal Information: OPA1678

THERMAL METRIC <sup>(1)</sup>		OPA1678		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	144	219	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77	79	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62	104	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	28	15	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	61	102	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

#### 6.5 Thermal Information: OPA1679

THERMAL METRIC <sup>(1)</sup>		OPA1679		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90	127	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55	47	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44	59	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	20	5.5	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	44	58	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.6 Electrical Characteristics: $V_S = \pm 15\text{ V}$

at  $T_A = 25^\circ\text{C}$ ,  $R_L = 2\text{ k}\Omega$ , and  $V_{CM} = V_{OUT} = \text{midsupply}$ , unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>AUDIO PERFORMANCE</b>						
THD+N	Total harmonic distortion + noise	$G = 1$ $R_L = 600\ \Omega$ $f = 1\text{ kHz}$ $V_O = 3\text{ V}_{RMS}$	0.0001%			
				-120		dB
IMD	Intermodulation distortion	$G = 1$ $V_O = 3\text{ V}_{RMS}$	SMPTE/DIN Two-Tone, 4:1 (60 Hz and 7 kHz)	0.0001%		
				-120		dB
			DIM 30 (3-kHz square wave and 15-kHz sine wave)	0.0001%		
			-120		dB	
			0.0001%			
			-120		dB	
<b>FREQUENCY RESPONSE</b>						
GBW	Gain-bandwidth product	$G = 1$		16		MHz
SR	Slew rate	$G = -1$		9		V/ $\mu\text{s}$
	Full power bandwidth <sup>(1)</sup>	$V_O = 1\text{ V}_P$		1.4		MHz
	Overload recovery time	$G = -10$		1		$\mu\text{s}$
	Channel separation (dual and quad)	$f = 1\text{ kHz}$		-130		dB
<b>NOISE</b>						
$e_n$	Input voltage noise	$f = 20\text{ Hz to } 20\text{ kHz}$ $f = 0.1\text{ Hz to } 10\text{ kHz}$	5.4			$\mu\text{V}_{PP}$
			1.74			
	Input voltage noise density	$f = 1\text{ kHz}$		4.5		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input current noise density	$f = 1\text{ kHz}$		3		$\text{fA}/\sqrt{\text{Hz}}$
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage	$V_S = \pm 2.25\text{ V to } \pm 18\text{ V}$		$\pm 0.5$	$\pm 2$	mV
		$V_S = \pm 2.25\text{ V to } \pm 18\text{ V}$ $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ <sup>(2)</sup>		2		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = \pm 2.25\text{ V to } \pm 18\text{ V}$		3	8	$\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current	$V_{CM} = 0\text{ V}$		$\pm 10$		pA
$I_{OS}$	Input offset current	$V_{CM} = 0\text{ V}$		$\pm 10$		pA
<b>INPUT VOLTAGE RANGE</b>						
$V_{CM}$	Common-mode voltage range		$(V-) + 0.5$		$(V+) - 2$	V
CMRR	Common-mode rejection ratio		100	110		dB
<b>INPUT IMPEDANCE</b>						
	Differential		100    6			M $\Omega$    pF
	Common-mode		6000    2			G $\Omega$    pF
<b>OPEN-LOOP GAIN</b>						
$A_{OL}$	Open-loop voltage gain	$(V-) + 0.8\text{ V} \leq V_O \leq (V+) - 0.8\text{ V}$ $R_L = 2\text{ k}\Omega$	106	114		dB
<b>OUTPUT</b>						
$V_{OUT}$	Voltage output	$R_L = 2\text{ k}\Omega$	$(V-) + 0.8$		$(V+) - 0.8$	V
$I_{OUT}$	Output current		See <a href="#">Typical Characteristics</a> curves			mA
$Z_O$	Open-loop output impedance	$f = 1\text{ MHz}$	See <a href="#">Typical Characteristics</a> curves			$\Omega$
$I_{SC}$	Short-circuit current <sup>(3)</sup>		50–50			mA
$C_{LOAD}$	Capacitive load drive		100			pF

(1) Full-power bandwidth =  $SR / (2\pi \times V_P)$ , where SR = slew rate.

(2) Specified by design and characterization

(3) One channel at a time

**Electrical Characteristics:  $V_S = \pm 15\text{ V}$  (continued)**

 at  $T_A = 25^\circ\text{C}$ ,  $R_L = 2\text{ k}\Omega$ , and  $V_{CM} = V_{OUT} = \text{midsupply}$ , unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>						
$V_S$	Specified voltage		$\pm 2.25$		$\pm 18$	V
$I_Q$	Quiescent current (per channel)	$I_{OUT} = 0\text{ A}$		2	2.5	mA
		$I_{OUT} = 0\text{ A}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}^{(2)}$			2.8	mA
<b>TEMPERATURE</b>						
	Specified range		-40		85	$^\circ\text{C}$
	Operating range		-55		125	$^\circ\text{C}$



## 6.7 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , unless otherwise noted

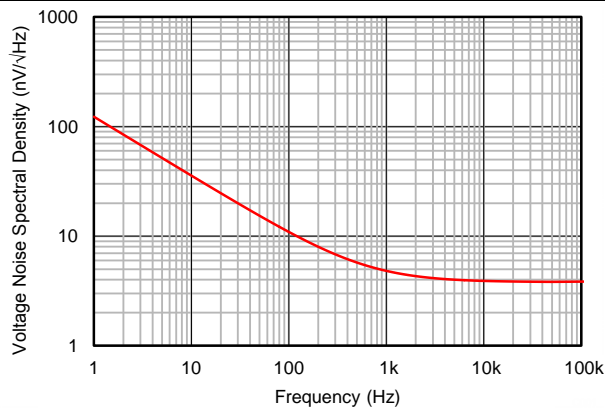


Figure 1. Input Voltage Noise Density vs Frequency

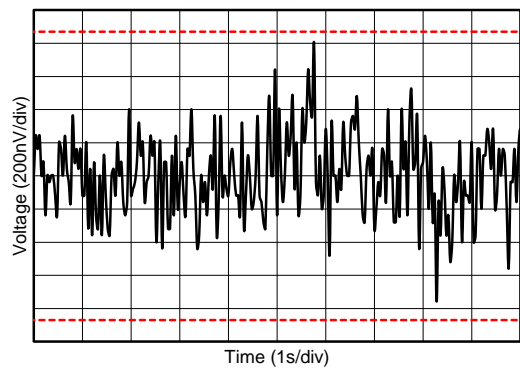


Figure 2. 0.1-Hz to 10-Hz Noise

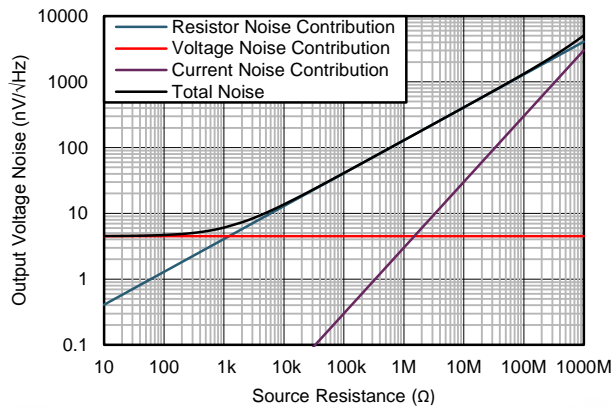


Figure 3. Voltage Noise vs Source Resistance

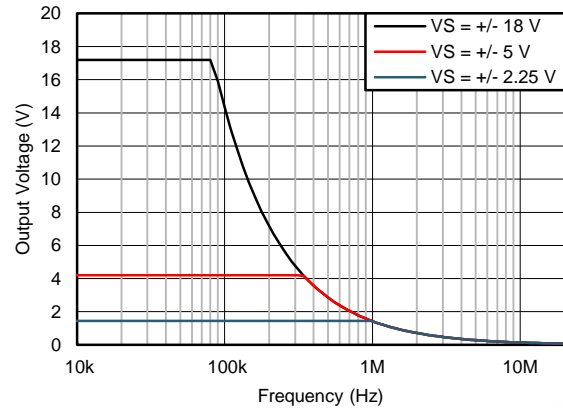


Figure 4. Maximum Output Voltage vs Frequency

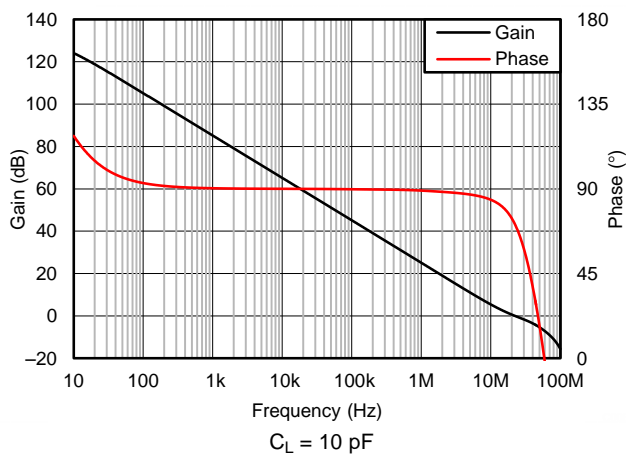


Figure 5. Open-Loop Gain and Phase vs Frequency

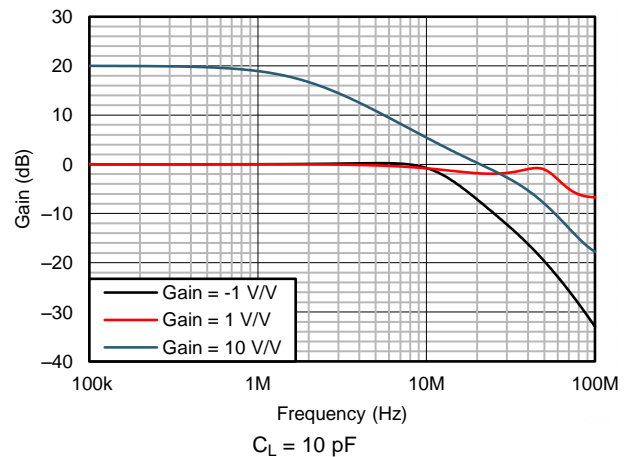
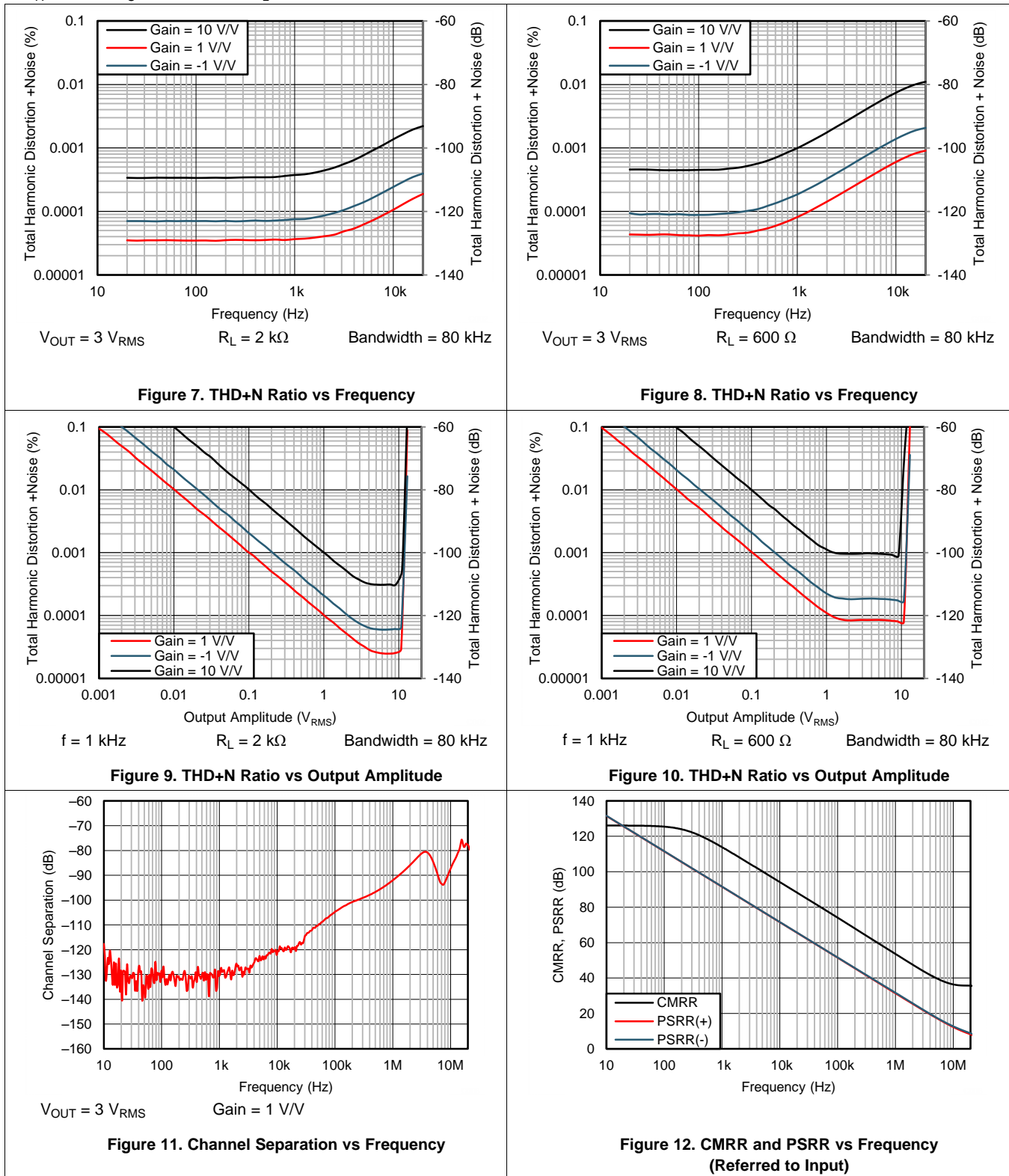


Figure 6. Closed-Loop Gain vs Frequency

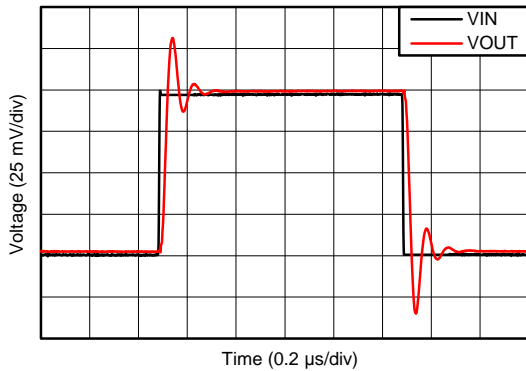
### Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , unless otherwise noted



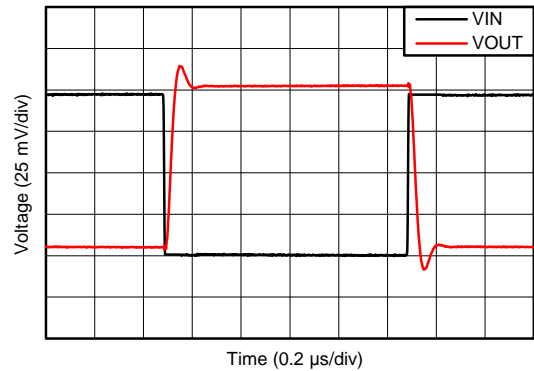
Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , unless otherwise noted



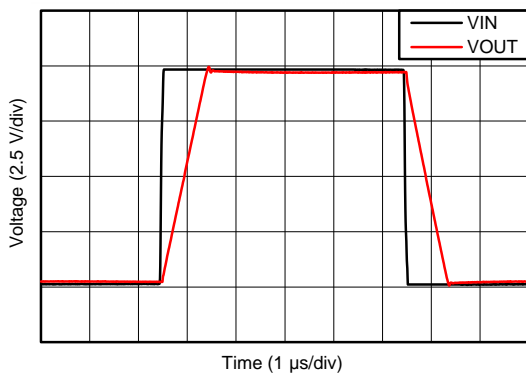
Gain = 1 V/V  $C_L = 100\text{ pF}$

Figure 13. Small-Signal Step Response (100 mV)



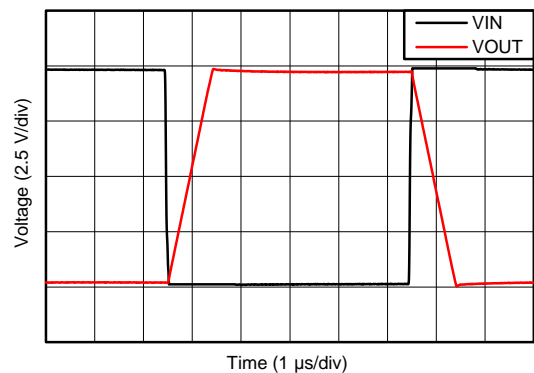
Gain = -1 V/V  $C_L = 100\text{ pF}$

Figure 14. Small-Signal Step Response (100 mV)



Gain = +1 V/V  $R_F = 2\text{ k}\Omega$   $C_L = 100\text{ pF}$

Figure 15. Large-Signal Step Response



Gain = -1 V/V  $C_L = 100\text{ pF}$

Figure 16. Large-Signal Step Response

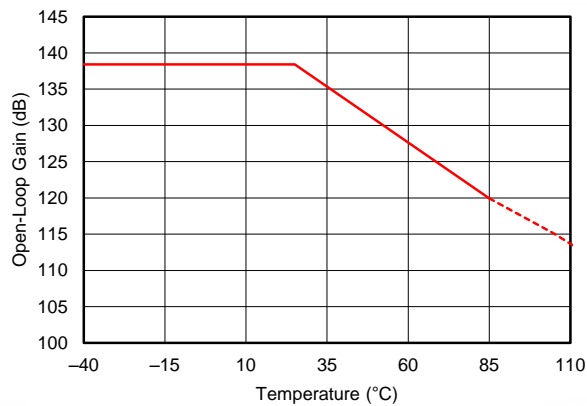


Figure 17. Open-Loop Gain vs Temperature

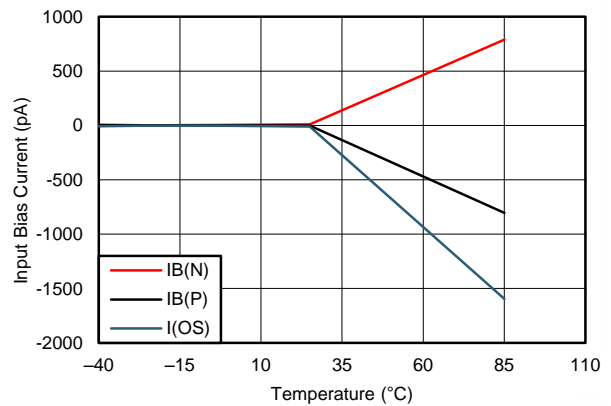
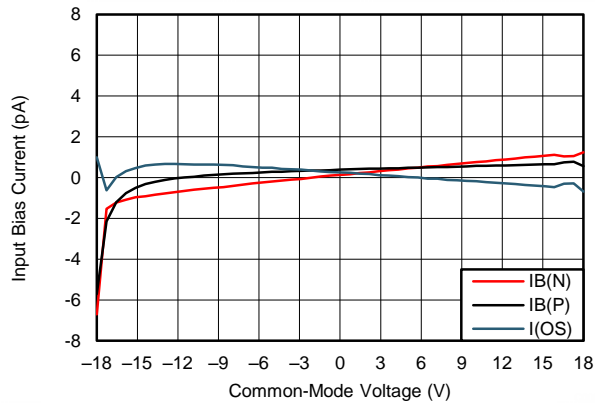


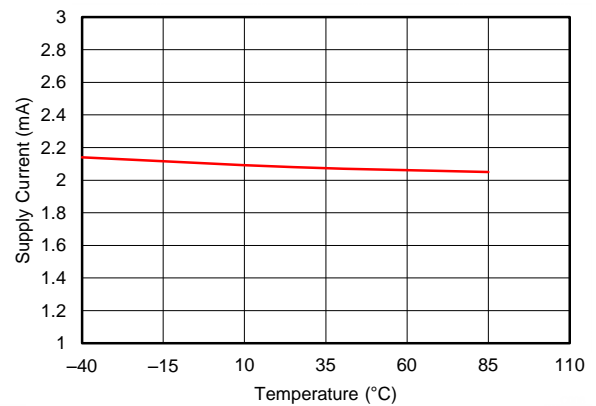
Figure 18.  $I_B$  and  $I_{OS}$  vs Temperature

**Typical Characteristics (continued)**

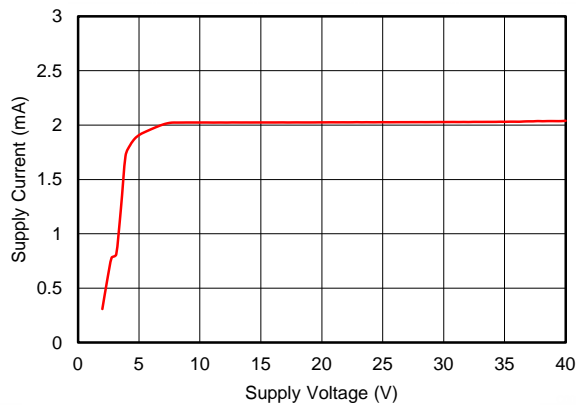
at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , unless otherwise noted



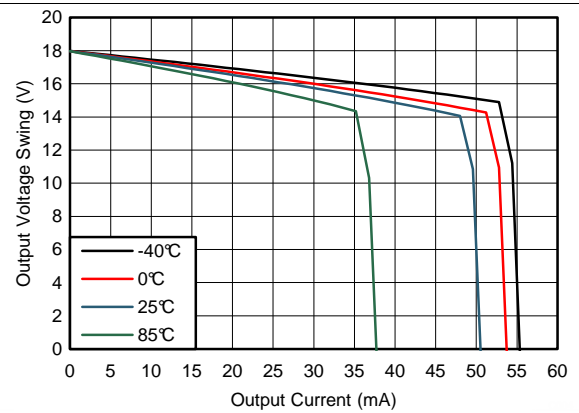
**Figure 19.  $I_B$  and  $I_{OS}$  vs Common-Mode Voltage**



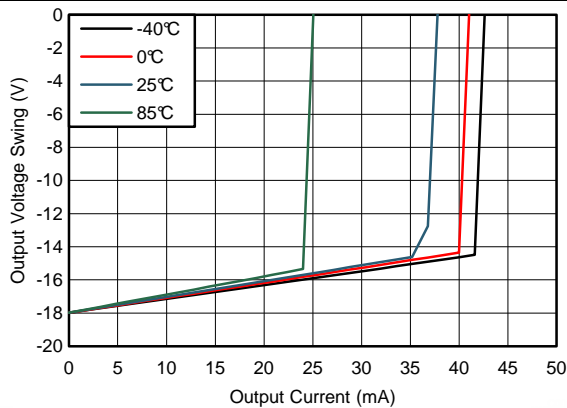
**Figure 20. Supply Current vs Temperature**



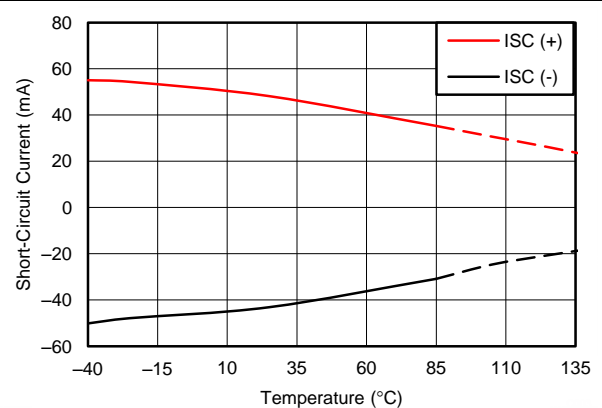
**Figure 21. Supply Current vs Supply Voltage**



**Figure 22. Output Voltage vs Output Current (Sourcing)**



**Figure 23. Output Voltage vs Output Current (Sinking)**



**Figure 24. Short-Circuit Current vs Temperature**

Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , unless otherwise noted

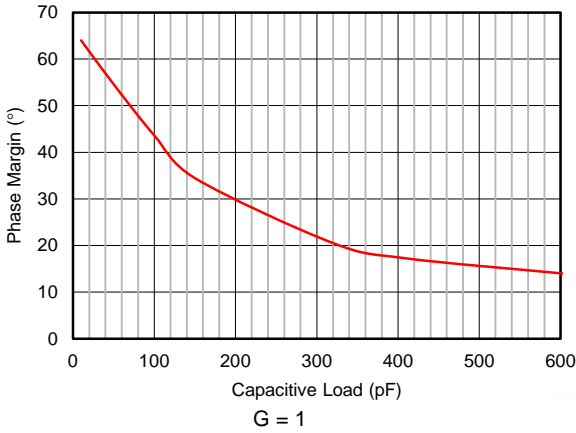


Figure 25. Phase Margin vs Capacitive Load

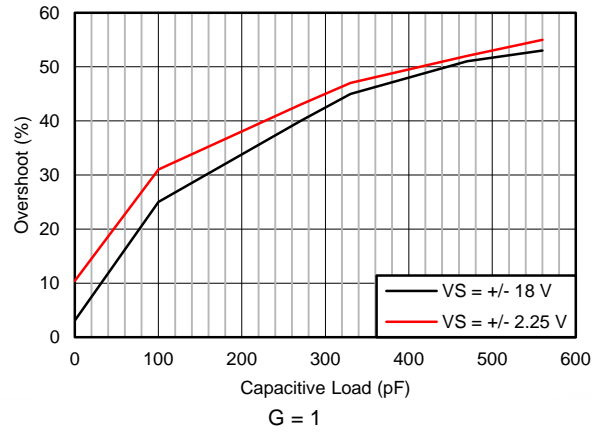
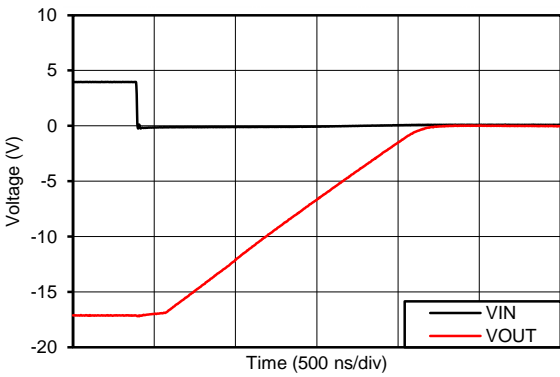
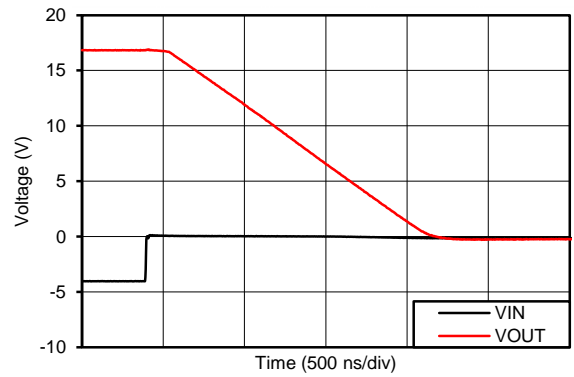


Figure 26. Percent Overshoot vs Capacitive Load



Gain = -10 V/V

Figure 27. Negative Overload Recovery



Gain = -10 V/V

Figure 28. Positive Overload Recovery

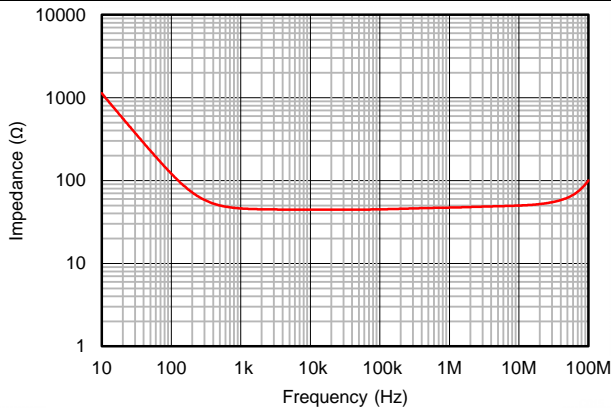
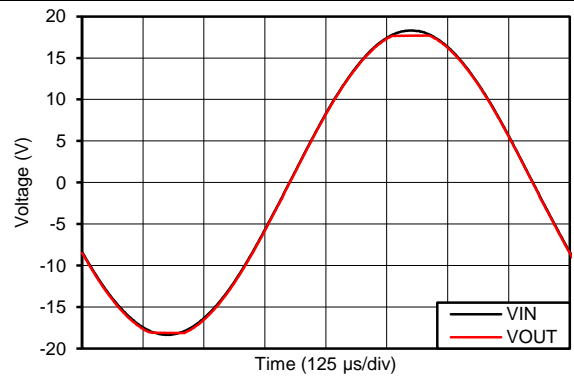


Figure 29. Open-Loop Output Impedance vs Frequency



Gain = 1 V/V

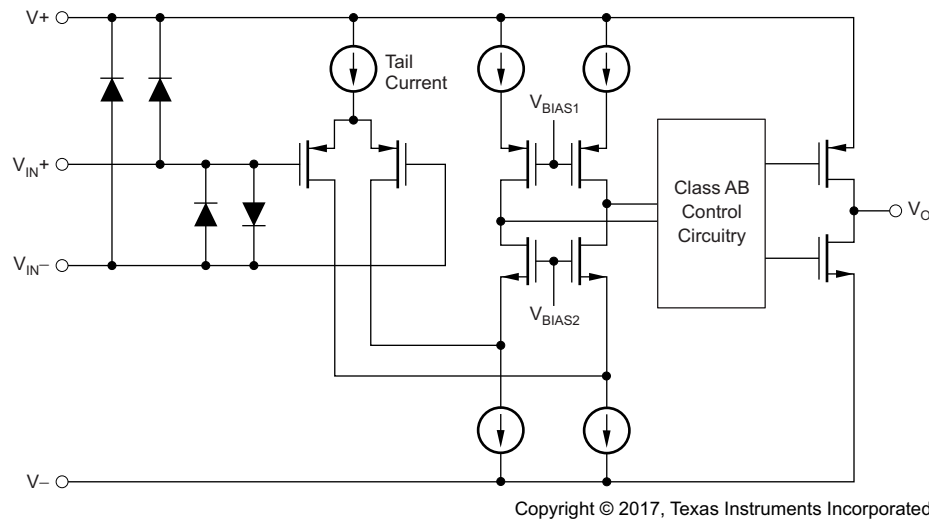
Figure 30. No Phase Reversal

## 7 Detailed Description

### 7.1 Overview

The OPA167x devices are unity-gain stable, dual- and quad-channel op amps with low noise and distortion. The [Functional Block Diagram](#) shows a simplified schematic of the OPA167x (one channel shown). The device consists of a low noise input stage with a folded cascode and a rail-to-rail output stage. This topology exhibits superior noise and distortion performance across a wide range of supply voltages that are not delivered by legacy commodity audio operational amplifiers.

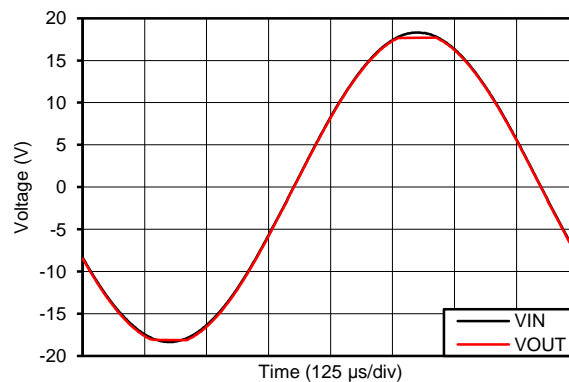
### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Phase Reversal Protection

The OPA167x family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPA167x prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in [Figure 31](#).



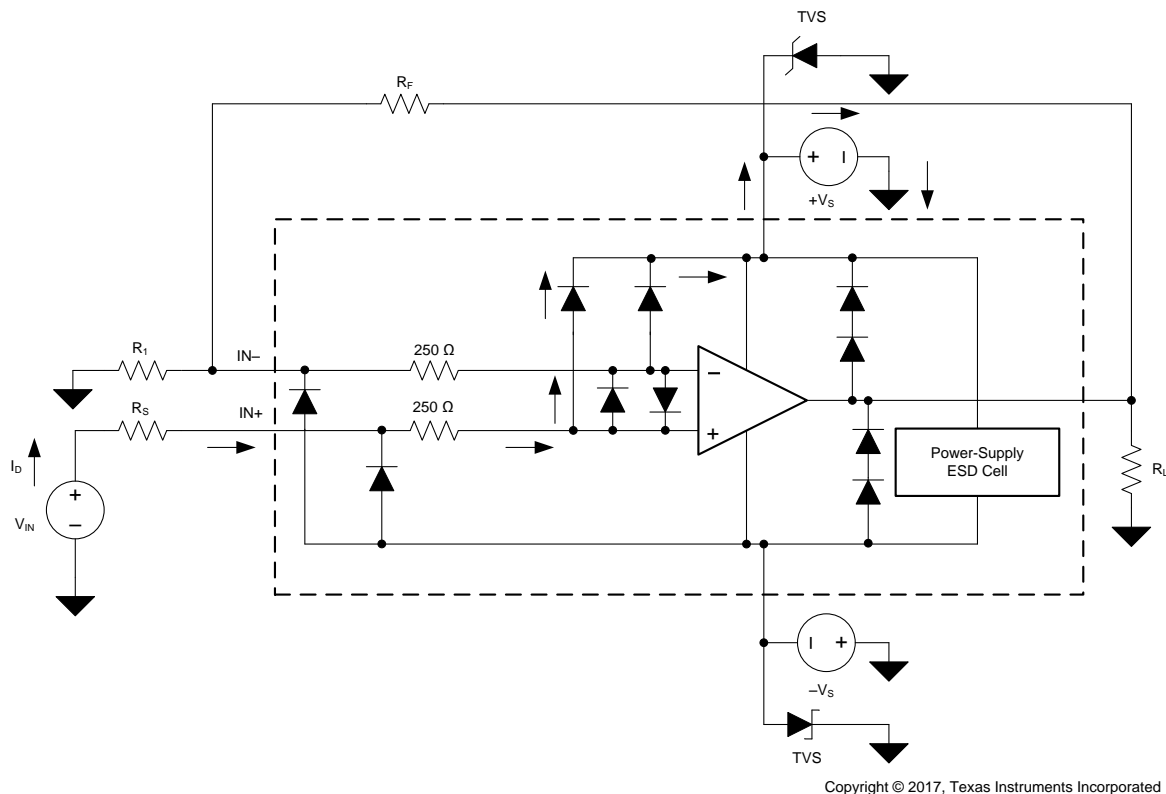
**Figure 31. Output Waveform Devoid of Phase Reversal During an Input Overdrive Condition**

## Feature Description (continued)

### 7.3.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 32 illustrates the ESD circuits contained in the OPA167x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.



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**Figure 32. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application**

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA167x but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

## Feature Description (continued)

When the operational amplifier connects into a circuit (see [Figure 32](#)), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

[Figure 32](#) shows a specific example where the input voltage ( $V_{IN}$ ) exceeds the positive supply voltage ( $V+$ ) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If  $V+$  can sink the current, one of the upper input steering diodes conducts and directs current to  $V+$ . Excessively high current levels can flow with increasingly higher  $V_{IN}$ . As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current,  $V_{IN}$  can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies ( $V+$  or  $V-$ ) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see [Figure 32](#). Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

### 7.3.3 EMI Rejection Ratio (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this document provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

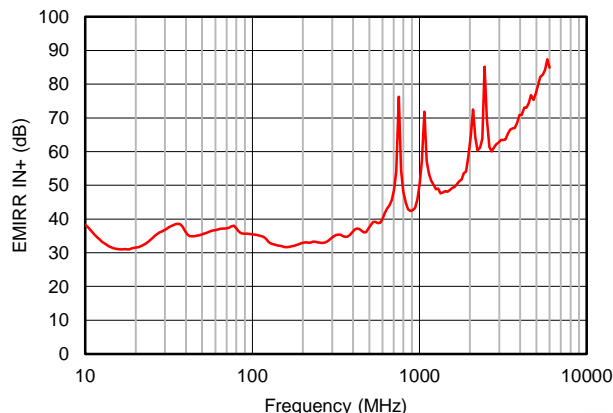
- Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
- EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input pin can be isolated on a printed-circuit-board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input pin with no complex interactions from other components or connecting PCB traces.

A more formal discussion of the EMIRR IN+ definition and test method is provided in the [EMI Rejection Ratio of Operational Amplifiers](#) application report, available for download at [www.ti.com](http://www.ti.com).

The EMIRR IN+ of the OPA167x is plotted versus frequency in [Figure 33](#). If available, any dual and quad operational amplifier device versions have nearly identical EMIRR IN+ performance. The OPA167x unity-gain bandwidth is 16 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.



**Feature Description (continued)**



**Figure 33. OPA167x EMIRR vs Frequency**

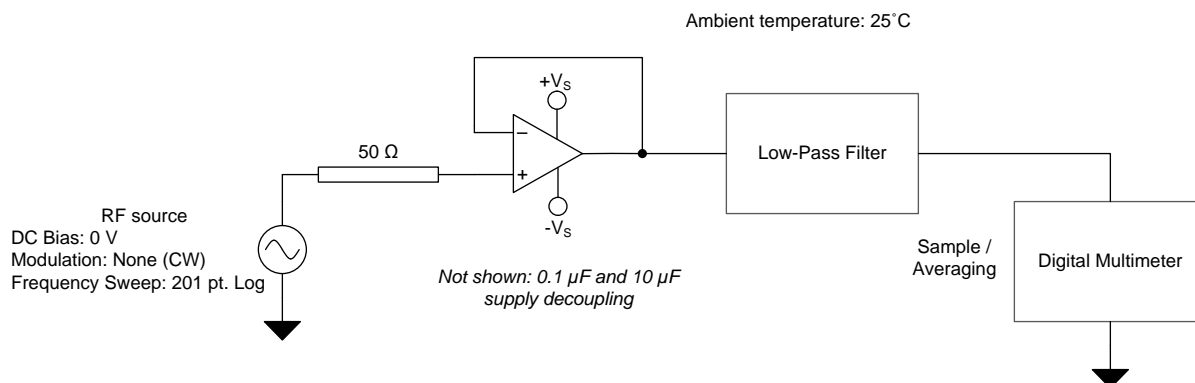
Table 1 lists the EMIRR IN+ values for the OPA167x at particular frequencies commonly encountered in real-world applications. Applications listed in Table 1 can be centered on or operated near the particular frequency shown. This information can be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

**Table 1. OPA167x EMIRR IN+ for Frequencies of Interest**

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, UHF	36 dB
900 MHz	GSM, radio communication and navigation, GPS (to 1.6 GHz), ISM, aeronautical mobile, UHF	42 dB
1.8 GHz	GSM, mobile personal comm. broadband, satellite, L-band	52 dB
2.4 GHz	802.11b/g/n, Bluetooth™, mobile personal comm., ISM, amateur radio and satellite, S-band	64 dB
3.6 GHz	Radiolocation, aero comm./nav., satellite, mobile, S-band	67 dB
5 GHz	802.11a/n, aero communication and navigation, mobile communication, space and satellite operation, C-band	77 dB

### 7.3.3.1 EMIRR IN+ Test Configuration

Figure 34 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the operational amplifier noninverting input pin using a transmission line. The operational amplifier is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the operational amplifier input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting dc offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that can interfere with multimeter accuracy. See the [EMI Rejection Ratio of Operational Amplifiers](#) application report for more details.



**Figure 34. EMIRR IN+ Test Configuration Schematic**

## 7.4 Device Functional Modes

### 7.4.1 Operating Voltage

The OPA167x series op amps operate from  $\pm 2.25$  V to  $\pm 18$  V supplies while maintaining excellent performance. The OPA167x series can operate with as little as 4.5 V between the supplies and with up to 36 V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA167x series, power-supply voltages are not required to be equal. For example, the positive supply can be set to 25 V with the negative supply at  $-5$  V.

In all cases, the common-mode voltage must be maintained within the specified range. In addition, key parameters are ensured over the specified temperature range of  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ . Parameters that vary significantly with operating voltage or temperature are shown in the [Typical Characteristics](#) section.

## 8 Application and Implementation

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### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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### 8.1 Application Information

#### 8.1.1 Capacitive Loads

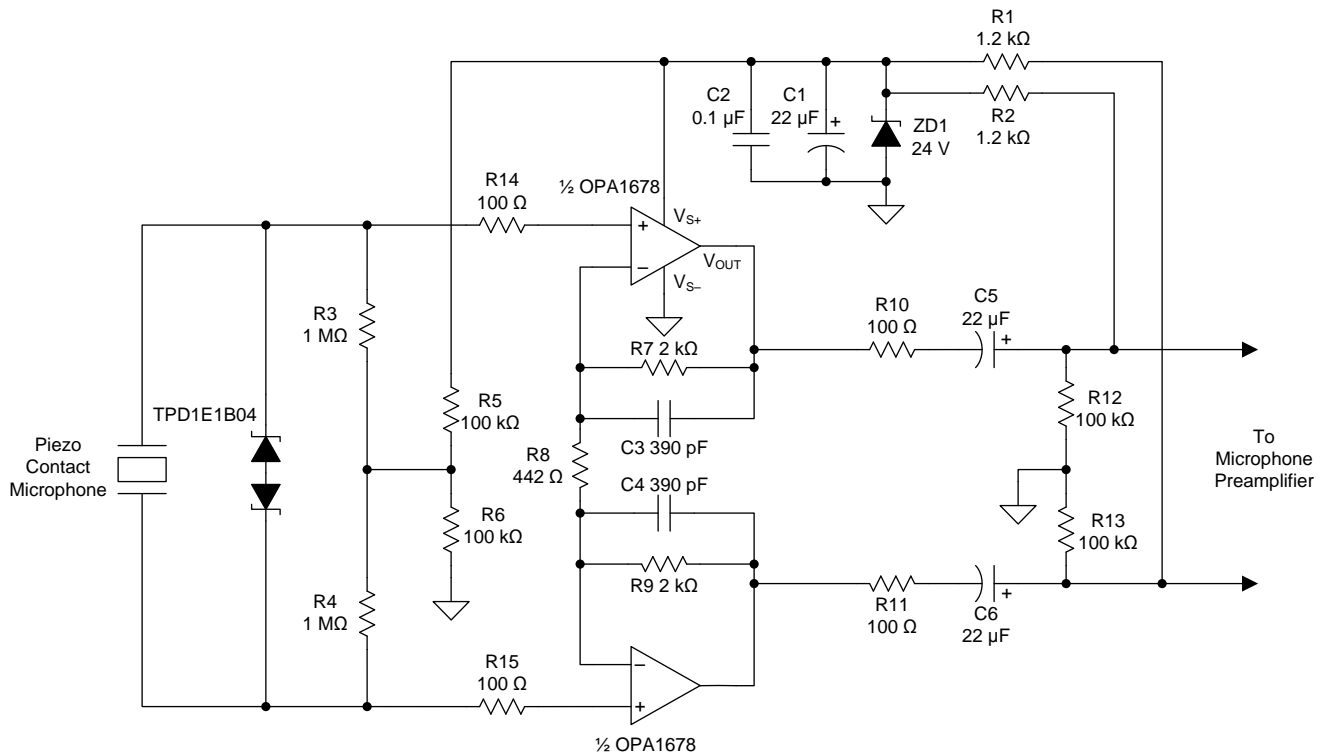
The dynamic characteristics of the OPA167x series are optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor ( $R_S$  equal to 50  $\Omega$ , for example) in series with the output.

This small series resistor also prevents excess power dissipation if the output of the device becomes shorted. For more details about analysis techniques and application circuits, see the [Feedback Plots Define Op Amp AC Performance](#) application report, available for download from the TI website ([www.ti.com](http://www.ti.com)).

## 8.2 Typical Application

Contact microphones are useful for amplifying the sound of musical instruments which do not contain electrical pickups, such as acoustic guitars and violins. Most contact microphones use a piezo element to convert vibrations in the body of the musical instrument to a voltage which may be amplified or recorded. The low noise and low input bias current of the OPA1678 make the device an excellent choice for high impedance preamplifiers for piezo elements. This preamplifier circuit provides high input impedance for the piezo element but has low output impedance for driving long cable runs. The circuit is also designed to be powered from 48-V phantom power which is commonly available in professional microphone preamplifiers and recording consoles.

A TINA-TI™ simulation schematic of the circuit below is available in the *Tools and Software* section of the OPA167x [product folder](#).



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**Figure 35. Phantom-Powered Preamplifier for Piezo Contact Microphones**

### 8.2.1 Design Requirements

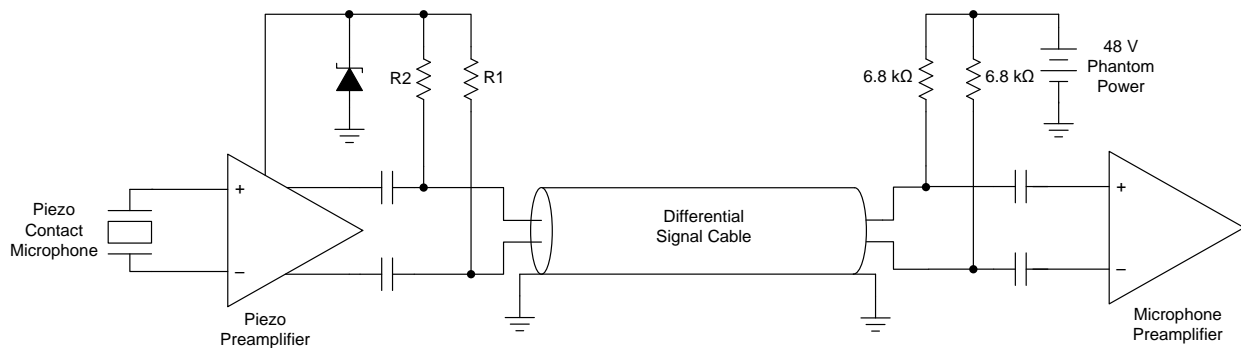
- –3 dB Bandwidth: 20 Hz to 20 kHz
- Gain: 20 dB (10 V/V)
- Piezo Element Capacitance: 8 nF (9-kHz resonance)

## Typical Application (continued)

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Power Supply

In professional audio systems, phantom power is applied to the two signal lines which carry a differential audio signal from the microphone. Figure 36 is a diagram of the system showing 48-V phantom power applied to the differential signal lines between the piezo preamplifier output and the input of a professional microphone preamplifier.



**Figure 36. System Diagram Showing the Application of Phantom Power to the Audio Signal Lines**

A voltage divider is used to extract the common-mode phantom power from the differential audio signal in this type of system. The voltage at center point of the voltage divider formed by R1 and R2 does not change when audio signals are present on the signal lines (assuming R1 and R2 are matched). A Zener diode forces the voltage at the center point of R1 and R2 to a regulated voltage. The values of R1 and R2 is determined by the allowable voltage drop across these resistors in the current delivered to both op amp channels and the Zener diode. There are two power supply current pathways in parallel, each sharing half the total current of the op amp and Zener diode. Resistors R1 and R2 can be calculated using :

$$R_1 = R_2 = R_{PS}$$

$$\frac{V_{ZD}}{\left(\frac{I_{OPA}}{2} + \frac{I_{ZD}}{2}\right)} - 6.8 \text{ k}\Omega = R_{PS}$$

A 24-V Zener diode is selected for this design, and 1 mA of current flows through the diode at idle conditions to maintain the reverse-biased condition of the Zener. The maximum idle power supply current of both op amp channels is 5 mA. Inserting these values into gives the values for R1 and R2 shown in .

$$\frac{24V}{\left(\frac{I_{OPA}}{2} + \frac{I_{ZD}}{2}\right)} - 6.8 \text{ k}\Omega = \frac{24V}{\left(\frac{5.0 \text{ mA}}{2} + \frac{1.0 \text{ mA}}{2}\right)} - 6.8 \text{ k}\Omega = 1.2 \text{ k}\Omega = R_{PS}$$

Using a value of 1.2 kΩ for resistors R1 and R2 establishes a 1-mA current through the Zener diode and properly regulate the node to 24 V. Capacitor C1 forms a low-pass filter with resistors R1 and R2 to filter the Zener diode noise and any residual differential audio signals. Mismatch in the values of R1 and R2 causes a portion of the audio signal to appear at the voltage divider center point. The corner frequency of the low-pass filter must be set below the audio band, as shown in .

$$C_1 \geq \frac{1}{2 \cdot \pi \cdot R_1 \parallel R_2 \cdot f_{-3dB}} \geq \frac{1}{2 \cdot \pi \cdot 600 \Omega \cdot 20 \text{ Hz}} \geq 13 \mu\text{F} \rightarrow 22 \mu\text{F}$$

A 22-μF capacitor is selected because the capacitor meets the requirements for power supply filtering and is a widely available denomination. A 0.1-μF capacitor (C2) is added in parallel with C1 as a high-frequency bypass capacitor.

## Typical Application (continued)

### 8.2.2.2 Input Network

Resistors R3 and R4 provide a pathway for the input bias current of the OPA1678 while maintaining the high input impedance of the circuit. The values of R3 and R4 are determined by the contact microphone capacitance and the required low-frequency response. The  $-3$ -dB frequency formed by the microphone capacitance and amplifier input impedance is given in :

$$F_{-3dB} = \frac{1}{2 \cdot \pi \cdot (R_3 + R_4) \cdot C_{MIC}} \leq 20 \text{ Hz}$$

A piezo element with 8 nF of capacitance was selected for this design because the 9-kHz resonance is towards the upper end of the audible bandwidth and is less likely to affect the frequency response of many musical instruments. The minimum value for resistors R3 and R4 is then calculated with [Equation 1](#):

$$R_3 = R_4 = R_{IN}$$

$$R_{IN} \geq \frac{1}{4 \cdot \pi \cdot F_{-3dB} \cdot C_{MIC}} \geq \frac{1}{4 \cdot \pi \cdot 20 \text{ Hz} \cdot 8 \text{ nF}} \geq 497.4 \text{ k}\Omega \quad (1)$$

1-M $\Omega$  resistors are selected for R3 and R4 to ensure the circuit meets the design requirements for  $-3$ -dB bandwidth. The center point of resistors R3 and R4 is biased to half the supply voltage through the voltage divider formed by R5 and R6. This sets the input common-mode voltage of the circuit to a value within the input voltage range of the OPA1678. Piezo elements can produce very large voltages if the elements are struck with sufficient force. To prevent damage, the input of the OPA1678 is protected by a transient voltage suppressor (TVS) diode placed across the preamplifier inputs. The TPD1E1B04 TVS was selected due to low capacitance and the 6.4-V clamping voltage does not clamp the desired low amplitude vibration signals. Resistors R14 and R15 limit current flow into the amplifier inputs in the event that the internal protection diodes of the amplifier are forward-biased.

### 8.2.2.3 Gain

The gain of the preamplifier circuit is determined by R7, R8, and R9. The gain of the circuit is given in [Equation 2](#):

$$A_V = 1 + \frac{R_7 + R_9}{R_8} = 10 \text{ V/V} \quad (2)$$

Resistors R7 and R9 are selected to be 2 k $\Omega$  to avoid loading the output of the OPA1678 and producing distortion. The value of R8 is then calculated in [Equation 3](#):

$$R_8 = \frac{R_7 + R_9}{A_V - 1} = \frac{2 \text{ k}\Omega + 2 \text{ k}\Omega}{10 - 1} = 444.4 \text{ }\Omega \rightarrow 442 \text{ }\Omega \quad (3)$$

Capacitors C3 and C4 are used to limited the bandwidth of the circuit so that signals outside the audio bandwidth are not amplified. The corner frequency produced by capacitors C3 and C4 is given in [Equation 4](#). This corner frequency should be above the desired  $-3$  dB bandwidth point to avoid attenuating high frequency audio signals.

$$C_3 = C_4 = C_{FB}$$

$$C_{FB} \leq \frac{1}{2 \cdot \pi \cdot F_{-3dB} \cdot R_{7/9}} \leq \frac{1}{2 \cdot \pi \cdot 20 \text{ kHz} \cdot 2 \text{ k}\Omega} \leq 3.98 \text{ nF} \quad (4)$$

390-pF capacitors are selected for C3 and C4, which places the corner frequency approximately 1 decade above the desired  $-3$  dB bandwidth point . Capacitors C3 and C4 must be NP0 / C0G type ceramic capacitors or film capacitors. Other ceramic dielectrics, such as X7R, are not suitable for these capacitors and produces distortion.

## Typical Application (continued)

### 8.2.2.4 Output Network

The audio signal is AC-coupled onto the microphone signal lines through capacitors C5 and C6. The value of capacitors C5 and C6 are determined by the low-frequency design requirements and the input impedance of the microphone preamplifier which connect to the output of the circuit. Equation 5 gives an approximation of the capacitor value requirements, and neglects the effects of R10, R11, R12, and R13 on the frequency response. 4.4 kΩ is used as a typical value for microphone preamplifier input impedance ( $R_{IN\_MIC}$ ) for the calculation.

$$C_5 = C_6 = C_{OUT}$$

$$C_{OUT} \geq \frac{2}{2 \cdot \pi \cdot R_{IN\_MIC} \cdot 20 \text{ Hz}} \geq \frac{2}{2 \cdot \pi \cdot 4.4 \text{ k}\Omega \cdot 20 \text{ Hz}} \geq 3.6 \mu\text{F} \quad (5)$$

For simplicity, the same 22-μF capacitors selected for the power supply filtering are selected for C5 and C6 to satisfy Equation 5. At least 50-V rated capacitors must be used for C5 and C6. If polarized capacitors are used, the positive terminal must be oriented towards the microphone preamplifier. Resistors R10 and R11 isolate the op amp outputs from the capacitances of long cables which may cause instability. R12 and R13 discharge AC-coupling capacitors C4 and C5 when phantom power is removed.

### 8.2.3 Application Curves

The frequency response of the preamplifier circuit is shown in Figure 37. The –3-dB frequencies are 15.87 Hz and 181.1 kHz which meet the design requirements. The gain within the passband of the circuit is 18.9 dB, slightly below the design goal of 20 dB. The reduction in gain is a result of the voltage division between the output resistors of the piezo preamplifier circuit and the input impedance of the microphone preamplifier. The A-weighted noise of the circuit (referred to the input) is 842.2 nV<sub>RMS</sub> or –119.27 dBu.

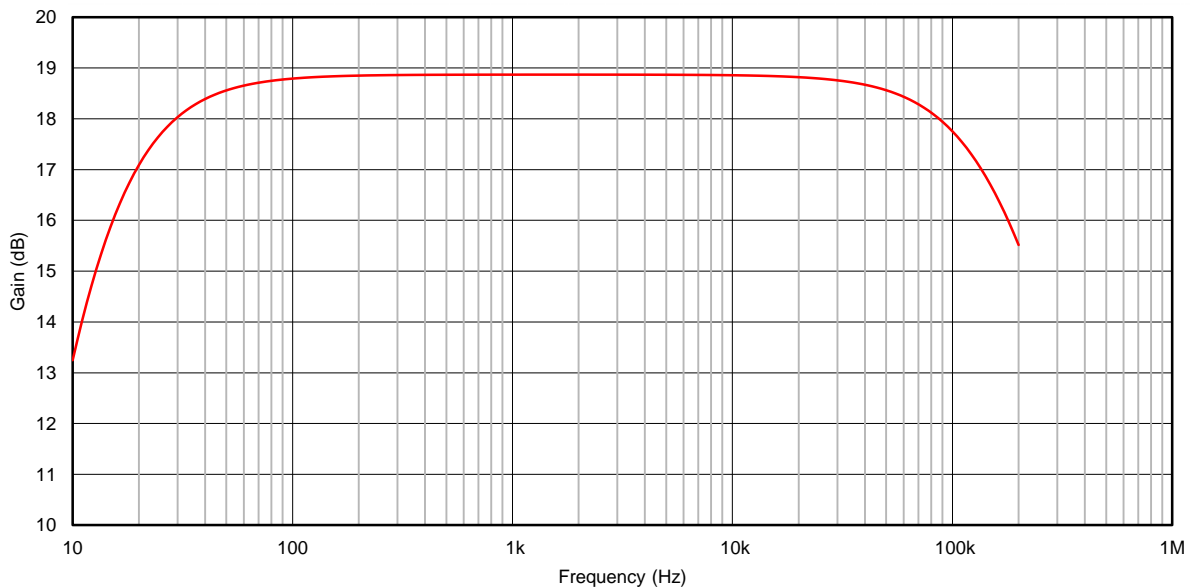


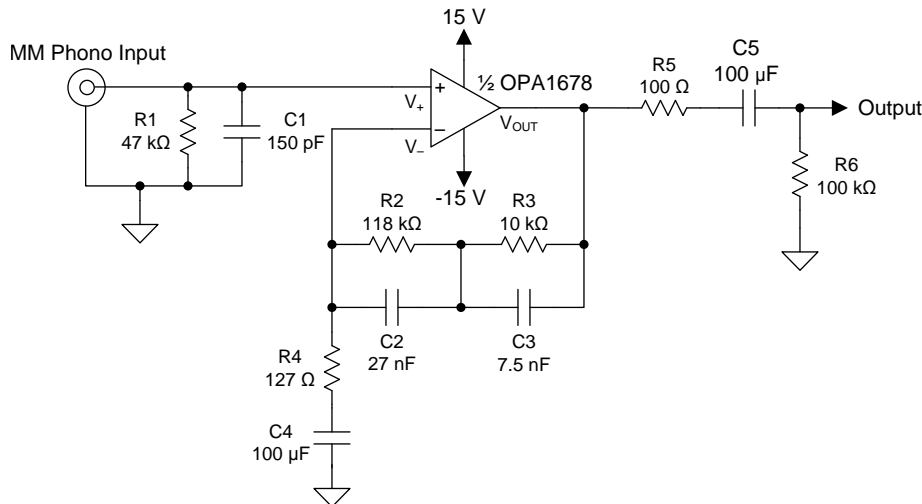
Figure 37. Frequency Response of the Preamplifier Circuit for a 8-nF Piezo Element

## 8.1 Other Applications

The low noise and distortion of the OPA167x series make the devices well-suited for a variety of applications in professional and consumer audio products. The examples shown here are possible applications where the OPA167x provides exceptional performance.

### 8.1.1 Phono Preampifier for Moving Magnet Cartridges

The noise and distortion performance of the OPA167x family of amplifiers is exceptional in applications with high source impedances, which makes these devices an excellent choice in preamplifier circuits for moving magnet (MM) phono cartridges. Figure 38 illustrates a preamplifier circuit for MM cartridges with 40 dB of gain at 1 kHz.

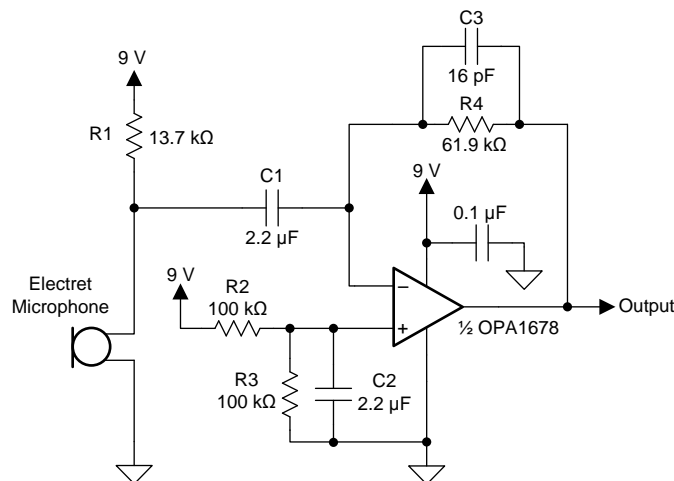


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**Figure 38. Phono Preampifier for Moving Magnet Cartridges (Single-Channel Shown)**

### 8.1.2 Single-Supply Electret Microphone Preamplifier

The preamplifier circuit shown in Figure 39 operates the OPA1678 as a transimpedance amplifier which converts the output current from the electret microphone's internal JFET into a voltage. The gain of the circuit is determined by resistor R4. Resistors R2 and R3 bias the input voltage to half the power supply voltage for proper functionality on a single-supply.



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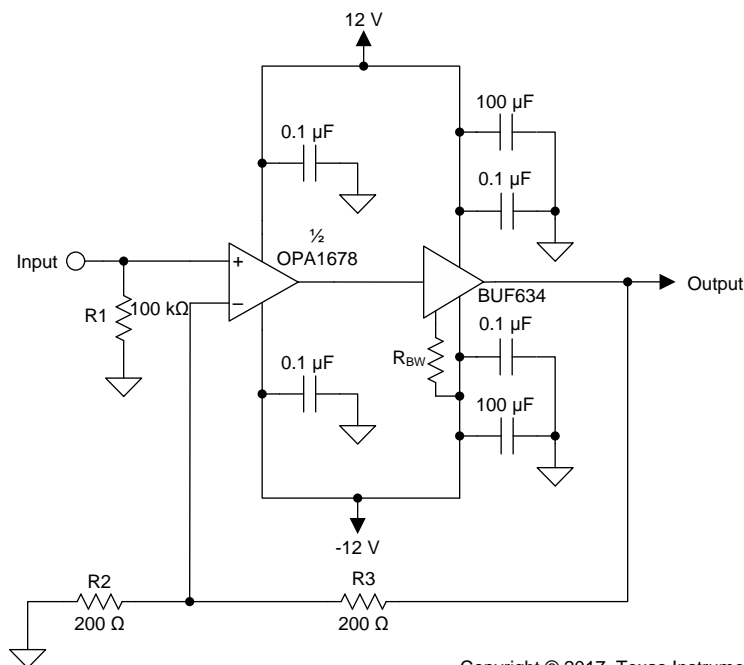
**Figure 39. Single-Supply Electret Microphone Preamplifier**



## Other Applications (continued)

### 8.1.3 Composite Headphone Amplifier

Figure 40 shows the BUF634 buffer inside the feedback loop of the OPA1678 to increase the available output current for low-impedance headphones. If the BUF634 is used in wide-bandwidth mode, no additional components beyond the feedback resistors are required to maintain loop stability.



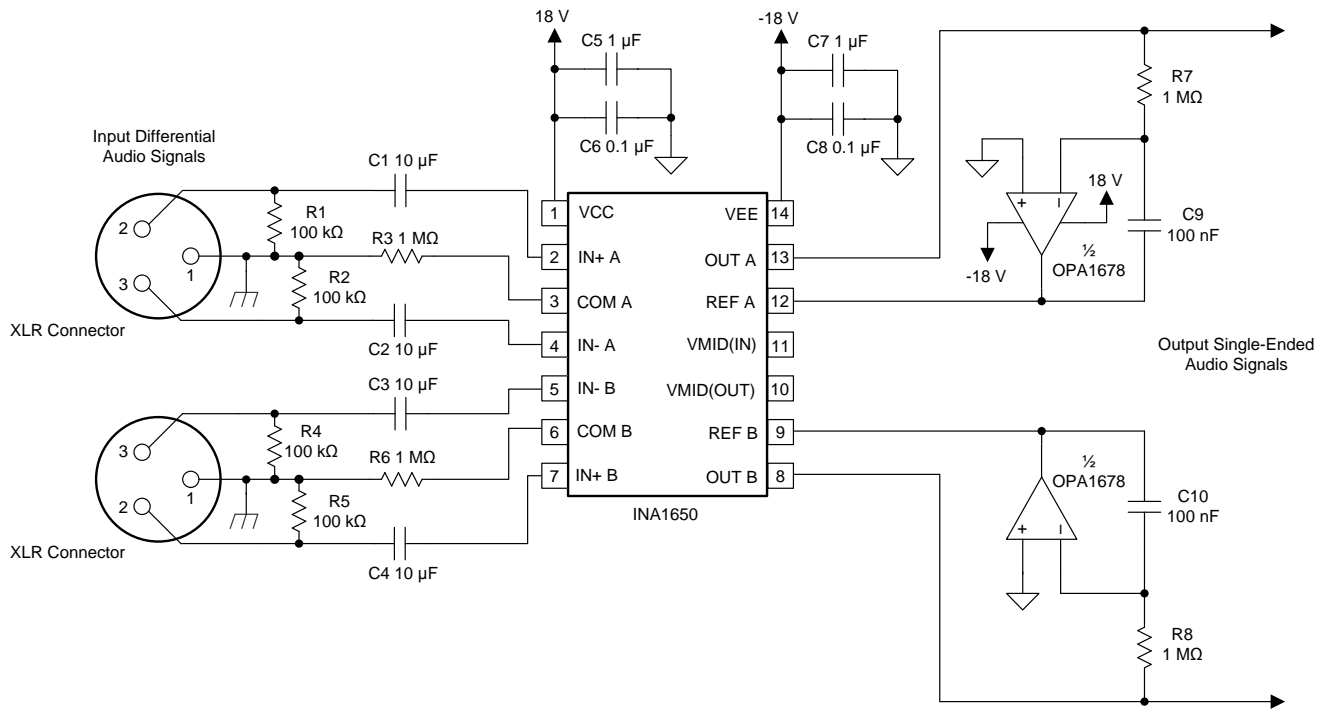
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Figure 40. Composite Headphone Amplifier (Single-Channel Shown)

### 8.1.4 Differential Line Receiver With AC-Coupled Outputs

Figure 41 shows the OPA1678 used as an integrator which drives the reference pin of the INA1650, forcing the output DC voltage to 0 V. This configuration is an alternative to large AC-coupling capacitors which may distort at high output levels. The low input bias current and low input offset voltage of the OPA1678 make the device especially well-suited for integrator applications.

Other Applications (continued)



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Figure 41. Differential Line Receiver With AC-Coupled Outputs

## 9 Power Supply Recommendations

The OPA167x are specified for operation from 4.5 V to 36 V ( $\pm 2.25$  V to  $\pm 18$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#) section. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1- $\mu\text{F}$  capacitors are adequate.

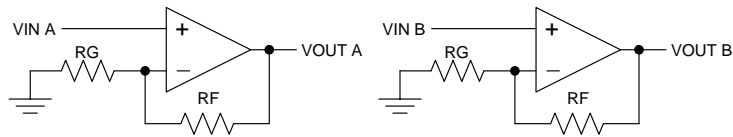
## 10 Layout

### 10.1 Layout Guidelines

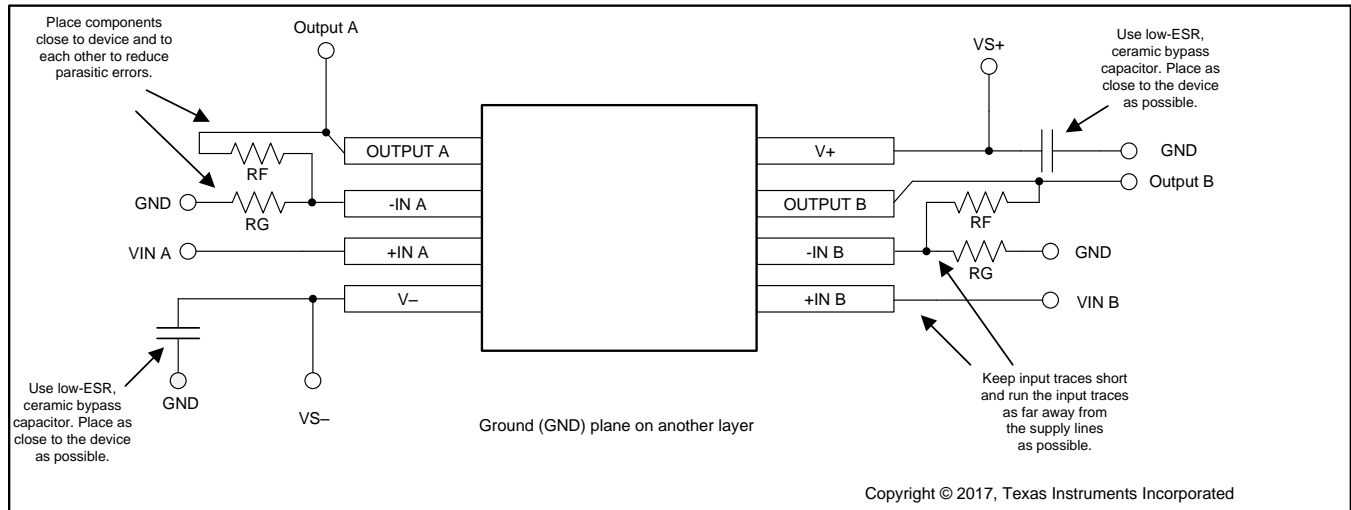
For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu\text{F}$  ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from  $V+$  to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Physically separate digital and analog grounds, observing the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in [Figure 42](#), keeping  $R_F$  and  $R_G$  close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post-cleaning bake at  $85^{\circ}\text{C}$  for 30 minutes is sufficient for most circumstances.

## 10.2 Layout Example



(Schematic Representation)


**Figure 42. Operational Amplifier Board Layout for Noninverting Configuration**

## 10.3 Power Dissipation

The OPA167x series op amps are capable of driving 2-k $\Omega$  loads with a power-supply voltage up to  $\pm 18$  V and full operating temperature range. Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA167x series op amps improves heat dissipation compared to conventional materials. Circuit board layout can also help minimize junction temperature rise. Wide copper traces help dissipate the heat by acting as an additional heat sink. Temperature rise can be further minimized by soldering the devices to the circuit board rather than using a socket.

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

##### 11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the WEBENCH® Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

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#### NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

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##### 11.1.1.2 DIP Adapter EVM

The [DIP Adapter EVM](#) tool provides an easy, low-cost way to prototype small surface mount devices. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT-23-6, SOT-23-5 and SOT-23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

##### 11.1.1.3 Universal Operational Amplifier EVM

The [Universal Op Amp EVM](#) is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of device package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, VSSOP, TSSOP and SOT-23 packages are all supported.

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#### NOTE

These boards are unpopulated, so users must provide their own devices. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

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##### 11.1.1.4 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at <http://www.ti.com/ww/en/analog/precision-designs/>.

##### 11.1.1.5 WEBENCH® Filter Designer

[WEBENCH® Filter Designer](#) is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer allows the user to create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, [WEBENCH® Filter Designer](#) allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

## 11.2 Documentation Support

### 11.2.1 Related Documentation

The following documents are relevant to using the OPA167x, and are recommended for reference. All are available for download at [www.ti.com](http://www.ti.com) unless otherwise noted.

- [Source resistance and noise considerations in amplifiers](#)
- [Single-Supply Operation of Operational Amplifiers](#)
- [Op Amp Performance Analysis](#)
- [Compensate Transimpedance Amplifiers Intuitively](#)
- [Tuning in Amplifiers](#)
- [Feedback Plots Define Op Amp AC Performance](#)
- [Active Volume Control for Professional Audio](#)

### 11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA1678	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
OPA1679	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.5 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.6 Trademarks

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 SoundPlus is a trademark of Texas Instruments Incorporated.  
 WEBENCH is a registered trademark of Texas Instruments.  
 TINA, DesignSoft are trademarks of DesignSoft, Inc.  
 is a trademark of ~ Texas Instruments.  
 is a registered trademark of ~ Texas Instruments.

### 11.7 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1678IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	1AW7	<a href="#">Samples</a>
OPA1678IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	1AW7	<a href="#">Samples</a>
OPA1678IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1678	<a href="#">Samples</a>
OPA1679IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1679	<a href="#">Samples</a>
OPA1679IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1679	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1678IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1678IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1678IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA1679IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA1679IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1678IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA1678IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA1678IDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA1679IDR	SOIC	D	14	2500	367.0	367.0	38.0
OPA1679IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



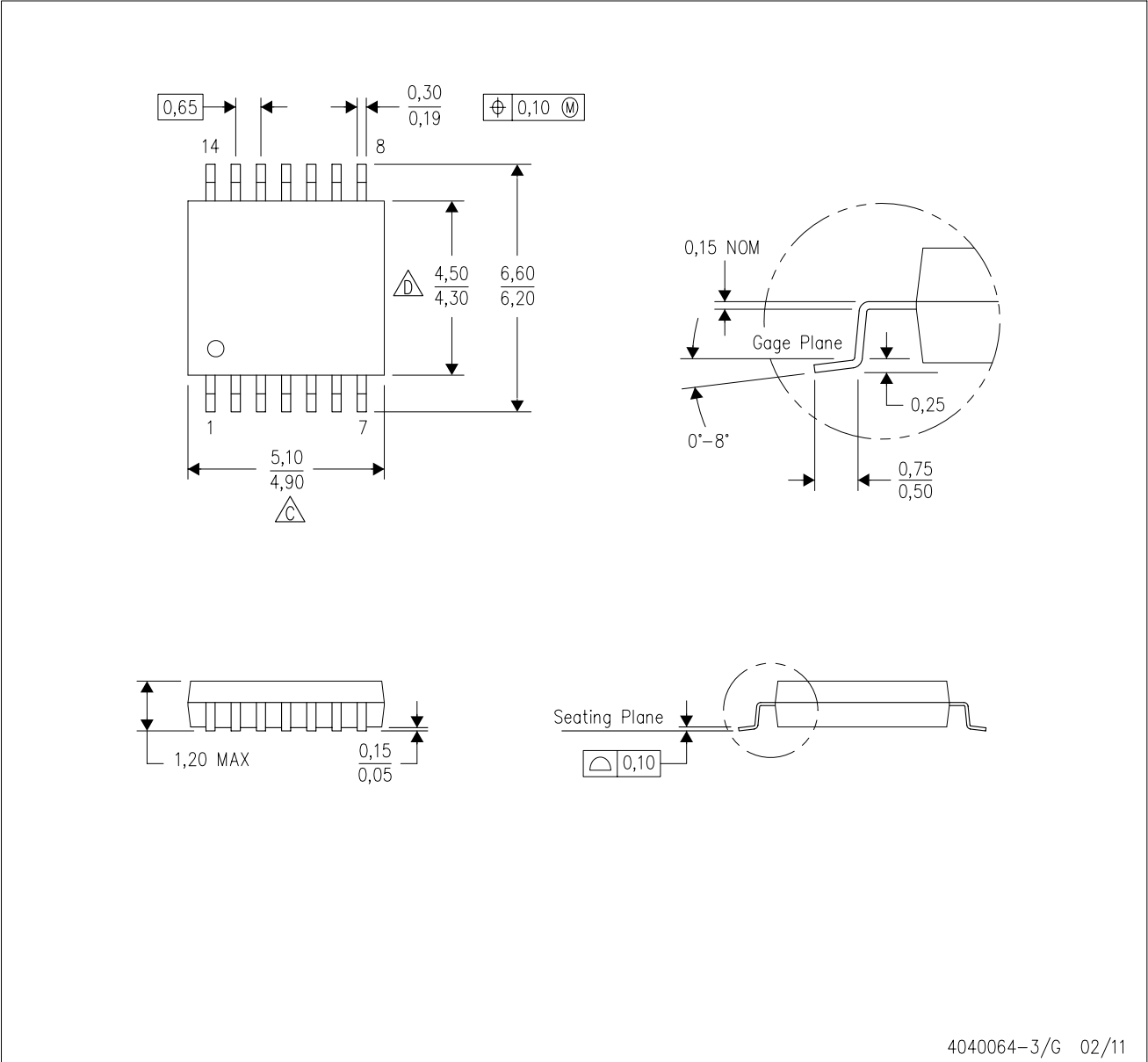
4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



**MECHANICAL DATA**

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.  
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.  
 E. Reference JEDEC MS-012 variation AA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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